A BJT-Based 0.08-mm^2 Oversampling SAR Temperature-to-Digital Converter for Thermal Drift Compensation in MEMS Inertial Sensors

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***Abstract*— This article describes a BJT-based oversampling successive-approximation-register (SAR) temperature-to-digital converter (TDC) designed for the compensation of thermal drift in high-precision micro-electro-mechanical system (MEMS) inertial sensors, increasingly employed devices in modern motion sensing applications. The system features a fully current-mode processing architecture and combines the low conversion energy advantage of SAR solutions with the resolution refining capability peculiar to ΣΔ modulators. Fabricated in a 180-nm CMOS technology, the TDC occupies a 0.08-mm^2 active area and draws 22 μA from a 1.8-V supply, resulting in a 2.5-nJ energy per sample according to the proposed temperature-to-digital conversion process. Furthermore, the sensor exhibits a 1.06% worst case inaccuracy in the −20 °C to 80 °C temperature range after a first-order trim and offers a 158-mK resolution.**

***Index Terms*— Current-mode, micro-electro-mechanical system (MEMS) thermal drift, oversampling successive-approximation-register (SAR) ADC, smart temperature sensor, temperature-to-digital converter (TDC).**

I. Introduction

MOTION sensing based on micro-electro-mechanical systems (MEMSs) plays a key role in a wide variety of applications of great interest in the current tech market; inertial navigation systems (INSs) [1], high-precision Internet-of-Things (IoT) nodes [2], consumer electronics devices [3], automotive ones [4], and many more [5], [6] usually rely on MEMS accelerometers and gyroscopes as inertial sensors, thanks to their compatibility with standard CMOS processes, compact size, and low cost [7]. One of the main issues affecting the performance of these devices is the temperature drift arising from the thermal expansion of the microstructures that compose them, resulting in a sensed quantity error which in many of the mentioned applications is not tolerable. For this reason, a first-order temperature compensation integrated circuit (IC) is often a requirement for both MEMS accelerometers [8], [9], [10], [11], [12], [13] and MEMS gyroscopes [1], [14], [15], [16], [17]. In this framework, temperature-to-digital converters (TDCs) are typically used [18]. Since the considered inertial sensors provide data in the digital domain, TDCs allow a straightforward combination of the sensed inertial quantity with the needed temperature information.

For the intended purpose, it is clear that the temperature compensation system plays an auxiliary role; accordingly, it should ensure a low impact on the performance and size of the whole inertial sensing system. Therefore, the TDC design should be driven by three main cornerstones.

1) Its conversion energy should be kept as low as possible, especially considering that most of the mentioned applications are mobile and thus battery-powered; taking into account that state-of-the-art MEMS six-axis motion sensors (that embed both an accelerometer and a gyroscope) such as [19] or [20] require an energy of at least a few hundred nJ to generate an output sample, reasonably, the TDC should not exceed a conversion energy of about 10 nJ.
2) It should feature a relatively high area efficiency; considering that a standard 180-nm CMOS process and a BJT-based approach were adopted for the proposed design as will be recalled in the following of this article, the area target was set to 0.1 mm^2 according to the compactness level of the state-of-the-art temperature sensors designed in such a mature technology node like [21] or [22].
3) The temperature resolution and accuracy requirements are quite moderate as constrained by the noise and by the inaccuracy of the output of the MEMS sensors to be compensated [23]. In light of this, a 200-mK resolution and a 2% relative inaccuracy in the industrial temperature range (−20 °C to 80 °C) have been estimated as targets.

Among the various sensing possibilities, even if resistor-based TDCs offer a higher sensitivity resulting in a better energy efficiency [24], [25], [26], BJT-based solutions are preferred, thanks to their superior linearity performance, a primary requirement given the compensating nature of

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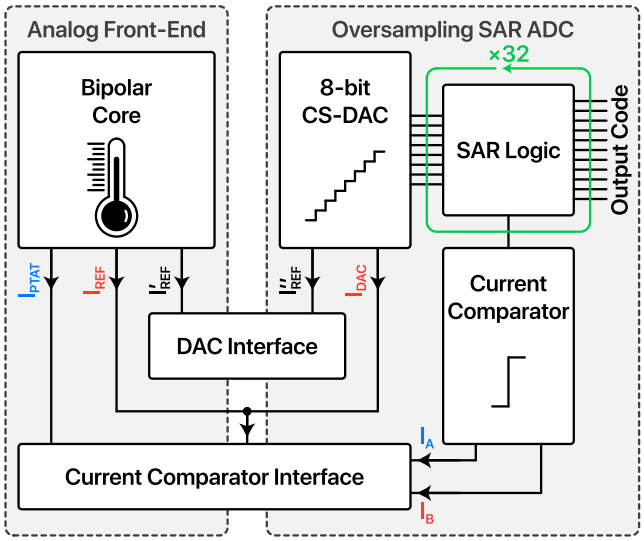

Fig. 1. Block diagram of the proposed TDC.

the temperature sensor. Taking the temperature-to-digital conversion process into account, two main approaches can be identified in this field. Low conversion energy designs typically use successive-approximation-register (SAR)-based ADCs to benefit from their relatively fast conversion process but are limited by a temperature resolution which commonly lies in the order of several hundreds of mK [27], [28], [29], [30]. Resolution-oriented designs, instead, usually rely on $\Sigma\Delta$ modulators that can achieve a temperature resolution in the order of few tens of mK but, on the other hand, feature relatively long conversion times in the order of several ms [31], [32], [33], [34], [35].

In this article, which is an extension of [36], a TDC combining the advantages of these two approaches is presented. The system, whose block diagram is shown in Fig. 1, features two main innovations: the use of a thermal-noise-based oversampling SAR (OS-SAR) ADC to convert the temperature information into the digital domain and a fully current-mode design (except for the SAR logic, every block of Fig. 1 processes signals in the form of electrical currents).

The OS-SAR allows the achievement of a conversion energy of just 2.5 nJ while offering an effective resolution of 158 mK overcoming the quantization noise limitation of conventional SAR solutions [27], [28], [29], [30]; as addressed earlier, these values provide a performance suitable with the battery lifetime specifications of the system which houses the inertial sensors to be compensated and also with the noise level of their outputs. The fully current-mode processing architecture, moreover, allows sparing several adding and amplifying circuits inherently required in its voltage-domain counterpart resulting in an op-amp-less and compact design. Accordingly, special care was devoted to its area efficiency in order not to subtract active area to the inertial sensors and their readout circuits; the TDC was fabricated in a standard 180-nm CMOS process and occupies a silicon area of 0.08 mm^2, quite competitive value in such a mature technology node.

The rest of this article is organized as follows. Section II, besides further motivating the adopted current-mode approach, discusses the proposed architecture with a focus on the transistor-level description of the main blocks of the TDC, Section III focuses on the temperature-to-digital conversion process, while Section IV presents the measurement results and includes a comparison of this work with other relevant ones in this framework. Conclusions are drawn in Section V.

II. TDC Architecture

Referring to the block diagram of Fig. 1, two parts can be identified within the TDC architecture: the analog front-end (AFE) and the OS-SAR ADC. The main circuit of the AFE is the bipolar core, which generates all the analog signals needed for the temperature-to-digital conversion: a proportional-to-absolute-temperature (PTAT) current (I_{PTAT}) and two reference currents (I_{REF} and I'_{REF}). The OS-SAR ADC, instead, consists of an 8-bit current-steering DAC (CS-DAC), a current comparator, and a SAR logic circuit, whose output is further processed by a 32× oversampling procedure. Moreover, the proper communication between the AFE module and the OS-SAR one is ensured by two dedicated interface circuits, the DAC interface and the current comparator interface.

Before moving to the circuit description of the main blocks of the proposed TDC, it is useful to further motivate the choice of a fully current-mode approach in comparison to the conventional voltage-mode SAR ADCs. The main advantage of the traditional charge redistribution SAR architectures is that the capacitive DAC they embed inherently offers a sample-and-hold (S/H) capability. However, in the temperature sensing framework no S/H circuit is needed since the information to be converted in the digital domain can be considered as a dc signal; consequently, it is worth to exploit the various benefits offered by processing signals in the current domain. First, as stated in the Introduction, the current-mode method does not require the use of operational amplifiers resulting in better compactness and reduced power consumption; indeed, signals in the form of electrical currents can be straightforwardly summed, scaled, and inverted without requiring extra circuitry which would increase the system complexity; as will be apparent in the following of this section, these basic operations are commonly required in a TDC design to set the desired conversion range, to quantize the analog input, to set the signal-to-noise ratio at the output of the AFE, and so on. In addition, the supply-voltage dependence of current-mode processing solutions is definitely less severe with respect to voltage-mode alternatives which also exhibit an upper limit for the signals to be processed (which does not exist adopting a current-mode approach) given by the supply voltage. Finally, CS-DACs typically offer significantly higher operating frequencies.

A. Bipolar Core

Fig. 2 shows the complete schematic of the bipolar core circuit. It consists of two modules, PTAT cell and CTAT cell, both based on lateral NPN transistors; the first generates three replicas of a PTAT current (I_{PTAT}, I_{PTAT1}, and I_{PTAT2}), while the

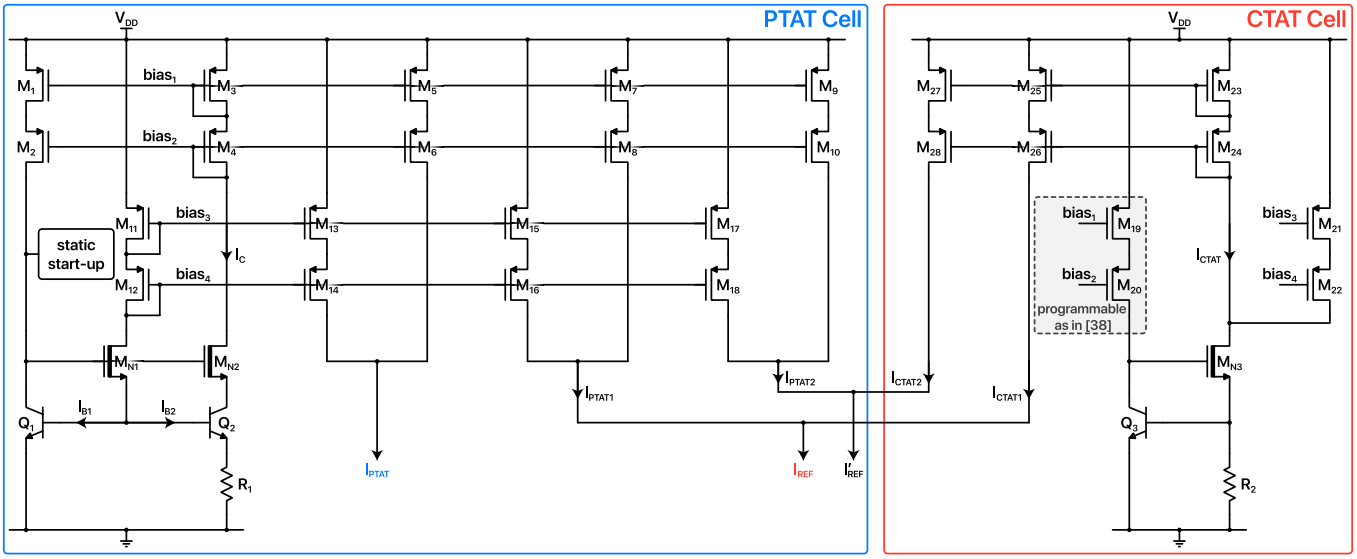

Fig. 2. Schematic of the bipolar core circuit.

second generates two replicas of a complementary-to-absolute-temperature (CTAT) current (I_{CTAT1} and I_{CTAT2}). These two cells share four bias voltages (bias$_{1-4}$) which are generated within the PTAT cell and are inherently used to drive the CTAT cell; with this arrangement, the static startup circuit [37] used to wake the PTAT cell up automatically brings also the CTAT cell to the desired operating condition.

Focusing on the PTAT cell, transistors Q_1 and Q_2 have been designed with a 1:8 emitter area (A_E) ratio to be arranged in a common-centroid configuration; accordingly, the current flowing through R_1 is PTAT ($\Delta V_{\mathrm{BE}}/R_1$). Since the β factor offered by the used NPN BJTs is relatively low ($\approx$6), a base current recovery structure has been implemented to preserve the integrity of this current signal throughout its delivery to the rest of the system. The native transistors M_{N1} and M_{N2} are used as current buffers and inherently bias the collectors of Q_1 and Q_2 at the same voltage; M_{N1} senses the sum of I_{B1} and I_{B2}, while M_{N2} senses I_C. Both these contributions are mirrored and recombined at the output according to

$$I_{\mathrm{PTAT}} = \alpha I_C + \frac{\alpha}{2}(I_{B1} + I_{B2}) \tag{1}$$

where α is the selected mirroring factor (the additional scaling factor 1/2 for the second term has been introduced to implement the average of I_{B1} and I_{B2}). Consequently, the analytical expression of the signal containing the temperature information to be converted is well-approximated by

$$I_{\mathrm{PTAT}} = \alpha \cdot \frac{\Delta V_{\mathrm{BE}}}{R_1}. \tag{2}$$

The same approach has also been adopted for the generation of I_{PTAT1} and I_{PTAT2}, which are replicas of I_{PTAT} needed for the generation of the reference currents for the OS-SAR ADC.

Shifting the focus on the CTAT cell, the I_C current is also mirrored to bias Q_3 by means of the M_3–M_4/M_{19}–M_{20} cascode structure which, in addition, has been made programmable according to [38] for calibration purposes. Moreover, the same base current recovery contribution discussed before is injected into the drain of M_{N3} by means of the M_{11}–M_{12}/M_{21}–M_{22} mirror to make I_{CTAT} current equal to V_{BE}/R_2. Two replicas of I_{CTAT} (I_{CTAT1} and I_{CTAT2}) are obtained by means of two additional mirrors and added to the corresponding PTAT signals to obtain I_{REF} and I'_{REF}, needed as references for the temperature-to-digital conversion process

$$I_{\mathrm{REF}} = \beta \cdot \frac{\Delta V_{\mathrm{BE}}}{R_1} + \gamma \cdot \frac{V_{\mathrm{BE}}}{R_2} \tag{3}$$

$$I'_{\mathrm{REF}} = \frac{\beta}{k_1} \cdot \frac{\Delta V_{\mathrm{BE}}}{R_1} + \frac{\gamma}{k_1} \cdot \frac{V_{\mathrm{BE}}}{R_2} = \frac{I_{\mathrm{REF}}}{k_1} \tag{4}$$

where β and γ are the scaling factors selected to implement the desired I_{REF} and I'_{REF} temperature dependence (shown in Section III) and where the attenuation factor k_1 present in (4) has been designed to reduce the power consumed by the DAC interface.

Eq. (5) shows the implementative equations of the scaling factors under consideration while Table I reports the chosen values of the main design parameters of the bipolar core. While the choice of the unit emitter area (A_E) was made to ensure sufficient matching between the used bipolar transistors, the values of α, R_1, and R_2 were determined within the power consumption versus ADC noise-limited resolution trade space

$$\begin{cases} \alpha = \dfrac{(W/L)_5}{(W/L)_3} = 2 \cdot \dfrac{(W/L)_{13}}{(W/L)_{11}} \\ \beta = \dfrac{(W/L)_7}{(W/L)_3} \\ \gamma = \dfrac{(W/L)_{25}}{(W/L)_{23}} \\ k_1 = \dfrac{(W/L)_7}{(W/L)_9} = \dfrac{(W/L)_{25}}{(W/L)_{27}}. \end{cases} \tag{5}$$

B. 8-Bit CS-DAC With Split Stage

Bearing the block diagram of Fig. 1 in mind, the signals generated by the bipolar core are collected by two interface

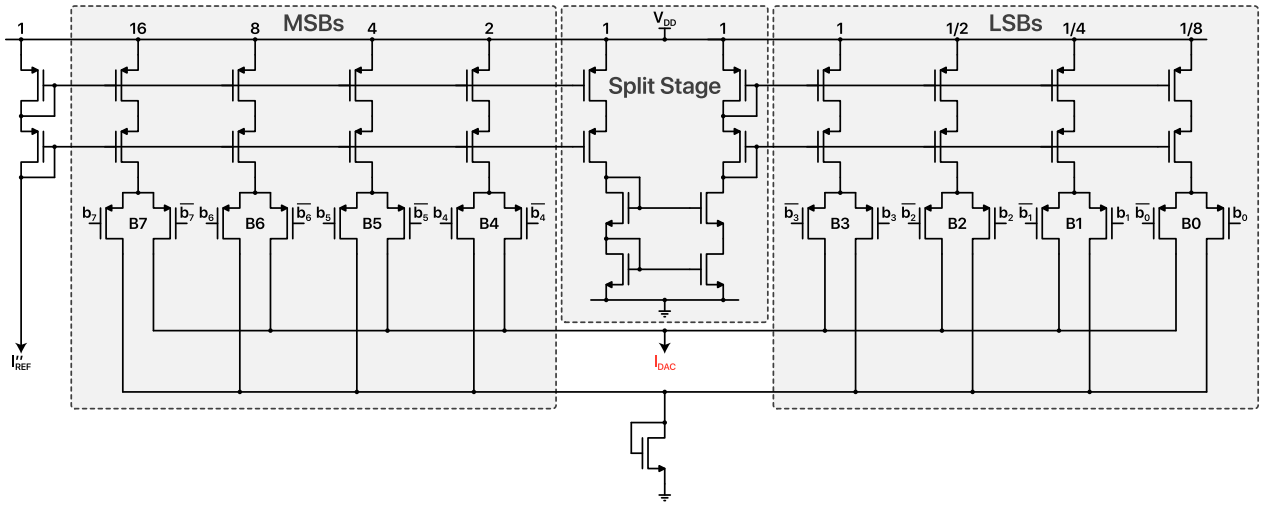

Fig. 3. Schematic of the 8-bit CS-DAC with split stage.

TABLE I
SELECTED VALUES OF THE MAIN DESIGN PARAMETERS OF THE BIPOLAR CORE

A_E	R_1	R_2	α	β	γ	k_1
$5\,\mu\text{m} \times 5\,\mu\text{m}$	$\sim 107\ \text{k}\Omega$	$3.25 \cdot R_1$	10	3.4	1	8

circuits (DAC interface and current comparator interface), which are basically NMOS current mirrors. Consequently, respectively according to (6) and (7), I''_{REF} is a $1/k_2$-scaled version of I'_{REF} while I_A and I_B are η-scaled replicas of I_{PTAT} and $I_{\text{REF}} + I_{\text{DAC}}$, respectively, I_{DAC} being the DAC output current

$$I''_{\text{REF}} = \frac{I'_{\text{REF}}}{k_2} \tag{6}$$

$$\begin{cases} I_A = \eta \cdot I_{\text{PTAT}} \\ I_B = \eta \cdot (I_{\text{REF}} + I_{\text{DAC}}). \end{cases} \tag{7}$$

Current I''_{REF} is provided as reference to a PMOS 8-bit cascode CS-DAC, whose schematic is shown in Fig. 3 (every branch is marked with its mirroring factor with respect to the reference). This circuit is controlled by the binary code provided by the SAR logic: depending on the configuration of $(b_0, b_1, \ldots, b_7)$, a larger or smaller replica of I''_{REF} is provided as output current (I_{DAC}), while a smaller or larger replica is absorbed by a diode-connected transistor. To optimize the area of the circuit and the matching among the branches corresponding to the different binary weights, this mechanism has been implemented with the three sections highlighted in Fig. 3. The reference current level has been designed corresponding to the weight of eight LSBs adopting a mid-range approach; the maximum required mirroring factor with this solution (16) is eight times smaller with respect to a standard 8-bit binary approach (128). In addition, the split stage block has been introduced to obtain a size restoration passing from the MSBs to the LSBs' section or, equivalently, to avoid all the CS-DAC mirrors to be insisting on one single reference branch; accordingly, an area optimization has been obtained

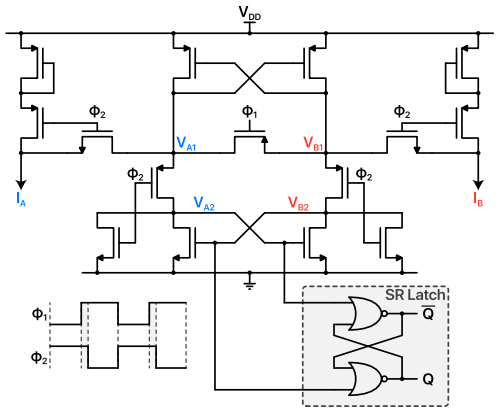

Fig. 4. Schematic of the current comparator.

and the matching requirements of the CS-DAC have been achieved with more ease. Finally, the proposed CS-DAC inherently restores the k_1 and k_2 scaling factors implemented within the generation of I'_{REF} and I''_{REF}; indeed, by design

$$k_1 \cdot k_2 = 32 \tag{8}$$

so that the full-scale I_{DAC} current turns out to be equal to the previously discussed I_{REF} current.

C. Current Comparator

As will be addressed in detail in Section III, the operation of the proposed TDC is based on a successive approximation algorithm run at a 4 MHz clock frequency: the subsequent decisions of the current comparator about the polarity of the $I_A - I_B$ difference drive the SAR logic block, which controls the CS-DAC described above. The schematic of the comparator is shown in Fig. 4; it is a current-adapted version of [39] featuring p-type current inputs which accept I_A and I_B. It is composed of a reset switch driven by the ϕ_1 signal, four complementary switches' pairs driven by the ϕ_2 signal, two diode-connected PMOS transistors, a p-type latched pair, an n-type latched one, and a set–reset latch at the output; its operation is organized according to the three phases resulting

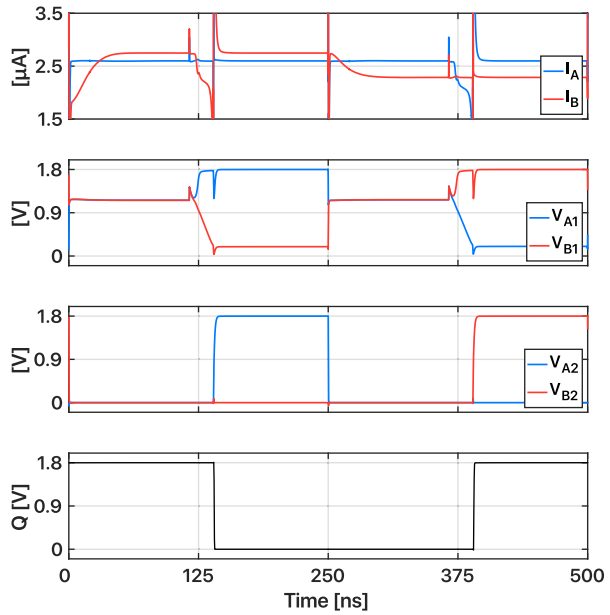

Fig. 5. Waveforms of the main signals of the current comparator during two decision cycles (simulation results).

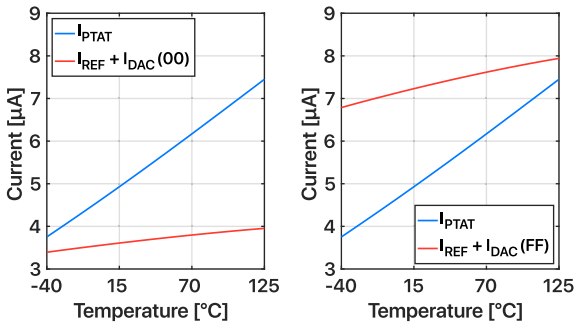

Fig. 6. Temperature characteristics of I_{PTAT} and I_{REF} + I_{DAC} at the two extremes of the DAC input range (simulation results).

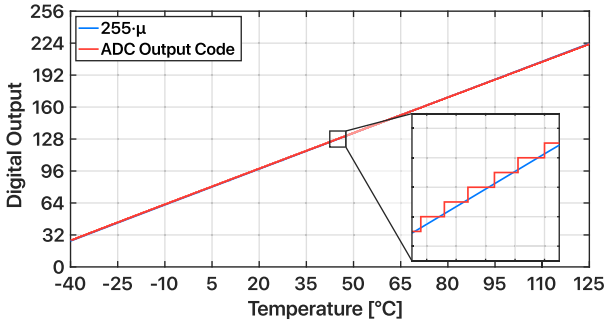

Fig. 7. Simulated TDC temperature characteristics: preconversion (blue) and postconversion (red).

from the disoverlapped rising edge of ϕ_1 with respect to the falling edge of ϕ_2, as illustrated by the conceptual waveforms of Fig. 4. When ϕ_1 is low and ϕ_2 is high (115 ns), the reset switch is on, forcing $V_{A1} = V_{B1}$ while currents I_A and I_B are absorbed by the two sides of the p-type latched pair which stays balanced; the n-type latched pair is pulled to ground with $V_{A2} = V_{B2} = 0$. As soon as ϕ_1 gets high, the p-type latched pair is free to unbalance depending on which of I_A and I_B is more intense: if $I_A > I_B$, V_{A1} falls while V_{B1} moves toward V_{DD}, vice versa if $I_A < I_B$. After 25 ns, when the direction of V_{A1} and V_{B1} is well-defined, ϕ_2 turns low kicking off the last phase of the comparison cycle which lasts for the remaining 110 ns. At this point, currents I_A and I_B are steered to the diode-connected PMOS transistors to avoid their influence on the decision transfer from the p-type latched pair to the n-type one which, implementing an additional positive-feedback gain stage, squares it at nodes V_{A2} and V_{B2}; the information about the $I_A - I_B$ sign is now available at these nodes and is finally processed by a simple set–reset latch which stores the comparator's decision until the next one is ready. Fig. 5 reports some transient analysis results of two comparison cycles simulated at room temperature (27 °C), confirming the previously described behavior. Finally, it is important to specify that the output branches of the current comparator interface have been designed to be identical to avoid a detrimental systematic offset within the comparator itself that may compromise its proper operation.

III. Temperature-to-Digital Conversion

As anticipated, the proposed system provides digital temperature data according to a SAR algorithm; it is iterated for eight clock cycles resulting in 8-bit digital words generated in 2 μs. The involved current signals, which get processed by the previously described comparator after a η-scaling (7), are I_{PTAT} and the sum of I_{REF} and I_{DAC}. Fig. 6 shows them as a function of temperature in the all-zeros CS-DAC input condition (left) and in the all-ones one (right); taking Fig. 3 and (8) into account,

$$\begin{cases} I_{DAC}(00) = 0 \\ I_{DAC}(FF) = \dfrac{255}{256} \cdot I_{REF}. \end{cases} \tag{9}$$

It can be noted that $I_{REF} + I_{DAC}$, with respect to which the temperature-to-digital conversion is carried out, is not a zero-temperature-coefficient (ZTC) signal but exhibits a slight positive slope; this feature has purposely been designed to improve the linearity of the TDC output in accordance with [40]. In addition, comparing the room temperature value of I_{PTAT} line of Fig. 6 with I_A waveform of the first strip of Fig. 5, observant readers can derive that η parameter introduced in (7) has been selected equal to 1/2. The 8-bit codes generated by the SAR conversion process track the PTAT input (I_{PTAT}) downshifted by I_{REF}; consequently, the normalized TDC digital output (μ) depends on the ratio between $I_{PTAT} - I_{REF}$ and the full-scale CS-DAC current which is nothing but I_{REF} according to its restoring feature (8). Recalling (2) and (3),

$$\mu = \frac{I_{PTAT}}{I_{REF}} - 1 = \frac{\alpha \cdot \frac{\Delta V_{BE}}{R_1}}{\beta \cdot \frac{\Delta V_{BE}}{R_1} + \gamma \cdot \frac{V_{BE}}{R_2}} - 1. \tag{10}$$

This is fully confirmed in Fig. 7 where the TDC temperature characteristic is shown; the preconversion simulated digital output is compared with the actual ADC output and they turn out to be well-matched (given the number of bits, a proportionality factor of 255 is considered).

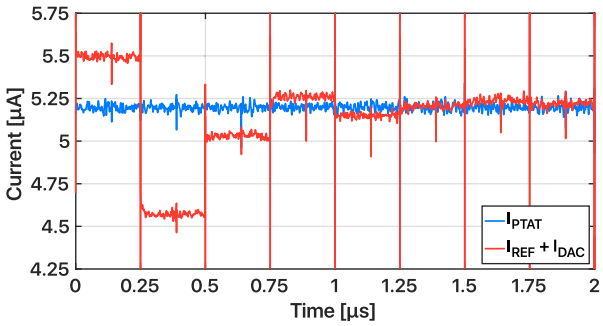

Fig. 8. SAR algorithm on I_{PTAT} and I_{REF} + I_{DAC} (noise transient simulation results).

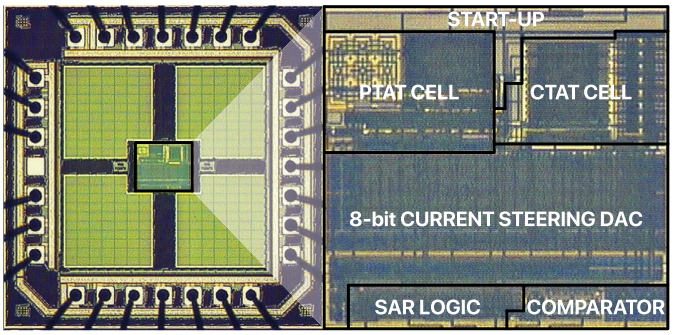

Fig. 9. Chip micrograph and magnified view of the active area with its breakdown.

To obtain an effective temperature resolution refinement, an oversampling procedure has been introduced at the output of the TDC (as indicated in the block diagram of Fig. 1); this approach, which requires the quantity to be processed to exhibit some kind of variability, has been possible thanks to the presence of electronic noise in the system. To support this, Fig. 8 shows the result of a noise transient simulation reporting the SAR algorithm iterated on I_{PTAT} and $I_{REF} + I_{DAC}$ in action. It can be noted that the thermal noise affecting the two considered signals has no impact on the first decisions of the comparator; the last decisions, instead, are basically random as the comparator is no longer able to discriminate between I_{PTAT} and $I_{REF} + I_{DAC}$. This effect results in a degree of uncertainty among the TDC's output codes even considering a fixed temperature, making the aforementioned oversampling possible; in particular, this is done by collecting the results of 32 different 8-bit conversions on which a decimation is carried out (the decimation filter has been kept off-chip for testing flexibility reasons) improving the TDC's resolution at the cost of a longer conversion time (64 μs). For the sake of generality, considering only the thermal noise contribution and an ideal decimator, this approach ensures a benefit of a factor $\sqrt{2}$ to the resolution of the sensor for every doubling of the number of samples (N) used to build each refined one according to

$$\mathrm{Res}_{\mathrm{OS}} = \frac{\mathrm{Res}_i}{\sqrt{N}} \tag{11}$$

where Res_i is the intrinsic resolution while $\mathrm{Res}_{\mathrm{OS}}$ is the oversampled one. At first glance, the fact of having a resolution benefit, thanks to the presence of noise in the system, may sound paradoxical; however it is important to highlight that if there was no variability among the 8-bit samples generated by the TDC, the quantization noise would completely mask the analog temperature value which is instead digitally extractable with the proposed technique.

IV. Measurement Results

The proposed TDC was fabricated in a standard 180-nm CMOS process and both the AFE module and the OS-SAR one have been supplied at 1.8 V. Fig. 9 shows the chip micrograph and a magnification of its active area with its breakdown while the used measurement setup is reported in Fig. 10. Including pads, the die area is equal to 1700 $\times$ 1700 μm while the core is a 298 $\times$ 268 μm rectangle (corresponding to an active area of less than 0.08 mm^2). Because of the pad-limited scenario, the free space around the core has been exploited to place four filtering capacitors to clean up the supply voltage while the resulting lanes have been reserved for the interconnections of the signals of interest with the pads. Taking the active area breakdown into account, the arrangement of the main blocks of the TDC can be seen: the PTAT cell and the CTAT cell have been placed side by side in the upper part of the core with their startup circuit placed on top. In addition, it is clear that the CS-DAC is the most area consuming block due to the matching constraints of its branches and occupies the central part of the core; the SAR logic and the current comparator, instead, have been placed below. Finally, the dies were enclosed in DIL28 ceramic packages.

Twenty samples from one batch were characterized in a thermal chamber (Vötsch VT4004) from −20 °C to 80 °C with steps of 10 °C according to the measurement setup illustrated in Fig. 10. Each device under test (DUT) got supplied keeping the analog and the digital voltage domains separated (avdd and dvdd) while the reference clock signal was provided from outside for testing flexibility. On top of that, a LabVIEW-automated testing routine has been implemented; besides controlling the thermal chamber status performing the desired temperature sweep, exploiting an external data acquisition (DAQ) system and a flat cable, the 8-bit TDC output codestream was read and the needed calibration procedures were carried out.

A. Power Consumption

The consumption measurements carried out on the fabricated samples showed that the analog part of the TDC draws about 13 μA from the supply while the digital part draws about 9 μA; considering that a 1.8-V supply voltage is adopted, in total the device consumes 39.6 μW. Since the system is clocked at 4 MHz, the conversion energy of a digital sample refined according to the previously described temperature-to-digital conversion process turns out to be as low as 2.5 nJ (= 39.6 μW $\times$ 250 ns $\times$ 8 $\times$ 32). Fig. 11 shows the power consumption breakdown among the main blocks of the TDC; the power consumption of the interface circuits has been included in the one of the neighboring blocks while the SAR logic one has been omitted due to its negligible contribution.

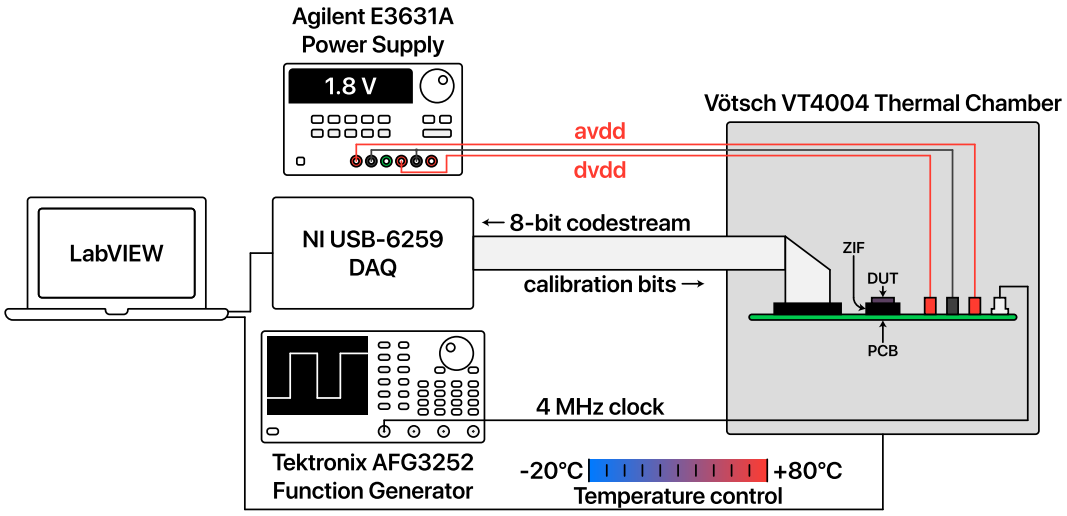

Fig. 10. Used measurement setup.

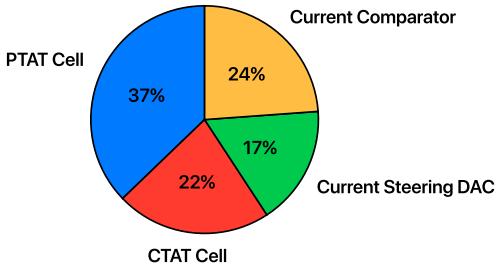

Fig. 11. TDC power consumption breakdown.

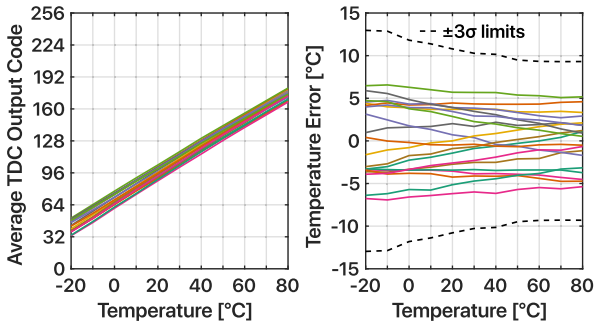

Fig. 12. Measured untrimmed TDC output characteristics with correspondent temperature errors (20 samples).

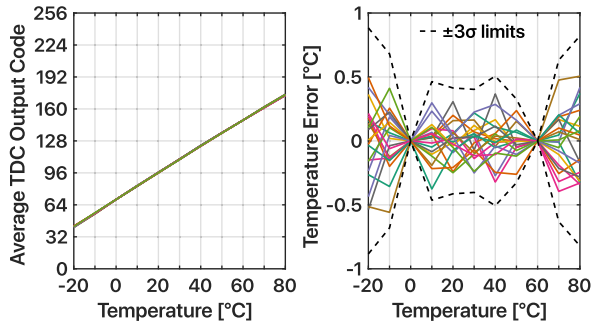

Fig. 13. Measured first-order trimmed TDC output characteristics with correspondent temperature errors (20 samples).

B. Temperature Inaccuracy and Linearity

The thermal response of the 20 measured samples was analyzed to evaluate the inaccuracy performance of the proposed TDC in the industrial temperature range. Fig. 12 (left) shows the measured untrimmed temperature characteristics in which the average TDC output code is considered; on the right, the correspondent temperature errors with the $\pm 3\sigma$ limits are reported. It can be noted that the reported characteristics are affected by a spread that translates into a 13.52% worst case relative accuracy in the considered range of interest which is not compliant with the targeted application requiring a 2% or lower accuracy value. To improve temperature inaccuracy, in [36] the sensors were calibrated according to a room temperature (30 °C) offset compensation followed by a slope trimming on the basis of the upper bound (80 °C) temperature measurement exploiting the previously mentioned programmability of the collector current of Q_3 [38]; with this approach, a 1.39% worst case inaccuracy was achieved. Alternatively, in this work, a more effective first-order calibration was carried out based on the 0 °C and 60 °C measured average codes. The resulting accuracy performance is reported in Fig. 13: the reduced spread of the resulting set of characteristics is clearly visible with a final temperature error well below ±1 °C. This corresponds to a 1.06% worst case relative inaccuracy meeting the desired performance level. The nonlinearity error of the proposed TDC was also measured. Fig. 14 reports the experimental results collected on the same 20 samples discussed above; the observed worst case nonlinearity is approximately equal to ±1 °C, while the $\pm 3\sigma$ one, as highlighted by the reported limits, amounts to −1.33 °C/+1.09 °C.

C. Temperature Resolution

To evaluate the TDC's resolution performance, 50 000 samples were acquired and analyzed while keeping a fixed controlled temperature and a fixed trimming condition. As presented in Section III, the 8-bit samples generated by the OS-SAR ADC were processed by an off-chip decimation filter to study the proposed resolution refining process; considering

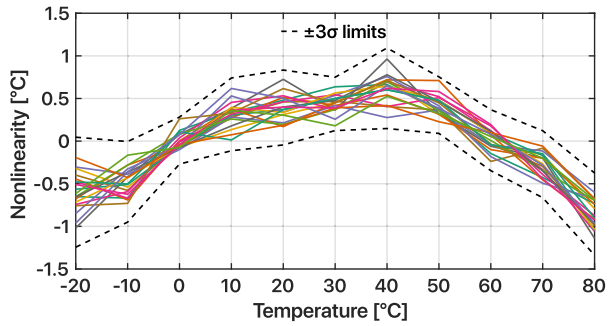

Fig. 14. Measured nonlinearity error (20 samples).

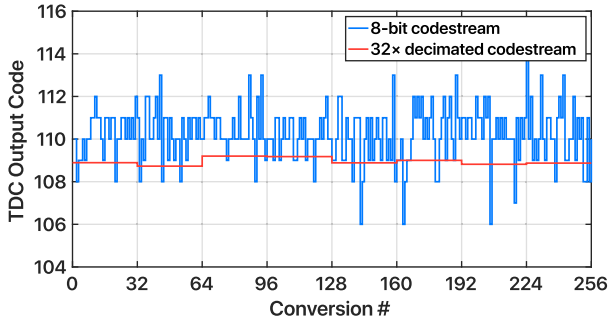

Fig. 15. Measured room temperature TDC output: 8-bit codestream (blue) and 32× decimated codestream (red).

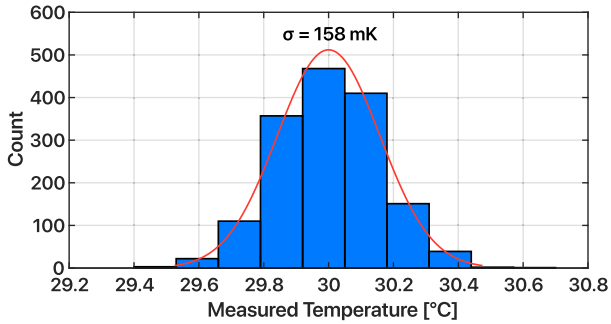

Fig. 16. TDC temperature resolution evaluation considering an oversampling factor of 32 (1562 samples).

an oversampling factor of 32, it was possible to examine more than 1500 refined digital samples. Fig. 15 shows the result of 256 8-bit room temperature conversions as an example (blue curve); in addition, the 32× decimated codestream is superimposed (red curve) and clearly exhibits a strongly reduced variability confirming the effectiveness of the adopted technique. Taking all the 50 000 8-bit conversions into account, their measured nonoversampled rms resolution turns out to be equal to 902 mK; considering, instead, all the available refined samples whose complete statistical distribution is shown in Fig. 16, their resolution is equal to 158 mK in full accordance with (11). In addition, Fig. 17 reports the measured resolution as a function of the conversion time; this graph has been obtained by sweeping the number of samples involved in the decimation process (N): starting with N equal to 1 (corresponding to a 2-μs conversion time, that is of single 8-bit conversions) at the left boundary, the shown curve is well-approximated by a straight line considering log-scaled

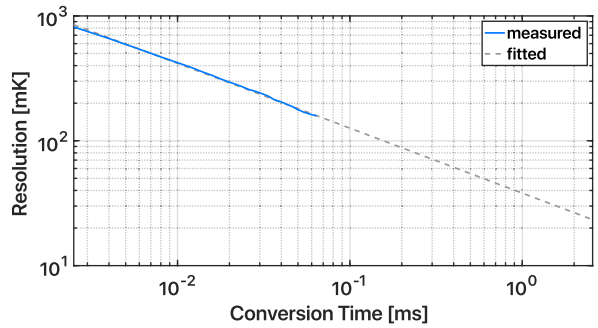

Fig. 17. Measured TDC resolution as a function of the conversion time with fit trend line.

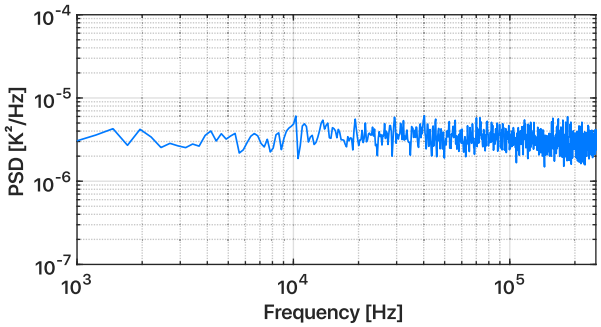

Fig. 18. Measured TDC power spectral density (Hanning window, 2048 samples, 16× averaging).

axes. This validates again the rule expressed within (11) and is further supported by the power spectral density shown in Fig. 18 which is purely white.

D. Prior Art Comparison

Table II reports a performance summary of this work and compares it with the recent BJT-based TDCs. Four SAR-based works and four $\Sigma\Delta$-based ones have been selected as frame of reference to highlight that the proposed TDC, employing an OS-SAR converter, combines the advantages of both approaches; accordingly, it exhibits an excellent conversion energy of 2.5 nJ while offering a 158-mK temperature resolution clearly being an intermediate solution between strongly low-energy oriented designs [27], [28], [29], [30] and high-resolution oriented ones [31], [32], [33], [34]. This results in a 63 pJ·K^2 resolution FoM [41].

In addition, considering the BJT-based works collected in [42] fabricated in similar technology processes with respect to the proposed one (130-, 160-, and 180-nm CMOS), the 0.08 mm^2 active area value turns out to be definitely competitive. This is further supported by the graphical comparison reported in Fig. 19 where conversion energy and area are taken into account. Alongside [29] and [43], the proposed TDC ranks among the best ones, leading the highlighted trend.

It is important to underline that the reported performance, in keeping with the policy adopted in the referenced works, does not include the power consumption and area of the decimation filter and of the clock generation circuit that, for testing flexibility reasons, have been kept off-chip. To further

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH RECENT BJT-BASED TDCS

	[27] ISSCC 2018	[28] SSC-L 2019	[29] TCAS-II 2020	[30] VLSI 2022	[31] TCAS-II 2019	[32] JSSC 2020	[33] TCAS-I 2020	[34] JSSC 2022	**This work 2024**
ADC Type	SAR	SAR	SAR	SAR	$\Sigma\Delta$1	$\Sigma\Delta$2	$\Sigma\Delta$1	$\Sigma\Delta$2	**OS-SAR**
Technology [nm]	22	16	180	4	55	160	65	180	**180**
Area [mm^2]	0.004	0.0025	0.121	0.006	0.015	0.146	0.003	0.42	**0.08**
Temperature Range [°C]	-30 to 120	-15 to 105	-10 to 100	-10 to 100	-40 to 125	-40 to 180	-10 to 110	-50 to 180	**-20 to 80**
Supply Voltage [V]	1.0	0.85	1.0	1.0	1.0	1.8	1.3	1.5	**1.8**
Measured Samples	38	103	15	30	12	24	25	25	**20**
Relative Inaccuracy [%]	1.43[a]	2.92[a]	4.27[b]	3.25[b]	2.06[a]	0.18[a]	2.25[b]	0.39[a]	**1.77[a]/1.06[b]**
Trimming Points	1	0	1	2	0	1	2	1	**2**
Power [µW]	50	18	0.0005	64	37	9.8	111.8	3.8	**39.6**
Conversion Time [ms]	0.032	0.013	200	0.011	32.8	20	4.1	8.3	**0.064**
Conversion Energy [nJ]	1.6	0.23	0.098	0.7	1214	195	460	32.5	**2.5**
Resolution [mK]	580	300	590	460	20	23	65	18	**158**
Resolution FoM[c] [pJ·K^2]	538	21	34	148	486	103	1944	10	**63**

[a]$\pm 3\sigma$ inaccuracy. [b]Worst case inaccuracy. [c]Defined in [41].

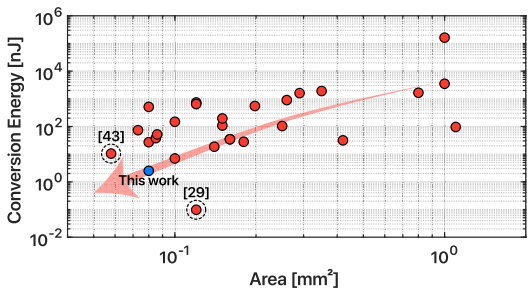

Fig. 19. Graphical comparison of the proposed TDC with state-of-the-art works taking conversion energy and area into account.

clarify the practical applicability of the proposed TDC, it is useful to discuss their impact if embedded within the presented IC. As concerns the digital filter, it is reasonable to assume that both its consumed power and its area occupation would be comparable to the SAR logic included in the proposed system since it exhibits a similar complexity; its power consumption, as reported in Section IV-A, is negligible with respect to the other items of the breakdown while its area, as visible in Fig. 9, is rather limited. The clock generation circuit, conversely, would contribute to a nonnegligible power consumption and area; indeed, state-of-the-art MHz-range oscillators commonly exhibit a power consumption in the order of tens of μW while occupying at least 0.01 mm^2 [44], [45], [46]. Nevertheless, since the clock generation circuit would not serve the proposed TDC alone but an entire inertial measurement unit which commonly features area and power of over an order of magnitude higher, its impact on the reported performance would be particularly small.

V. CONCLUSION

A TDC for the temperature compensation of high-precision MEMS inertial sensors has been presented. Featuring a BJT-based analog core, the system fully operates in the current-mode domain achieving a significant degree of compactness (active area of 0.08 mm^2) considering the adopted 180-nm CMOS technology node. In addition, the proposed solution combines the low conversion energy benefit of SAR TDCs with the resolution refining capability of $\Sigma\Delta$-based solutions using an OS-SAR ADC to obtain temperature-dependent digital data. With a total power consumption of 39.6 μW, the system achieves a 158-mK temperature resolution with a conversion energy of just 2.5 nJ, excellent performance level to ensure an adequate lifetime of the battery supplying the motion sensors to be compensated and considering the noise affecting the sensed inertial signals. Finally, the 1.06% worst case inaccuracy resulting from the 20 samples characterized in the −20 °C to 80 °C temperature range after a first-order calibration turns out to be in line with the requirements of the considered application.

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