Influence of Parasitic Capacitance on Turn-Off Current and Its Optimization Method for Transient Electromagnetic System

Xian Liao, Zhengyu Xu, *Member, IEEE*, Wei Liu, Xuquan Hu, Jie Zhou, and Zhihong Fu

***Abstract*— In transient electromagnetic (TEM) inverter circuits, a damping resistor is typically connected in parallel to the transmitting coil to prevent overshoot during the turn-off period of the pulse current. This configuration results in an exponential decay waveform for the pulse current, which prolongs the turn-off time and increases the nonlinear error. This article analyzes the impact of the parasitic capacitance on the value of the damping resistor and the end-period waveform of the pulse current base on the inverter circuits, and proposes an optimized control method to reduce both the turn-off time and the nonlinear error of the pulse current. The method is validated through the construction of an experimental circuit. According to the experimental data, this optimization method reduces the turn-off time by 23.8% and the nonlinear error by 5.5%. In the unexploded ordnance (UXO) detection experiment, the optimization method's detection results exhibit higher resolution.**

***Index Terms*— Parasitic capacitance, tail current (TC), transient electromagnetic (TEM), unexploded ordnance (UXO) detection.**

I. Introduction

THE transient electromagnetic method (TEM) is a widely employed geophysical exploration technique. It operates by generating a primary magnetic field through the production of a bipolar pulse current in the transmitting coil. The secondary electromagnetic field induced during the pulse current turn-off period is then detected. Subsequently, the secondary electromagnetic field data are processed by means of inversion techniques in order to extract valuable information on subsurface geological structures. TEM has found extensive application in mineral exploration, engineering surveys, and related fields [1], [2], [3], [4].

The current inverter is a pivotal component of the TEM system. The turn-off characteristic of the pulse current is one of the most critical factors influencing the TEM response and data interpretation [5], particularly in applications such as shallow surface detection [6]. Therefore, to improve the detection accuracy and shallow geological structure detection capability, it is necessary to reduce the turn-off time and the nonlinear error of the falling edge of the pulse current [7], [8].

An effective strategy for reducing turn-off time and nonlinear errors involves the use of the active clamp circuit. This approach typically uses a high-voltage bulk capacitor to clamp the falling edge of the pulse current [9]. For instance, rapid turn-off of the pulse current was achieved through the resonance of the high-voltage capacitor with the transmitting coil [10]. However, this method yields the falling edge of the pulse current similar to the sinusoidal waveform, resulting in a larger nonlinear error. To address this, a bulk clamping capacitor is deployed and its voltage is maintained at a relatively constant level to yield a highly linear turn-off waveform [11]. Furthermore, the oscillation at the end period of the pulse current's falling edge can be eliminated by connecting a damping resistor in parallel to the transmitting coil, which can further decrease the nonlinear error [12]. Implementing an RCD snubber circuit into the full bridge circuit can also curb the oscillation induced by stray inductance, thereby reducing the nonlinear error [13]. Zhang et al. [14] proposed a method distinct from matching damping resistors, which eliminates the oscillation by using the *RC* snubber circuit and pole configuration. This approach achieves the same performance as using damping resistors, without requiring the switching device to connect the damping resistor to the circuit. However, using this method will cause the pulse current to have an overshoot phenomenon.

However, these circuits pose a challenge. At the end period of the current's falling edge, the clamping effect will eventually disappear. Consequently, for the inverter circuit equipped with a damping resistor or *RC* snubber, the current continues to flow through the damping resistor or *RC* snubber circuit, resulting in exponential decay [12], [13], [14], [15]. For the circuit without a damping resistor or *RC* snubber, the current oscillates via the coil's parasitic capacitance and internal resistance [9], [10], [11]. We defined the current during this time as the tail current (TC). Evidently, the existence of an exponentially decaying or oscillating TC escalates the off-time and non-linear error of the pulse current.

The initial attenuation value of the TC is primarily determined by the ratio between the clamping voltage and the damping resistance. As a result, if the damping resistance value is exceedingly small, it will cause an increment in the

Manuscript received 28 May 2023; revised 17 August 2023; accepted 29 August 2023. Date of publication 14 September 2023; date of current version 21 December 2023. This work was supported in part by the Natural Science Foundation of Chongqing, China, under Grant CSTB2023NSCQ-MSX0449, and in part by the Theoretical Research on UAV Transient Electromagnetic Method for Site Selection of Mountain Power Engineering Project of Science and Technology Research Program of Chongqing Education Commission of China under Grant KJQN202301430. The Associate Editor coordinating the review process was Dr. Hamed Hamzehbahmani. *(Corresponding authors: Zhengyu Xu; Zhihong Fu.)*

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Digital Object Identifier 10.1109/TIM.2023.3315408

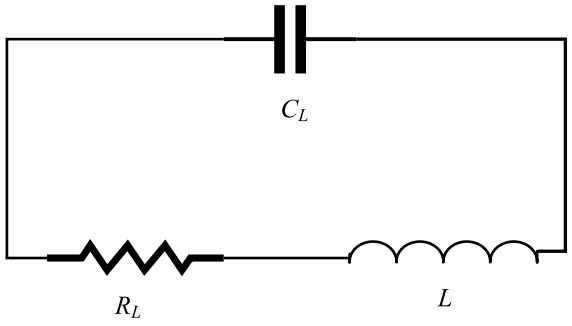

Fig. 1. Model of the air-core coil.

initial value of the TC. Conversely, an overly large value could lead to a zero-crossing or oscillation in the TC. Therefore, it is crucial to determine the optimal value of the damping resistance for analyzing the TC. Typically, this calculation is performed based on a second-order circuit model comprised of the transmitting coil's inductance and parasitic capacitance under critical damping conditions [5], [16], [17], [18]. However, this method disregards the impact of the switching device's parasitic capacitance on the critical damping resistance value. But it not only influences the damping resistor's value but also significantly affects the initial value and the waveform of the TC.

The objective of this article is to analyze the impact of the switching device's parasitic capacitance on the optimal value of the damping resistor and the waveform of the TC. We then propose a novel optimization control method designed to reduce the turn-off time and the nonlinear error of the TC. Following the application of this control method, we compute the TC's waveform. Based on this waveform, we utilize numerical methods to determine the optimal solution for the initial value of the TC, aiming to minimize the non-linear error. Ultimately, reduce the impact of the TC on detection and improve the detection accuracy and shallow detection capability of the TEM system.

II. Circuit Model Analysis

A. Circuit Model of the Transmitting Coil

The small loop TEM system usually uses a multiturn air-core coil as its transmitting coil, and the circuit model [17] shown in Fig. 1 is usually used to analyze the transient process of the coil in the inverter circuit. In this figure, L is the coil inductance, R_L is the coil resistance, and C_L is the coil's parasitic capacitance.

As the value of the parasitic capacitance is typically small, its impact is usually ignored in the constant voltage clamp circuit models. However, the parasitic capacitance, inductance, and damping resistor together form a second-order circuit that gives rise to the phenomenon of the TC. As a result, it is crucial to consider the impact of parasitic capacitance C_L when analyzing the transient process of the TC. The value of C_L is usually measured by using the parallel resonance phenomenon between the parasitic capacitance and the inductance.

B. Active Clamping Circuit

In this section, we will use the active clamping circuit [12] as an example to analyze the circuit process and determine

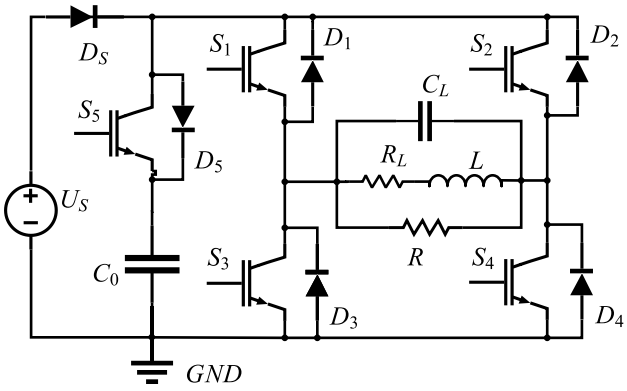

Fig. 2. Basic model of the active clamp circuit.

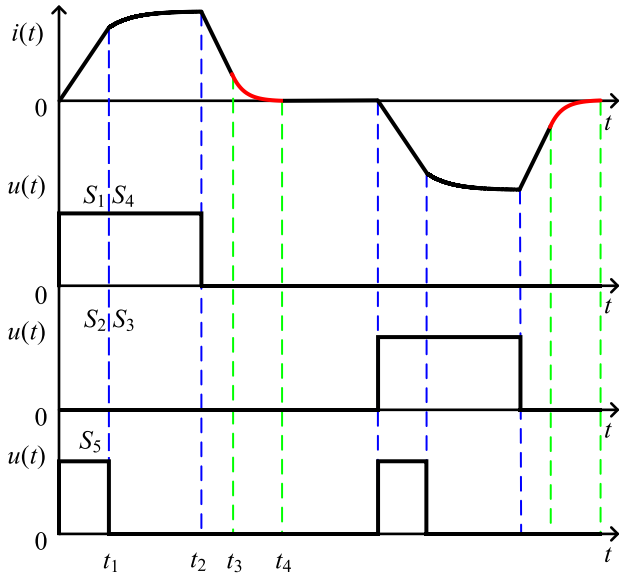

Fig. 3. Control signals and pulse current.

the optimal value of the damping resistance. The basic circuit model is shown in Fig. 2. Switches S_1, S_2, S_3, and S_4 constitute a full-bridge inverter circuit, R_L C L is the equivalent model of the air-core coil, switch S_5 and capacitor C_0 constitute the constant voltage clamping circuit, and R is the damping resistor.

The circuit operates by storing energy through the use of the large capacitor C_0, which helps to maintain a relatively stable voltage across the inductor L during the falling edge period of the pulse current. This results in a rapid and linear turn-off of the pulse current. During the rising edge period, the high voltage of the capacitor C_0 is utilized to increase the rising speed of the current. The voltage of capacitor C_0 is maintained relatively stable by storing energy during the falling edge period and releasing energy during the rising edge period. The control signal of switches S_1, S_2, S_3, S_4, S_5, and pulse current waveform are shown in Fig. 3.

In Fig. 3, it is assumed that the circuit has reached a stable operating state before time 0. At time 0, switches S_5, S_1, and S_4 are turned on, and the high voltage across capacitor C_0 makes the pulse current rise rapidly. At time t_1, switch S_5 is turned off, while switches S_1 and S_4 remain on, and the power supply U_S supplies power to inductor L through D_S,

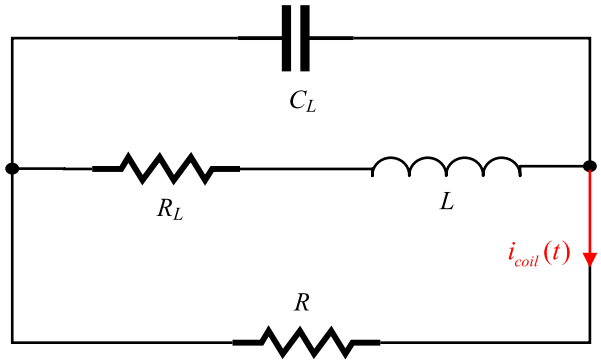

Fig. 4. Equivalent circuit model during t_3–t_4.

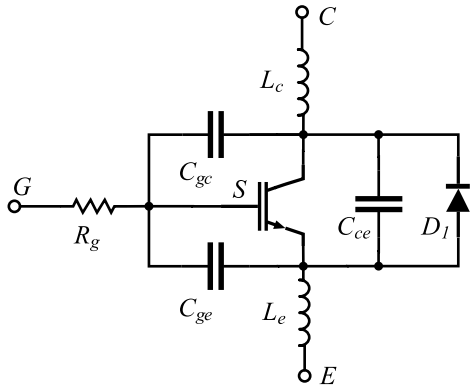

Fig. 5. Parasitic parameter model of IGBT.

S_1, and S_4. Therefore, the current rises slowly until it reaches the maximum current I_0. At time t_2, switches S_1 and S_4 are turned off, and the inductor L charges the clamp capacitor C_0 through D_2, D_5, and D_3. During this period, the voltage of C_0 will gradually increase. In the following analysis, we assume that the capacitance of C_0 is large enough to ignore any change in the clamping voltage U_0. In addition, it is noteworthy that as t_1 decreases, U_0 will increase. This feature can be exploited to achieve the shortest current falling edge time within the allowable withstand voltage of the switches. Additionally, by controlling t_1, the turn-off time of the pulse current can be dynamically adjusted [5].

During t_3–t_4, $|U_L| < |U_0|$, D_2, D_5, and D_3 are off, and the equivalent circuit during this period is shown in Fig. 4. The current of the air-core coil during this period is the TC.

Since the actual coil current is the sum of the two branch currents of the inductor L and the capacitor C_L, the coil current $i_{\text{coil}}(t)$ is [17]

$$\frac{d^2 i_{\text{coil}}(t)}{dt^2} + \frac{(R_L RC_L + L)}{RLC_L}\frac{di_{\text{coil}}(t)}{dt} + \frac{(R + R_L)}{RLC_L} i_{\text{coil}}(t) = 0 \quad t_3 < t < t_4 \tag{1}$$

where $i_{\text{coil}}(t)$ is the current of the air-core coil, L is the inductance of the air-core coil, C_L is the parasitic capacitance of the air-core coil, R_L is the internal resistance of the air-core coil, and R is the damping resistance.

In order to avoid any overshoot in the air-core coil current, the characteristic equation derived from (1) must possess either two real roots, which may be equal or unequal, as follows:

$$\left(\frac{R_L RC_L + L}{RLC_L}\right)^2 - 4\frac{(R + R_L)}{RLC_L} \geq 0. \tag{2}$$

Considering that usually $R_L \ll 2(L/C_L)^{1/2}$, (2) can be simplified as follows:

$$R \leq \frac{1}{2}\sqrt{\frac{L}{C_L}}. \tag{3}$$

Thus, if the damping resistance R satisfies the condition given in (3), the air-core coil current $i_{\text{coil}}(t)$ has no overshoot during the period t_3–t_4. However, it should be noted that the resistance value of R should not be set to the minimum possible value. According to (1), the damping factor δ of the air-core coil current can be expressed as [19]

$$\delta = \frac{R_L RC_L + L}{2RLC_L}. \tag{4}$$

According to (4), it can be inferred that a smaller value of resistance R leads to a larger attenuation coefficient δ and an extended turn-off time for the air-core coil current. If the diode voltage drop is ignored, the current value $i_{\text{coil}}(t)$ of the air-core coil at time t_3 can be expressed as follows:

$$i_{\text{coil}}(t_3) = \frac{U_0}{R} \tag{5}$$

where U_0 represents the clamping voltage of the capacitor C_0.

Formula (5) suggests that for a constant clamping voltage U0, a smaller resistance R leads to a higher initial value of the term TC, which in turn increases the decay time of TC. At the same time, this also leads to a rise in the non-linear error of the falling edge and causes energy loss in the circuit. Thus, based on (3)–(5), it can be deduced that the optimal value for the damping resistance is

$$R_{\text{opt}} = \frac{1}{2}\sqrt{\frac{L}{C_L}}. \tag{6}$$

However, during the practical implementation, even after adopting the optimal damping resistance value R_{opt}, the air-core coil current $i_{\text{coil}}(t)$ may still exhibit overshoot due to the presence of parasitic capacitance in the switching devices.

C. Circuit Model of Switching Devices

Due to their structure and package, commonly used high-power switching devices such as IGBT, GTR, etc., usually possess certain parasitic parameters that can adversely affect their switching performance, energy efficiency, and transient behavior. For instance, in the case of the IGBT, its circuit model [20] including parasitic parameters is shown in Fig. 5. Where, C_{ge}, C_{gc}, and C_{ce} denote the capacitances between the gate-emitter, gate-collector, and collector-emitter of the IGBT, respectively. Similarly, L_c and L_e are the parasitic inductances of the drain and source, R_g represents the gate parasitic resistance, and D_1 represents the parasitic diode of the IGBT.

The values of parasitic parameters may vary due to different structures, power, materials, and processes [20]. In order

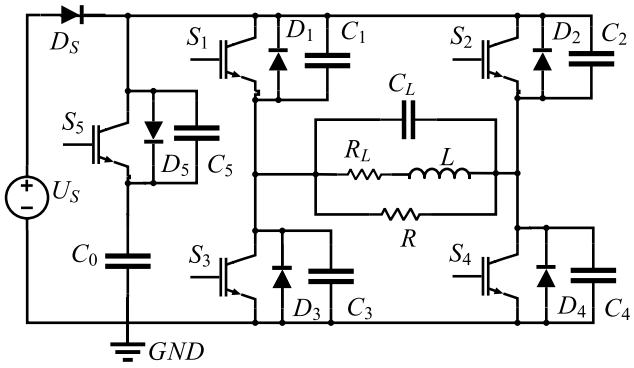

Fig. 6. Active clamping circuit with parasitic capacitance.

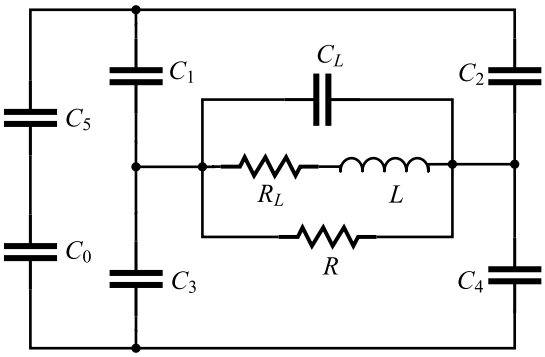

Fig. 7. Equivalent circuit during t_3–t_4.

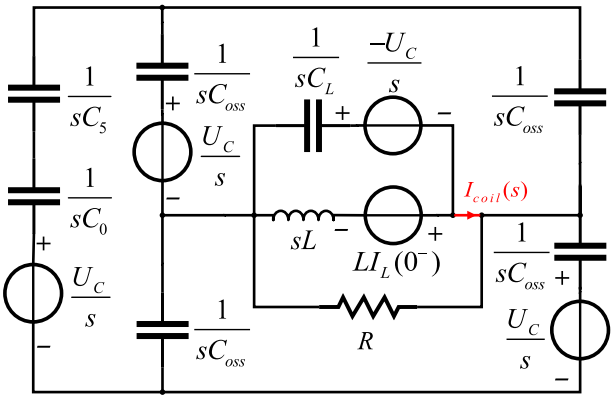

Fig. 8. Equivalent complex frequency domain model during t_3–t_4.

to satisfy parameters such as voltage, current, and heat dissipation, high-power devices usually have a large volume, which typically results in an increase in parasitic capacitance. Therefore, when using high-power devices, it is essential to account for the potential impact of parasitic capacitance, particularly during the analysis of transient processes.

Since all switches are turned off during t_3–t_4, the primary parameter that affects the TC is the output capacitance (C_{oss}) of the switch, which is typically measured with the gate and source short-circuited. So, the output capacitance can be expressed as [21]

$$C_{oss} = C_{gd} + C_{ds}. \tag{7}$$

In addition, it is worth noting that the values of these parasitic capacitances are not fixed and are significantly influenced by the voltage across the gate and source (V_{DS}). The parasitic capacitance values corresponding to different V_{DS} levels can typically be found in the device manual.

D. Active Clamping Circuit With Parasitic Capacitance

By combining the active clamping circuit shown in Fig. 2 with the parasitic parameter model of IGBT in Fig. 5, an active clamping circuit with the parasitic capacitance of the switching devices is proposed in Fig. 6. Following the turn-off of the switching device, only the capacitance between the drain and source, known as the output capacitance C_{oss}, affects the circuit. Accordingly, in Fig. 6, C_1 through C_5 represent the output capacitance of the switch S_1 through S_5, respectively. The control signals in Fig. 3 remain applicable to this circuit. The operation of the inverter circuit during the period 0-t_3 is similar to that of the circuit in Fig. 2.

During t_3–t_4, the switches S_1, S_2, S_3, S_4, and S_5 are all turned off, the circuit in Fig. 6 can be simplified to the circuit shown in Fig. 7.

The solution of the circuit model in Fig. 7 is complicated. Therefore, based on the state of the circuit at time t_3 and the actual situation, the following assumptions are made:

1) According to (2) and (3), the internal resistance R_L of the coil has a negligible effect on the circuit after time t_3, so R_L is ignored.
2) The resistance of the switches and diodes during conduction is neglected.
3) The capacitance of the clamping capacitor C0 is sufficiently large, and therefore, any voltage change across it can be disregarded.
4) It is assumed that switches S_1, S_2, S_3, and S_4 are typically of the same type, so, any difference between the capacitances C_1, C_2, C_3, and C_4 is ignored, that is

$$C_1 = C_2 = C_3 = C_4 = C_{oss} \tag{8}$$

where C_{oss} represents the output capacitance of the switch devices.

The initial state of each energy storage element can be expressed based on the circuit's operational state before time t_3

$$\begin{cases} U_{C_0}(t_{3-}) = U_{C_1}(t_{3-}) = U_{C_4}(t_{3-}) = -U_{C_L}(t_{3-}) = U_C \\ U_{C_2}(t_{3-}) = U_{C_3}(t_{3-}) = U_{C_5}(t_{3-}) = 0 \\ I_L(t_{3-}) = I_{\text{coil}}(t_{3-}) = U_C/R \end{cases} \tag{9}$$

where $U_{C_X}(t_{3-})$ represents the initial voltage of capacitor C_x ($x = 0, 1, \ldots, 5,$ or L) at time t_3, U_C is the clamp voltage, and $I_L(t_{3-})$ represents the initial current of the inductance L at time t_3, and $I_{\text{coil}}(t_{3-})$ represents the initial current of the air-core coil at time t_3.

Based on (8) and (9), the circuit depicted in Fig. 7 can be converted into a complex frequency domain model, as shown in Fig. 8.

Therefore, the TC during t_3–t_4 can be expressed as follows:

$$I_{\text{coil}}(s) = \frac{U_C}{R} \frac{s + \frac{L - C_{oss}R^2}{(C_{oss}+C_L)RL}}{(s+\alpha)^2 + \omega_d^2} \tag{10}$$

where

$$\alpha = \frac{1}{2(C_{oss} + C_L)R}$$
$$\omega_0 = \frac{1}{\sqrt{(C_{oss} + C_L)L}}$$
$$\omega_d = \sqrt{\omega_0^2 - \alpha^2}$$

when $\omega_0 \leq \alpha$, the current has no overshoot. Then R satisfies

$$R \leq \frac{1}{2}\sqrt{\frac{L}{C_{oss} + C_L}}. \tag{11}$$

For the same reason as (6), the optimal damping resistance can be determined as follows:

$$R_{\text{opt}} = \frac{1}{2}\sqrt{\frac{L}{C_{oss} + C_L}}. \tag{12}$$

Comparing (12) with (6), it can be found that the output capacitance of the switching devices reduces the optimal damping resistance R. This results in an increase in the initial value $i_{\text{coil}}(t_{3-})$ of the TC, a longer turn-off time of the pulse current, and an increase in the nonlinear error.

By comparing (12) with (6), it can be observed that the output capacitance of the switching devices decreases the optimal damping resistance R. As a result, the initial value $i_{\text{coil}}(t_{3-})$ of the TC increases, the turn-off time of the pulse current becomes longer, and the nonlinear error increases.

E. Circuit Model Simulation

Take circuit parameters $L = 1$ mH, $C_L = 1$ nF, $C_{oss} = 1$ nF, $U_C = 1000$ V, according to the circuit shown in Fig. 6, and build a circuit in Simulink for simulation. The damping resistance calculated by (6) is 500 Ω, and calculated by (12) is 353 Ω. The turn-off current waveform of different resistance is shown in Fig. 9.

Utilizing circuit parameters $L = 1$ mH, $C_L = 1$ nF, $C_{oss} = 1$ nF, and $U_C = 1000$ V, a simulation is constructed in Simulink, based on the circuit depicted in Fig. 6. The damping resistance, as computed by (6), amounts to 500 Ω, whereas the resistance computed by (12) is 353 Ω.

In Fig. 9, the simulation and experimental current waveform of the TC demonstrates that even when the critical damping condition of the coil is satisfied at $R = 500$ Ω, the TC waveform exhibits an overshoot. Taking into account the output capacitance of the switches at $R = 353$ Ω, the TC waveform shows no overshoot, thereby confirming that the critical damping resistance of the active clamping circuit is determined by both the coil's parasitic capacitance (C_L) and the switches' output capacitance (C_{oss}).

III. Optimization Control Method of TC

A. Process of the Clamping Circuit

The voltage across the inductor is proportional to the rate of change of its current; thus, we will analyze the process of inductor voltage change. Initially, before switches S_1 and S_4 turn off at time t_2, the current in inductor L attains a steady state, and the inductor voltage ($u_L(t)$) equals the power supply

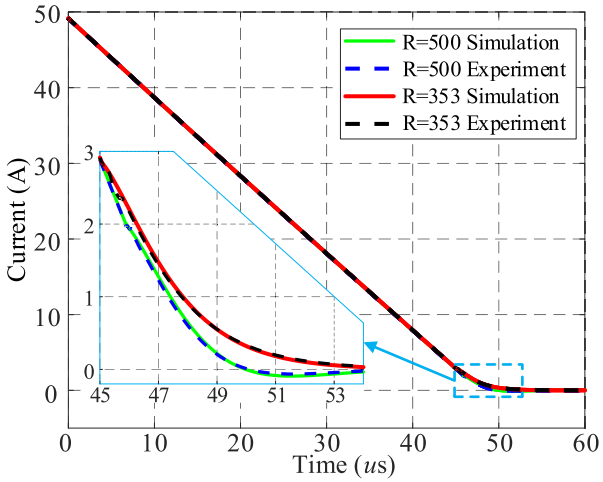

Fig. 9. Simulation and experimental current waveform of different damping resistance.

voltage U_s. After time t_2, when S_1 and S_4 are switched off, the inductor L charges the capacitor C_L. Due to the small capacitance of C_L, the voltage of the inductor $u_L(t)$ rapidly declines from U_s to $-U_C$. When $u_L(t)$ falls below $-U_C$, meaning $|u_L(t)| > |U_C|$, diodes D_2, D_5, and D_3 begin conducting. The inductor L charges the clamping capacitor C_0 through the D_2, D_5, and D_3 diode paths. As the capacitance of C_0 is sufficiently large, the inductor voltage $u_L(t)$ can be regarded as stable. This process persists until time t3. Beyond time t_3, the inductor current, $i_L(t)$, becomes less than U_C/R. At this point, $|u_L(t)| < |U_C|$, causing diodes D_2, D_5, and D_3 to turn off, and $u_L(t)$ gradually decreases along with the diminishing $i_L(t)$ until both $u_L(t)$ and $i_L(t)$ reach zero at time t_4.

After the time t_3, owing to the unidirectional conduction properties of diodes D_2, D_5, and D_3, the clamping capacitor C_0 is unable to provide power to the coil. Therefore, by turning on switches S_2, S_5, and S_3, the inductor voltage, $u_L(t)$, can be maintained stable at the clamping voltage U_C. In this way, the current can keep decreasing linearly after the time t_3.

B. Realization of the Optimization Method

For the circuit shown in Fig. 6, based on the analysis presented in Section III-A, we designed the control signal displayed in Fig. 10 to minimize the influence of the TC on the current.

As shown in Fig. 8, the operating mode of the circuit remains unchanged before time t_3. At time t_3, S_2, S_5, and S_3 are turned on, allowing the capacitor C_0 to maintain the voltage of the inductor $u_L(t)$ at U_c. As a result, the current $i_L(t)$ can continue to decrease linearly. When t_{off} is reached, S_2, S_5, and S_3 are turned off, and the current continues to decrease through the damping resistor R.

The energy flow during the period t_2–t_3 differs from that during the period t_3–t_{off}. The inductor voltage remains at $-U_C$ throughout t_2–t_{off}, resulting in zero parasitic capacitor current and a damping resistor current is $I_R = -U_C/R$. However, during t_2–t_3, $i_L(t) > I_R$, causing a portion of the inductor

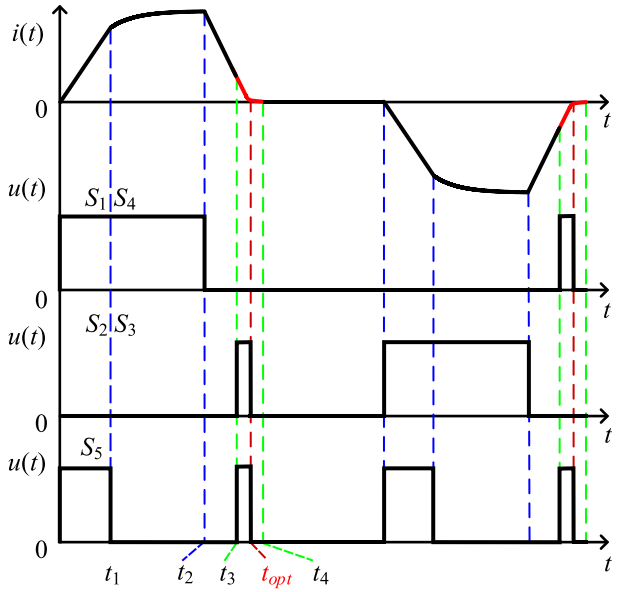

Fig. 10. Control signal for the optimization method.

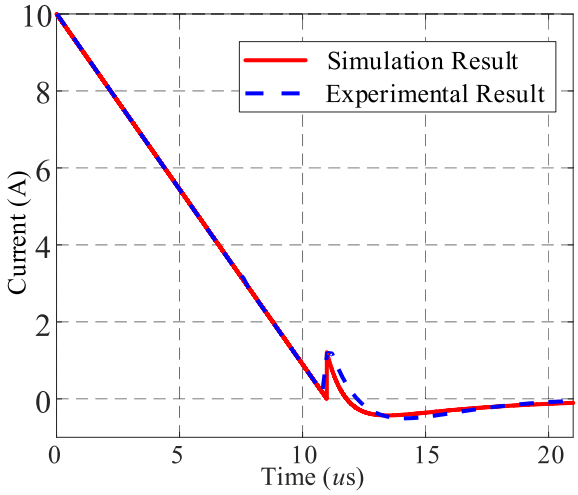

Fig. 11. Inductor current waveform when $i_L(t_{\text{off}}) = 0$.

current to flow through the damping resistor R and another portion to flow through the clamping capacitor C_0. Therefore, the energy of the inductor flows to both the capacitor C_0 and the resistor R. During t_3–t_{off}, $i_L(t) < I_R$, and all of the inductor current flows through the resistor R. At this time, the capacitor C_0 provides a portion of the current to R, causing both the inductor energy and the clamping capacitor energy to flow to the resistor R.

By controlling the turn-off time t_{off}, the initial value of the TC $i_L(t_{\text{off}})$ can be reduced to zero. However, after time t_{off}, the voltage of capacitors C_L C_1 and C_4 remain at U_C, causing them to discharge through the inductor L and resistor R. This discharge causes the inductor current $i_L(t)$ to exhibit overshoot, the simulation, and experiment current waveform is shown in Fig. 11.

Based on Fig. 11, it is apparent that the overshoot amplifies the nonlinear error of the falling edge current. Consequently, an optimal solution exists during the period t_3–t_4 for the turn-off time (t_{off}) of switches S_2, S_5, and S_3, such that the falling edge current $i_L(t)$ can attain the least nonlinear error. Let t_{opt} be the turn-off time of the switches when the current reaches the least nonlinear error, and I_{opt} be the initial value of the TC at that time. Then, we can express this as follows:

$$I_{\text{opt}} = i_{\text{coil}}(t_{\text{opt}}). \tag{13}$$

C. Solution of the t_{opt} and I_{opt}

To minimize the nonlinear error at the falling edge of the pulse current, it is essential to first determine the turn-on time (t_{on}) and turn-off time (t_{off}) for switches S_2, S_5, and S_3.

When the switches are turned on precisely at time t_3, there is a period where diodes D_2, D_5, and D_3 and switches S_2, S_5, and S_3 are off due to the time required for switching. During this period, the falling edge current cannot continue to decrease linearly. Therefore, the optimal conduction time should be less than time t_3 to ensure the linear decay of the falling edge current. Additionally, since $|u_L(t)| > |U_C|$ during the period t_2–t_3, the conduction of S_2, S_5, and S_3 before time t_3 does not affect the operating state of the circuit. Obviously, the minimum value of the conduction time cannot be less than t_2. Considering the dead time required for switches S_1 and S_4 to turn off, the optimal conduction time t_{on} should satisfy

$$t_2 + t_{S\_DT} \le t_{\text{on}} \le t_3 - t_{S\_\text{ON}} \tag{14}$$

where t_{on} represents the conduction time of switches S_2, S_5, and S_3. t_{S_DT} represents the minimum dead time required for the switch to turn off. t_{S_ON} represents the minimum time required for the switch to turn on.

Next, we will analyze the turn-off time t_{off} of switches S_2, S_5, and S_3. Assume that the optimal turn-off time is t_{opt}. If we ignore the change in clamp voltage U_C, the inductor current $i_L(t)$ during t_2–t_{opt} decays linearly, and therefore, $i_L(t)$ satisfies

$$i_L(t) = -\frac{U_C}{L}(t_{\text{off}} - t_2) + I_0, t_2 \le t_{\text{off}} < t_{\text{opt}} \tag{15}$$

where I_0 represents the peak value of the pulse current.

After time t_{opt}, all switches are turned off and all diodes are non-conducting, and the operating state of the circuit is still the same as the circuit model shown in Fig. 5, but with a different initial value of the energy storage element. Based on the operating state of the circuit before t_{opt}, the initial value of the energy storage element can be expressed as follows:

$$\begin{cases} U_{C_0}(t_{\text{opt}-}) = U_{C_1}(t_{\text{opt}-}) = U_{C_4}(t_{\text{opt}-}) = -U_{C_L}(t_{\text{opt}-}) = U_C \\ U_{C_2}(t_{\text{opt}-}) = U_{C_3}(t_{\text{opt}-}) = U_{C_5}(t_{\text{opt}-}) = 0 \\ I_L(t_{\text{opt}-}) = I_{\text{opt}}. \end{cases} \tag{16}$$

According to the equivalent complex-frequency-domain model in Fig. 8 and (16), the TC during t_{opt}–t_4 can be expressed as follows:

$$I_{\text{coil}}(s) = \frac{(RI_{\text{opt}}C_{oss} + U_C C_L)Ls + I_{\text{opt}}L - RU_C C_{oss}}{R(C_{oss} + C_L)Ls^2 + Ls + R}. \tag{17}$$

TABLE I
MAIN PARAMETERS OF THE NUMERICAL CALCULATION

Parameters	Value
Coil inductance (L)	1.1 mH
Coil capacitance (C_L)	0.8 nF
Transmitting current (I_0)	20 A
Clamping voltage (U_C)	1000 V
Output capacitance (C_{oss})	2.5 nF

Taking the inverse Laplace transform of (17), the TC during t_{opt}-t_4 is

$$i_{\text{coil}}(t) = 2\alpha S_1 e^{-\alpha t}\left[\cos\omega_d t + \sin\omega_d t\left(\frac{LI_{\text{opt}} - C_{oss}RU_C}{L\omega_d S_1} - \frac{\alpha}{\omega_d}\right)\right] \tag{18}$$

where

$$\alpha = \frac{1}{2(C_{oss}+C_L)R}$$
$$\omega_0 = \frac{1}{\sqrt{(C_{oss}+C_L)L}}$$
$$\omega_d = \sqrt{\omega_0^2 - \alpha^2}$$
$$S_1 = C_L U_C + RC_{oss}I_{\text{opt}}.$$

Equations (15) and (18) determine the falling edge waveform of the pulse current, and the nonlinear error can be expressed as [11]

$$\gamma = \frac{|\Delta I_{\max}|}{I_0} \times 100\% \tag{19}$$

where γ represents the nonlinear error of the pulse current and $\Delta I_{\max}$ represents the maximum error between the falling edge current and its best-fitting straight line.

Based on (15), (18), and (19), we can determine I_{opt} using a numerical calculation method. The relevant parameters are shown in Table I.

According to the parameters in Table I, we can calculate $R = 288.7\ \Omega$ using (12). The falling edge current waveform during the t_2–t_4 interval can be computed using (15) and (18), while the nonlinear error is determined by (19). Using this data, we obtain the relationship between I_{opt} and the nonlinear error, as illustrated in Fig. 12.

Fig. 12 illustrates that the optimized falling edge current achieves the smallest nonlinear error of 4.18% with $I_{\text{opt}} = 1.25$ A, whereas the unoptimized case yields a nonlinear error of 11.31% with $I_{\text{opt}} = U_C/R = 3.46$ A. Consequently, the optimization control method reduces the nonlinear error by 7.13% for the falling edge current. The falling edge current waveforms before and after optimization are depicted in Fig. 13.

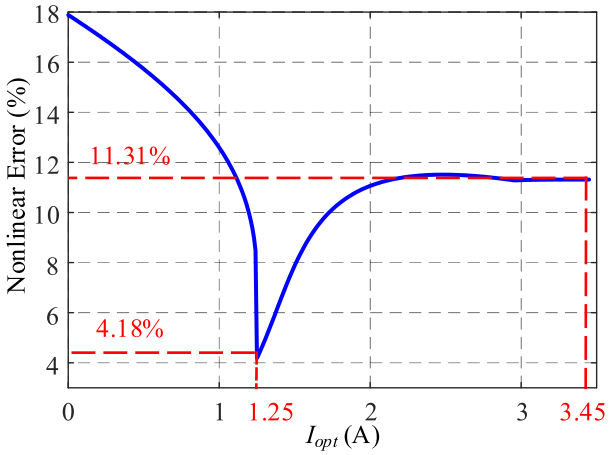

Fig. 12. Nonlinear error of different I_{opt}.

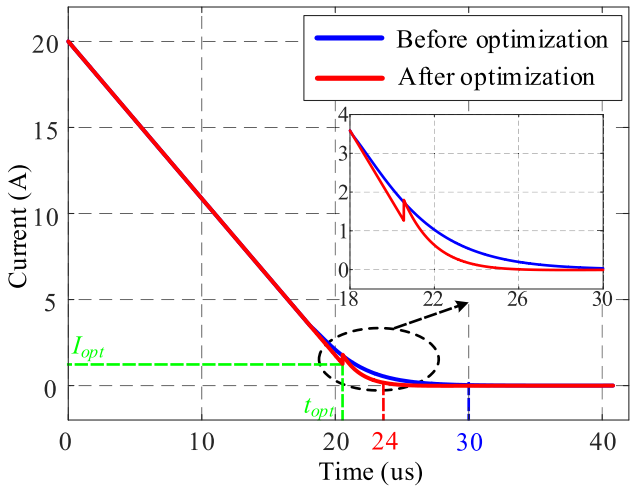

Fig. 13. Falling edge current waveform before and after optimization.

In Fig. 13, the abrupt rise in the current waveform at time t_{opt} is attributable to the energy storage of the coil capacitance and the switching device capacitance. The turn-off time of the pulse current, before and after correction, decreases from 30 to 24 μs, representing a 20% reduction. Numerical calculations demonstrate that the optimization method can effectively diminish the non-linear error and curtail the turn-off time of the pulse current.

IV. EXPERIMENTAL RESULTS

To validate the impact of the parasitic capacitance circuit model depicted in Fig. 4 and the optimization method proposed in Section III-B, we construct the experimental circuit illustrated in Fig. 14(a), and Fig. 14(b) is the circuit diagram of the experimental circuit. The circuit comprises three components: the control board, IGBT full-bridge circuit, and the clamping circuit. The model of the five IGBT switches is Infineon FF150R17KE4, the diode model is DH2 × 61.18A, the current probe model is Agilent 1146A, and the oscilloscope model is Tektronix MDO3012.

The relevant parameters of the experimental circuit and the transmitting coil are provided in Table II. The output

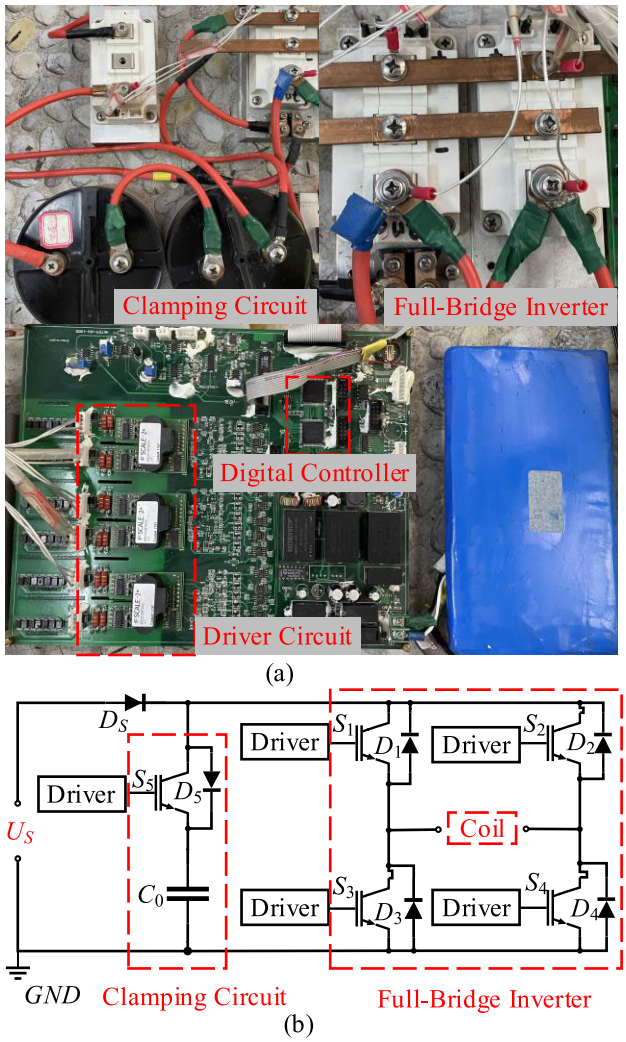

Fig. 14. Experimental circuit for the parasitic capacitance circuit model and the optimization control method. (a) Test setup. (b) Circuit diagram.

TABLE II
MAIN PARAMETERS OF THE EXPERIMENTAL CIRCUIT

Parameters	Value
Coil inductance (L)	1.65 mH
Coil capacitance (C_L)	2.8 nF
Transmitting current (I_0)	20 A
Clamping voltage (U_C)	950 V
Output capacitance (C_{oss})	1.7 nF

capacitance C_{oss} is determined based on the datasheet when the drain–source voltage is 950 V.

According to the coil parameters in Table II, the damping resistance of the coil is calculated to be 384 Ω using (6). However, the value determined by (12) is 303 Ω. To validate the circuit model in Fig. 6, the zero-input response of the transmitting coil was measured under the following three scenarios: 1) the damping resistance is 384 Ω, and the transmitting coil is not connected to the experimental circuit, as shown in Fig. 15(a); 2) damping resistance is 384 Ω, and the transmitting coil is connected to the experimental circuit, as shown in Fig. 15(b); and 3) damping resistance is 303 Ω, the transmitting coil is connected to the experimental circuit, as shown in Fig. 15(c).

Fig. 15(a) and (b) demonstrate that the damping resistance R remains at 384 Ω; however, connecting to the experimental circuit leads to overshoot in the zero-input response. To solve this issue, the resistance was adjusted by considering the output capacitance C_{oss} of the switches. The value of the damping resistor R was then adjusted to 303 Ω. As illustrated in Fig. 15(c), the measured zero-input response of the transmitting coil exhibits no overshoot at this adjusted resistance value. This suggests that the primary reason for the change in damping resistance is the output capacitance of the switches. It also implies that the circuit model presented in Fig. 6 is accurate and can correctly represent the change in TC after time t_3.

Employing the optimization control method and the parameters listed in Table I, we determined the optimal parameters to be $t_{\text{opt}} = 32.4\ \mu s$ and $I_{\text{opt}} = 1.13$ A. Fig. 16 displays the actual measurements of the current waveform both before and after the optimization process.

The graph in Fig. 16 demonstrates that the turn-off time of the pulse current is 46.2 μs before optimization and 35.2 μs after optimization, signifying a reduction of 23.8%. Moreover, the nonlinear error of the falling edge current, calculated using (19), is 10.5% before optimization and 5.0% after optimization. With the pole configuration method, the turn-off time is 48.5 us, and the non-linear error is 8.2%. According to the waveform in Fig. 16, it can be observed that the use of the pole configuration method and the damping resistor achieved similar performance. The pole configuration method allows the pulse current to drop to zero more quickly, but it produces overshoot, and the time it takes for the overshooting current to decay to zero is also relatively long. Meanwhile, after using the optimization control method, both the turn-off time and non-linear error are less than the results when using the pole configuration method and the damping resistor.

Fig. 17 presents the detection results of the unexploded ordnance (UXO) model using the TEM method. The TEM field detection instrument adopts the FCTEM60-1 towed and high-resolution TEM system independently developed by the laboratory. We adopted the towed measurement method to improve the lateral resolution of the detection results. And we categorized the data based on RTK coordinates. The field collection parameters are: coil diameter is 0.9 m, the transmitting frequency is 16 Hz, the towed speed is 2 m/s, the sampling rate is 1.25 M, and transmitting current is 60 A.

Specifically, Fig. 17(a) displays the target object of the experiment, which is a model of UXO with a diameter of 23 cm and a height of 90 cm. Fig. 17(b) displays the apparent resistivity profile without the optimization method, while Fig. 17(c) shows the apparent resistivity profile after applying the optimization method. It can be observed that due to the volume effect of TEM [22], the detection results

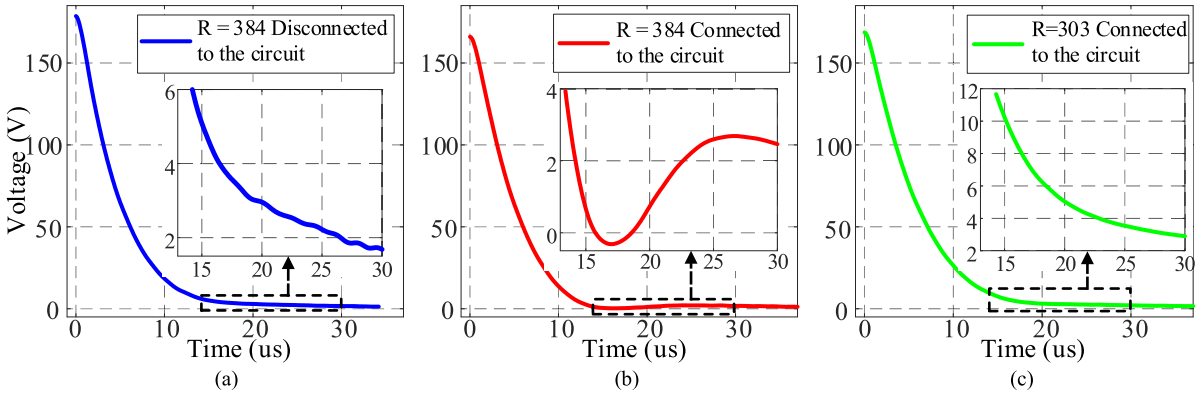

Fig. 15. Zero-input response of the transmitting coil. (a) $R = 384\ \Omega$ and disconnected to the circuit. (b) $R = 384\ \Omega$ and connected to the circuit. (c) $R = 303\ \Omega$ and connected to the circuit.

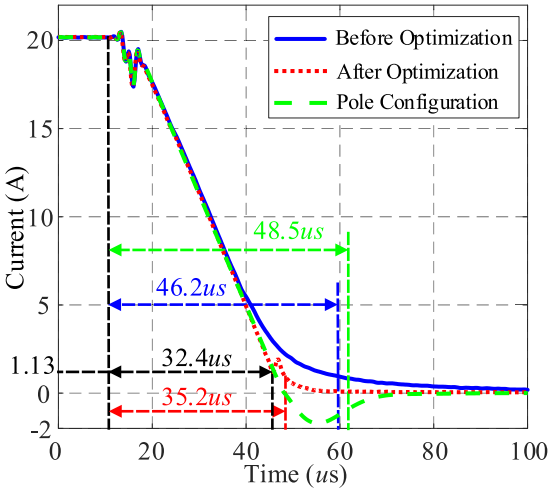

Fig. 16. Comparison of the performance between before optimization, after optimization, and the pole configuration method.

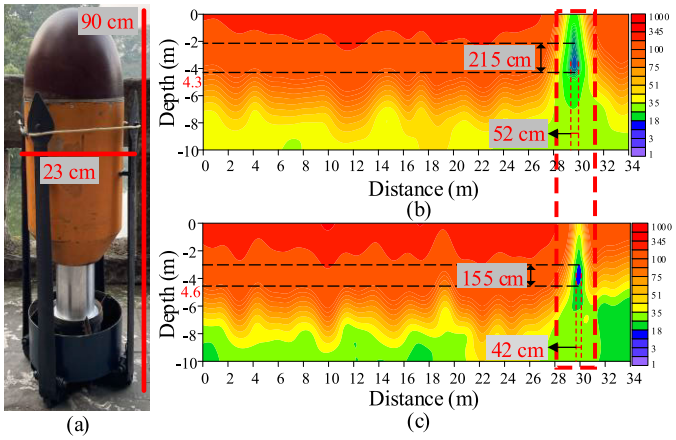

Fig. 17. Target object and resistivity distribution profile. (a) UXO. (b) Before optimization. (c) After optimization.

of diameter and height exhibit errors both before and after optimization. However, post-optimization, the detected results of the diameter are 42 cm and the height is 155 cm. This represents a reduction in error of 10 cm for diameter and 60 cm for height when juxtaposed against the unoptimized results. The detection depth was 4.3 m before optimization and 4.6 m after optimization. Relative to the true burial depth of 4.9 m, there is a 6% enhancement in detection accuracy following optimization. The detection results verify that the optimization method proposed in this article can enhance the shallow detection accuracy and resolution of the TEM system.

V. Conclusion

In conventional constant voltage clamping circuits, the presence of TC leads to an increase in the turn-off time and the nonlinear error of the pulse current. This article examines the causes of TC, proposes a circuit model that accounts for the IGBT switch's output capacitance, and studies the impact of output capacitance on TC. Moreover, an optimization control method based on the active clamping circuit is introduced to minimize the effect of TC on the nonlinear error and the turn-off time of the pulse current. The feasibility of this optimization method is validated through simulation. Optimal parameters are determined via theoretical analysis and numerical calculation methods. Subsequently, an experimental circuit is constructed to assess the impact of the optimal parameters. The experimental results indicate that the optimization reduces the nonlinear error by 5.5% and shortens the turn-off time by 23.8%. In the UXO detection experiment, the detection results obtained using the optimized circuit exhibit higher resolution.

It should be noted that the actual effectiveness of this optimization method is also influenced by the circuit parameters. Based on the circuit parameters presented in Table I, we analyzed the impact of different circuit parameters on the optimization effects. Fig. 18 illustrates the variations in the non-linear error and turn-off time with changes in total capacitance, coil inductance, transmitting current, and clamping voltage. The results before and after correction are juxtaposed for comparison.

In Fig. 18(a), as the total capacitance increases, the difference in non-linear error and turn-off time before and after optimization gradually enlarges. This indicates that with other parameters remaining constant, the larger the total capacitance, the more effective the proposed optimization method is.

In Fig. 18(b), as the coil inductance increases, the difference in non-linear error before and after optimization decreases, indicating that as the coil inductance grows, the optimization

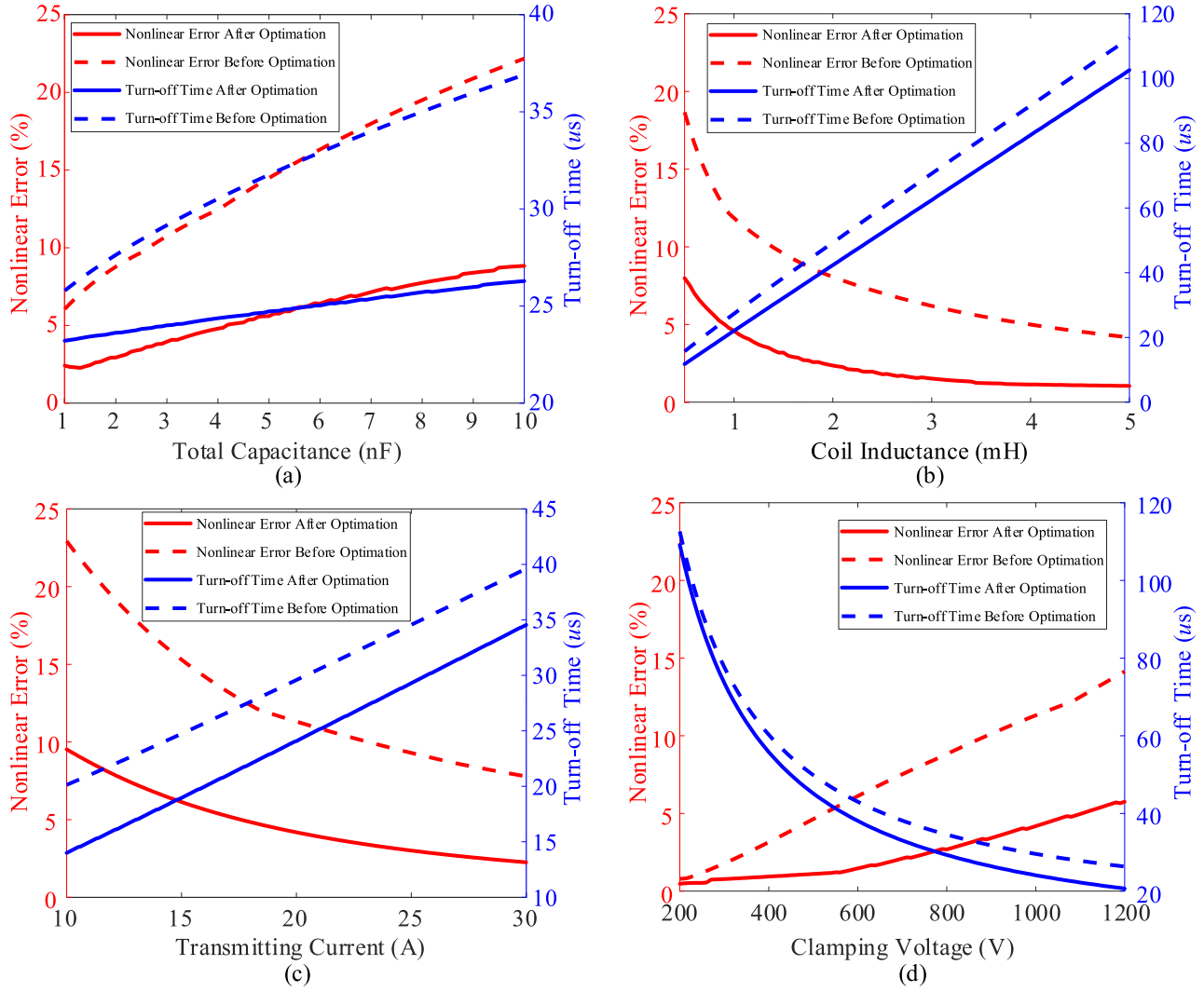

Fig. 18. Impact of different circuit parameters on optimization effects. (a) Total capacitance. (b) Coil inductance. (c) Transmitting current. (d) Clamping voltage.

effect gradually diminishes. However, the optimization effect on the turn-off time increases with the rise in inductance.

In Fig. 18(c), as the transmitting current increases, the difference in non-linear error before and after optimization gradually decreases, indicating that the optimization effect weakens as the transmitting current grows. This is because, when calculating the non-linear error, the maximum transmitting current is treated as the denominator. However, the optimization effect on the waveform during the TC period has not diminished. At the same time, the increase in transmitting current does not affect the optimization effect on the turn-off time.

In Fig. 18(d), as the clamping voltage increases, the difference in non-linear error and turn-off time before and after optimization gradually grows. This indicates that when other parameters remain unchanged, the higher the clamping voltage, the better the effect of the proposed optimization method.

In summary, the optimization control method proposed in this article performs better in scenarios with the larger total capacitance, the higher clamping voltage, the smaller coil inductance, and the lower transmitting current. This approach presents an efficient and easy-to-implement optimization method for TC, as it does not necessitate the addition of any power devices.

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