From the Measurement of C_{OSS}–V_{DS} Characteristic to the Estimation of the Channel Current in Medium Voltage SiC MOSFET Power Modules

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***Abstract*— This article presents a novel method for the dynamic measurement of C_{OSS}–V_{DS} characteristic of SiC MOSFET power modules based on the process of charging the output capacitance of the transistors. This technique has been used to determine the C_{OSS}–V_{DS} characteristics of medium voltage SiC MOSFET modules, which allows for the extraction of the capacitive current while switching off the transistor. Based on this measurement method, the influence of the turn-off gate voltage V_{GS-OFF} on the C_{OSS}–V_{DS} characteristics has been studied, exhibiting an impact on the output capacitance at low drain–source voltages. However, it is shown that the effect of V_{GS-OFF} on the capacitive current and power loss is limited in this area. Finally, the channel current and the capacitive current distribution within the drain current were determined based on the determined C_{OSS}–V_{DS} in the experimental test at various switched currents and switching speeds. According to the capacitive charge calculations for several cases, the method's accuracy is high enough to perform switching power loss estimations for medium voltage power modules to be employed in the design of the state-of-the-art power converters. Furthermore, the method is very simple, based on basic capacitance equations, and the required experimental setup is very similar to one used in double-pulse tests.**

***Index Terms*— Dynamic characterization, MOSFET, power electronics, silicon carbide, switching losses, zero-voltage switching.**

I. Introduction

MEDIUM voltage SiC MOSFETs are excellent candidates for high-power soft-switched power converters, where they can replace currently employed Si-based IGBTs. Operating in zero voltage switching (ZVS) conditions, such as in dc–dc or inductive power transfer (IPT) converters, these power semiconductors can achieve lower power losses, improving the overall efficiency of the system [1], [2], [3], [4]. Such systems usually operate at high switching frequencies, and a substantial part of the power losses occurring in semiconductor elements is losses generated during the switching-off process. Therefore, it is essential to correctly determine the switching losses to design the converter properly from an electrothermal perspective. Several publications, to mention only [5], [6], [7], [8], [9], and [10], have shown that the switch-off transition is quite complex and has not been fully examined yet. This is especially true for SiC MOSFETs, which switch at exceptional speeds, showcasing the issues that were omittable in the case of slow Si counterparts [5], [6]. For example, using SiC-based power devices with sufficient gate current may even lead to a situation with ultralow turn-off switching losses [7], and thus considering the gate driver is essential as well [8]. Moreover, apart from the commonly used power loss sources in the form of switching and conduction losses, additional losses such as residual loss [9] should also be taken into account. Finally, the effects of the measuring equipment have a substantial impact as well [10]. All in all, without deep analysis of the turn-off switching process, it can be concluded that the drain current includes the channel current, which causes conduction power losses in the transistor's channel, and the capacitive current, which is almost lossless [11]. Therefore, to correctly determine the switch-off power losses, it is necessary to distinguish these two components. This can be done by finding the capacitive current from the derivative of the drain–source voltage; for this, the C_{OSS}–V_{DS} characteristic of the power device must be employed [12]. However, this characteristic is not available for all power modules—this is the case of the power modules discussed in this work [13], [14], [15] or other power modules under development. Moreover, the characteristics provided by the manufacturer are usually measured only for gate–source voltage $V_{GS} = 0$, while gate-related capacitance is dependent on polarization, as has been proved both in TCAD simulations and experimentally [16], [17], [18].

The problem of characterization of MOSFET parameters [19], [20], including measuring C_{OSS}–V_{DS} characteristics, also for SiC power devices, was undertaken by many research teams [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26]. The key question is if the observations for single-chip modules will be the same as for multichip power modules.

There are classic methods using an impedance analyzer or an *LRC* bridge to determine the C_{OSS}–V_{DS} characteristics, but

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the main problem is the need for high-voltage polarization, as most of the equipment is not able to reach even 800 V, not to mention higher voltages required for testing medium voltage power modules. Hence, various circuit concepts have arisen to allow measurements at higher voltages [16], [17], [18], [21]; however, the complexity of such systems is high. Another testing approach is based on running one- or two-pulse tests and observing the corresponding waveforms to determine the charges and capacitances [22], [23], [24], [25]. It is also possible to use a similar method in transistors' continuous operation without load [26]. However, these methods also induce their complexities, such as the need for another active switch in parallel to the device under the test [22], which may induce additional error; or the requirement of precise calibration of the inductor to achieve the resonance with C_{OSS} capacitance [23]; or were focused on other transistor capacitances, e.g., C_{RSS} [24], [25].

Considering the special features of medium voltage SiC power modules, i.e., a large active surface and potentially a large output capacitance, the authors propose a very simple, dynamic method for the measurement of C_{OSS} capacitance based on a single-pulse test. It is based on monitoring the drain–source voltage and the current flowing through the power device. The method has been successfully validated, showing that it is possible to precisely determine the C_{OSS}–V_{DS} characteristic without much computational and experimental effort, based on basic capacitance equations and using a simple setup akin to the conventional double-pulse test bench. This method has also been employed to study the influence of the turn-off gate voltage V_{GS-OFF}, whose value affects the parasitic capacitances of the power device.

This article is organized as follows: after the introduction, the origins of the parasitic capacitances in a SiC MOSFET device are briefly described, and then, the proposed method for measuring the C_{OSS}–V_{DS} characteristic is presented. In Section III, this method is applied to a 1700-V/900-A SiC MOSFET power module to find suitable characteristics, also with nonzero gate polarization. Then, the studied devices are tested in single-pulse tests with an inductive load at different switched currents and switching speeds, with frequencies up to 25 kHz, and the capacitive current is estimated based on the determined C_{OSS}–V_{DS} characteristic. The work is concluded with a discussion of the results and a summary of the primary outcomes, successfully validating the proposed method.

This article is an extension of the proceedings article [12], but with additional theoretical insight, a more detailed description of the proposed method, as well as an expanded experimental study, also including the impact of different turn-off V_{GS} values.

II. Origins of the SiC MOSFET Output Capacitance

A. Single-Cell MOSFET Capacitances

The origins of parasitic capacitances of SiC vertical drift region-type double-diffusion MOSFET (VDMOS) are directly associated with the internal structure of the power semiconductor device. Depending on the gate-to-source voltage V_{GS} and if it is below or above the threshold voltage V_{TH}, two different

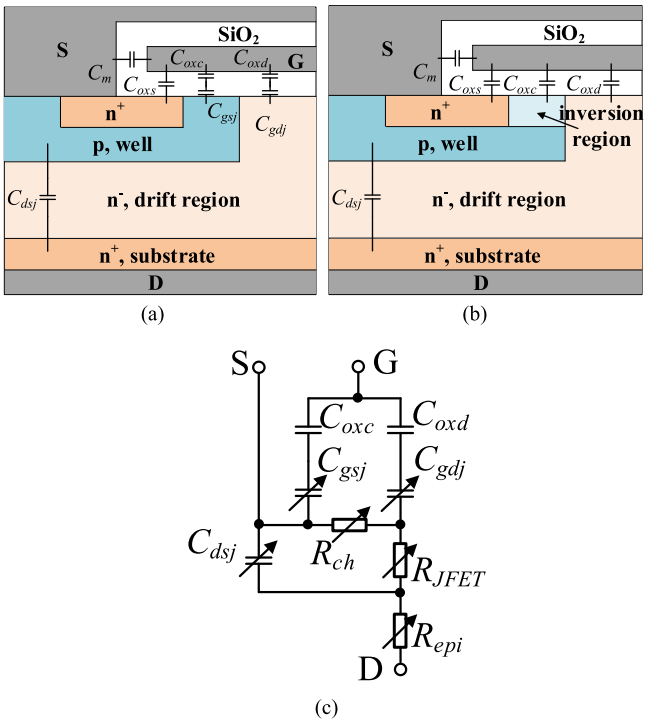

Fig. 1. Parasitic capacitances of a half-cell MOSFET structure-cross section with (a) closed ($V_{GS} < V_{TH}$) and (b) open ($V_{GS} > V_{TH}$) channel. (c) Equivalent electrical circuit of the transistor, including resistances for the current flow path [29].

situations can be distinguished. These situations are depicted in the cross-sectional illustrations of a MOSFET cell when the device is closed with $V_{GS} < V_{TH}$ in Fig. 1(a) and when the device is open ($V_{GS} > V_{TH}$) in Fig. 1(b) [19], [27], [28], [29], [30]. Furthermore, an equivalent electrical circuit of the transistor, also including the most relevant ON-state resistances (channel resistance R_{ch}, JFET region resistance R_{JFET}, and epitaxial layer resistance R_{epi}) for the current flow path, is shown in Fig. 1(c). Regarding the parasitic capacitances, the main difference between both situations is that while gate–source and gate–drain capacitances are separated by a depleted region in the p-well when the device is closed ($V_{GS} < V_{TH}$), they are connected through the channel resistance when the device is open [29].

Generally, the terminal parasitic capacitances between the following MOSFET electrodes are distinguished: gate-to-source capacitance C_{GS}, gate-to-drain capacitance C_{GD}, and drain-to-source capacitance C_{DS}. They are crucial in affecting the device switching behavior and are typically classified into three equivalent capacitances used for performance evaluation of the MOSFETs: the input capacitance seen from the gate ($C_{ISS} = C_{GS} + C_{GD}$), the reverse transfer capacitance ($C_{RSS} = C_{GD}$), and the main interest of this article, the output capacitance seen from the drain ($C_{OSS} = C_{DS} + C_{GD}$). The nature of the terminal capacitances is an effect of the device structure, including the semiconductor and oxide junctions and interfaces, and is highly dependent on V_{GS} and V_{DS} transistor voltages.

When a situation with a closed MOSFET channel is considered [Fig. 1(a)], the C_{GS} capacitance is comprised of the capacitance between the gate (G) and source (S) electrodes

within the oxide (C_m) and capacitances between the gate and: n^+ region (C_{oxs}), p^+ region (C_{oxc}), and p^+ depletion region (C_{gsj}). The capacitances between the gate and the drain (D) within the oxide C_{oxd} and the capacitance of the depletion region C_{gdj} are parts of the C_{GD} capacitance. Finally, the C_{dsj} capacitance across the depletion region below the p base is the only component of C_{DS}. When the gate polarization changes and $V_{GS} > V_{TH}$, which is the case during the turn-on process, the channel is established, and R_{CH} decreases [Fig. 1(b)]. Thus, the depletion capacitance C_{gsj} basically disappears, and capacitance C_{gdj} becomes negligible, while the oxide capacitances (C_m, C_{oxs}, C_{oxc}, and C_{oxd}) and the C_{dsj} capacitance remain, in practice, unchanged. Furthermore, when the device is open ($V_{GS} > V_{TH}$), the channel resistance is low, and therefore, $C_{oxc}+C_{gsj}$ is in parallel with $C_{oxd}+C_{gdj}$; hence, C_{GD} becomes part of C_{GS}.

On the other hand, when the device is turning-off, the increase of V_{DS} shifts the charge on the p-/n-junction, changing the C_{dsj} capacitance. Moreover, a similar effect is observed in the JFET region and C_{gdj}—both capacitances decrease with the drain potential.

Moreover, additional effects, such as drain-induced barrier lowering (DIBL) [31], are also observed, but they have a limited impact on the capacitance characteristics. Recently, the charge trap issues have also been discussed [32]; however, its influence is rather seen in the C_{GS} capacitance without affecting the C_{OSS} analyzed in this article.

B. MOSFET Capacitances in Power Modules

When high-power systems are considered, also in the medium voltage range, power module MOSFET packaging comes into play. Since these devices are made for high-power applications, current ratings of hundreds of amps are expected, requiring the use of multichip structures. In such modules, several MOSFET dies are connected in parallel and act as a single transistor, as shown in a simplified schematic of the power module in Fig. 2. This way, the power density achievable with these power modules can be improved since more power can be managed in a lower volume.

When multichip SiC power modules are considered, the characterization of the parasitic capacitances becomes even more complex as additional parasitics are present [33]. The complexity of employing SiC-based power modules is alleviated even more by the fact that, in most cases, the manufacturer does not share how many dies are used and what are the individual chips employed in the module, and generally, the datasheets lack of information regarding the parasitic capacitance characterization. Consequently, determining the switching performance of the SiC power modules based on capacitance characteristics is not a simple task and has not been studied widely before.

Furthermore, each MOSFET chip in a power module is characterized by different values of, among others, internal gate resistances and capacitances. Thus, in practice, the switching process for each chip occurs individually and can vary between the paralleled wafers. However, from the power electronics designer's perspective, the power module is still a single device and a characterization method based on establishing an equivalent characteristic seen from the power device terminals is required. To this end, such a technique is proposed in Section III of this article.

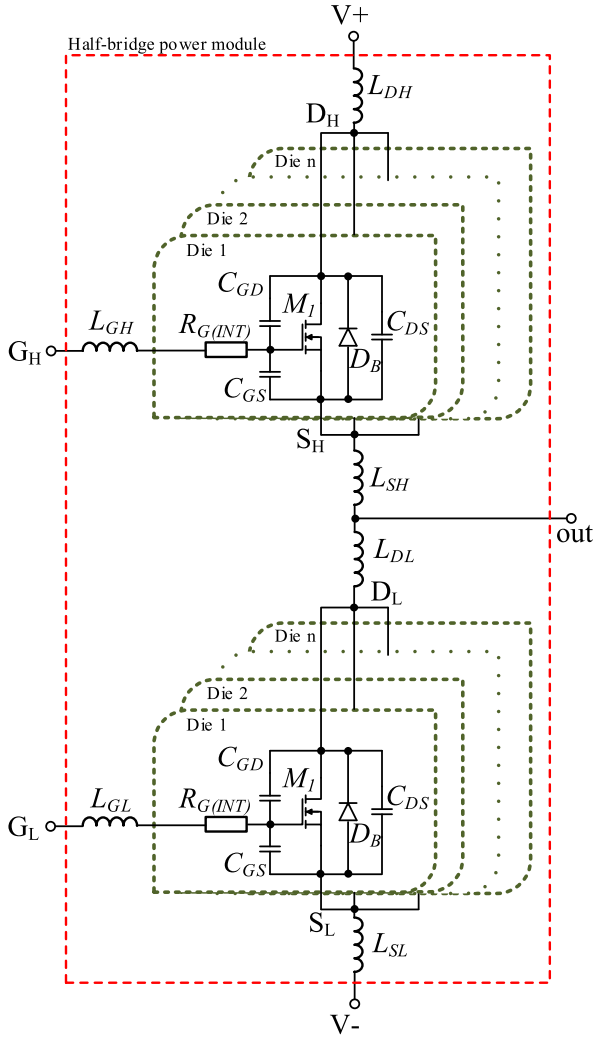

Fig. 2. Simplified equivalent circuit with parasitic capacitances of a multichip SiC MOSFET half-bridge power module.

III. C_{OSS}–V_{DS} Test Method

A. C_{OSS}–V_{DS} Test Method for the Off-State Device

The method proposed by Rabkowski et al. [12] uses a half-bridge power module (scheme in Fig. 3, photograph of the laboratory setup in Fig. 4) similar to [26], but only a single pulse test is performed. The low-side transistor of the half-bridge is the device under test (DUT) and is permanently in the OFF-state, with $V_{GS} < V_{TH}$, while the upper transistor plays the role of the control switch, applying a positive voltage to its gate V_{ctrl} in order to establish a constant voltage V_{DC} to V_{DS} of the DUT. In consequence, the output capacitance of the lower transistor is charged via the upper transistor. There is no resistor in series to limit the current slope, but an increased gate resistor R_G is applied to control the switching speed and peak of the charging current i_{Coss}.

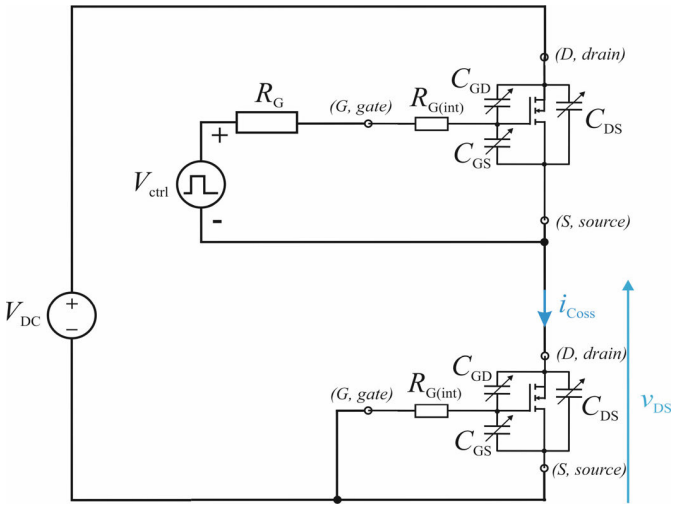

Fig. 3. Half-bridge test setup for the C_{OSS}–V_{DS} characteristic measurements of the SiC power module.

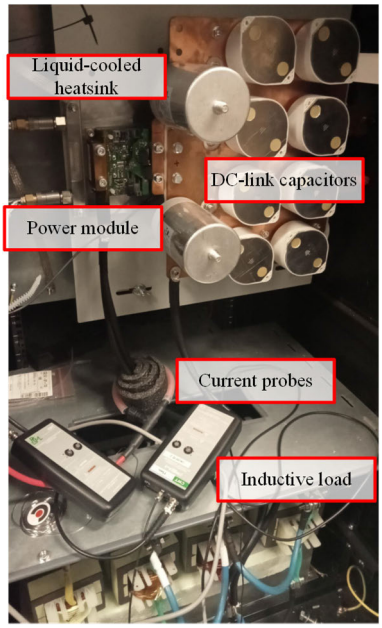

Fig. 4. Photograph of the laboratory setup with the SiC power module used for the experiments.

An example of the waveforms obtained for a 1.7-kV/900-A SiC MOSFET power module, for which C_{OSS}–V_{DS} characteristic is not available in its datasheet, is presented in Fig. 4 for a test performed at 1200-V dc voltage. At the beginning of the process, V_{DS} is low, and the capacitance shows maximum values; therefore, the charging current rises fast and reaches peak value when the V_{DS} slope becomes linear. Then, while the voltage increases, the output capacitance drops, and the charging current is reduced. Note that a similar current also discharges the capacitances of the upper transistor. At the end of the test, the V_{DS} slope becomes nonlinear again, most likely, due to increased capacitance of the upper transistor. All in all, the single pulse takes a few microseconds, and the recorded voltage and current waveforms are employed to perform the

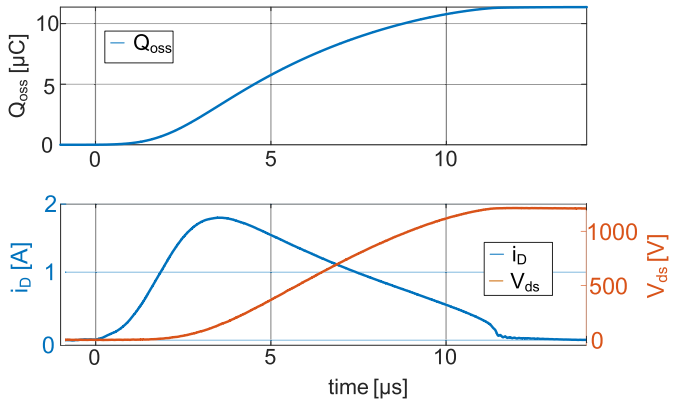

Fig. 5. Waveform of the drain current and drain–source voltage during a test of MSM900FS17ALT power module.

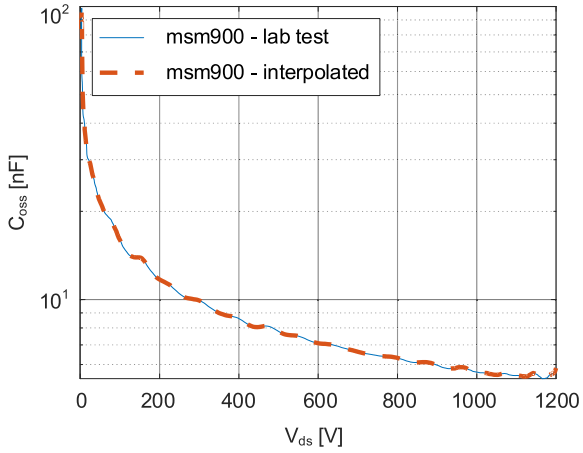

Fig. 6. Measured C_{OSS}–V_{DS} characteristics for MSM900FS17ALT.

calculations according to the basic capacitor formula

$$C_{OSS} = \frac{i_{COSS}}{dV_{DS}/dt}. \tag{1}$$

The calculation of (1) based on the waveforms in Fig. 5 was conducted in MATLAB, and the obtained C_{OSS}–V_{DS} characteristic is shown in Fig. 6. The obtained results have proved to be consistent with those obtained for a 1200-V/450-A SiC MOSFET power module compared to the characteristic available in its datasheet [34].

B. C_{OSS}–V_{DS} Test Method With Nonzero Turn-Off Voltage V_{GS}

As was mentioned above, several works reported the dependence of the capacitances on the turn-off gate-to-source voltage V_{GS-OFF} applied by the gate driver [15], [29], [30]. Therefore, further tests were conducted, with turn-off voltages ranging from −9 to +2 V applied, while the rest of the testing procedure was performed identically to what has been described before. In accordance with the theoretical assumptions, the impact is visible for low V_{DS} values [see Fig. 7(a)], where tests performed at low dc voltage are shown, while for higher V_{DS}, the differences were minimal, and thus, the results at high V_{DS} are not shown. Due to increased C_{GD} at higher V_{GS-OFF}, the C_{OSS} characteristic rises at low V_{DS} voltages,

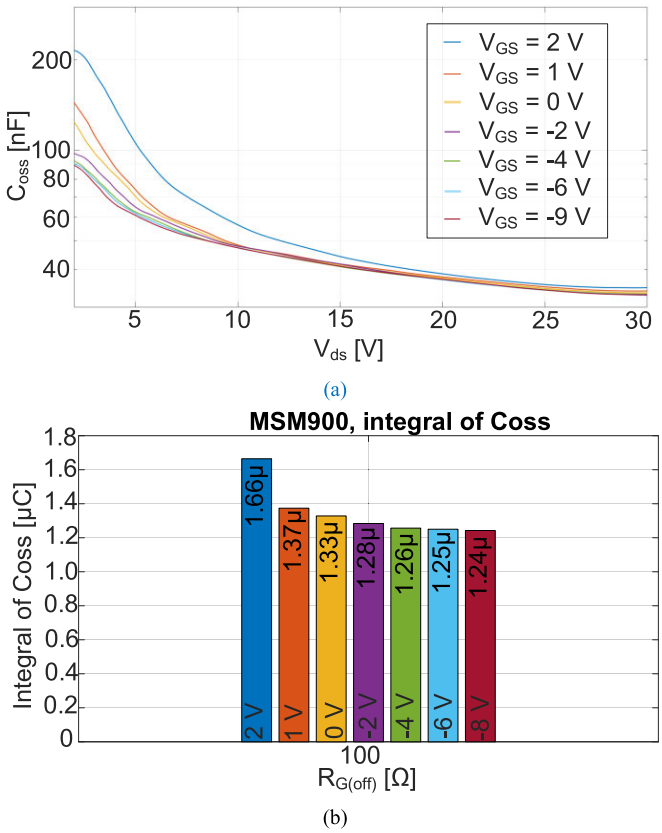

Fig. 7. (a) Dependence of measured C_{OSS} capacitance on the gate–source voltage value for low V_{DS} values. (b) Its impact on C_{OSS} integrated from 0 to 30 V of V_{DS}.

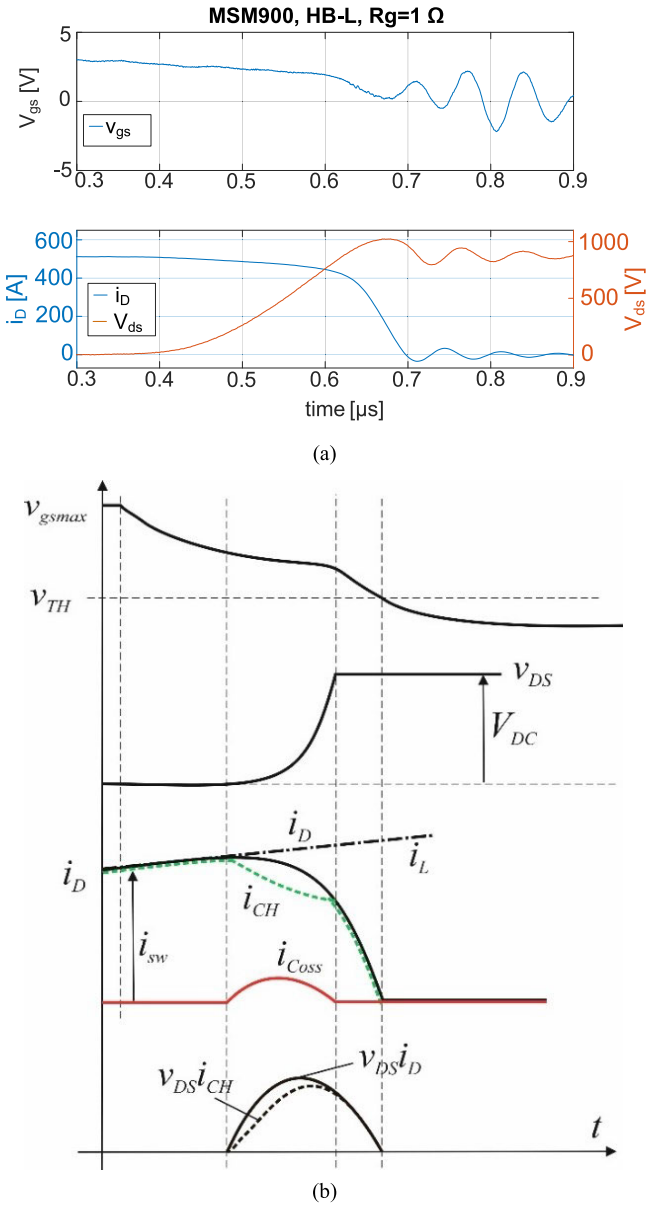

Fig. 8. (a) Waveforms during turn-off—recorded for the MSM900FS17ALT. (b) Idealized—without an influence of the parasitic inductance.

especially when V_{GS} is close to or above zero. In consequence, the charge Q_{OSS}, calculated as (2) for V_{DS} voltages up to 30 V, increases with the increase of V_{GS} [Fig. 7(b)]. The obtained results reflect that turning off at a voltage of −9 V results in a lower Q_{OSS}, meaning a lower switched current is required to achieve ZVS successfully. This difference is below 10% comparing turning off at 0 and −9 V, but the difference can be even as high as 30% comparing +2 and −9 V

$$Q_{OSS} = \int C_{OSS} dV_{DS}. \tag{2}$$

The gate voltage indisputably affects the C_{GD} capacitance, which notably impacts the transistor switching performance. This is caused by the influence of the gate voltage on the drain depletion layer beneath the gate oxide capacitance, which is dependent on the $V_{GD} = V_{GS} - V_{DS}$. However, the whole MOSFET output capacitance C_{OSS} required for estimating the channel current from V_{DS} value is dominated by the C_{DS} part, which is mainly unaffected by the change in gate–source voltage. Furthermore, the most notable shifts in capacitance occur for low drain–source voltages when the dissipated losses are rather low. When the switching turn-off power losses are considered, the crucial is the area for roughly 20%–80% V_{DS}, where the current is still on a significant level, while the voltage already reaches notable values, and the product (power loss) is eminent. Thus, the overall impact of the V_{GS} level on the proposed method can be easily neglected as the slight variations most likely still appearing in the C_{GD} component are so minuscule that are not distinguishable among the discrepancies and accuracy of the measurements. All in all, based on the performed tests and according to the MOSFET structure, the C_{OSS} capacitance is effectively independent of the gate polarization value, at least in terms of C_{OSS}–V_{DS} characterization for channel current estimation.

IV. Difference Between Drain and Channel Currents

Several typical waveforms recorded at the turn-off process of the MSM900FS17ALT at 850 V and 600 A are presented in Fig. 8(a), while idealized equivalents can be seen in Fig. 8(b). To simplify, the impact of parasitic inductances and high-frequency oscillations is not considered. In the optimal scenario from the switching losses point of view, the gate driver can quickly discharge the gate–source capacitance C_{GS}

to reach threshold voltage V_{TH} before drain–gate capacitance C_{GD} is charged and drain–source voltage v_{DS} achieves high values. The current through the channel of the power transistor i_{CH} is rapidly reduced to zero before v_{DS} is high, and, as a result, the power dissipated in the transistor (as the product of v_{DS} and i_{CH}) is low. These conditions can be recognized as almost ZVS, and this scenario is preferable as it results in nearly zero switch-on losses and therefore leads to higher efficiencies [7].

However, this scenario is challenging to achieve in most high-current power modules. The substantial input capacitance C_{ISS} requires a large gate current to be quickly discharged, but the limited supply voltage of the gate driver and nonzero internal gate resistance are the limiting factors. Thus, the real scenario usually observed is presented in the idealized waveforms in Fig. 8(b): during the voltage rising phase, the v_{GS} is above the threshold, and the channel remains open. This causes a major difference in the estimation of the switching power losses since the only source of power losses is the joule losses caused by the channel current through the device resistances, while the displacement current charging the output capacitance is not contributing to these power losses. Therefore, the resulting power losses are lower than the product of v_{DS} and i_D multiplication usually provided in the datasheets. Finally, v_{GS} drops below V_{TH} (and i_{CH} becomes zero) after v_{DS} has reached V_{DC}. It is worth noting that, at the end of the voltage rise phase, the observed i_D is equal to i_{CH}, since there is no displacement current in the output capacitances C_{OSS} when the voltage has reached a constant value. In practice, it will also be increased by voltage overshoots across parasitic inductances in the switching loop, as shown in Fig. 8(a).

V. Estimation of I_{COSS} and I_{CH}

The MSM900FS17ALT has been arranged in a half-bridge circuit supplied from an 850-V source and loaded with an inductive load (3 × 114 μH/100 A in parallel) with negligible resistance, so that the power circulates between the two power switches. The scheme of the experimental test system is presented in Fig. 9, using the same experimental setup as before but with an inductive load (shown in Fig. 4). Then, the transistors were controlled to generate a square voltage wave in the load to obtain a different amplitude of the load current, with a variable switching frequency up to 25 kHz, which is a typical value for high-power semiconductor modules as used in the article. These conditions lead to a triangle shape of the load current and switching conditions similar to those in soft-switched dc–dc converters. In particular, the transistors turn on with the current flowing through the antiparallel diode, and therefore, the on-state voltage is close to zero and turns off at peak load current. Thus, most of the power losses appear during the turn-off event twice per single switching period. In the circuit in Fig. 9, the drain–source voltage and drain current waveforms were measured with the high-bandwidth voltage probe (P5200A) and Rogowski coil. Examples of the results from the experimental study for different switched currents, along with the estimations of the channel and capacitive currents are depicted In Fig. 10 and Fig. 11 for

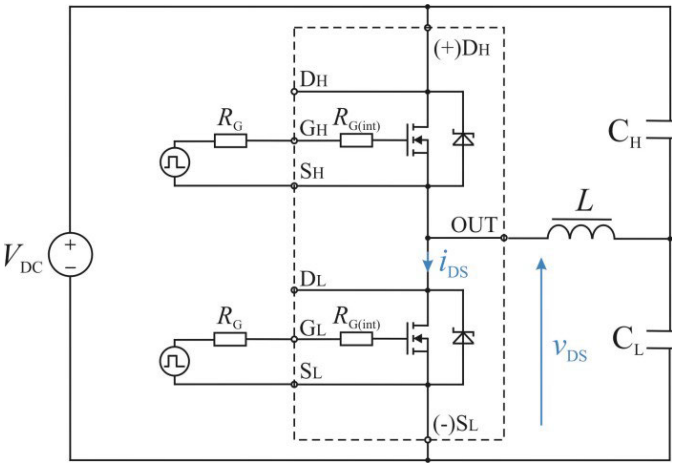

Fig. 9. Scheme of the half-bridge circuit with an inductive load.

$R_{G(EXT)} = 3.3\ \Omega$, and in Fig. 12 and Fig. 13 for a case without an external gate resistor. The switching process is faster for the higher current and lower gate resistance; the same observation can be made for the oscillations—they become more severe for the higher current and lower gate resistance.

The C_{OSS}–V_{DS} characteristic determined at $V_{GS\_OFF} = 0$ V before (Fig. 6) has been employed to calculate the capacitive current i_{COSS} during the switching process as (3), calculating the derivative of the drain–source voltage dv_{DS}/dt in MATLAB based on the measured waveforms

$$i_{COSS} = C_{OSS}(v_{DS})\frac{dv_{DS}}{dt}. \tag{3}$$

Furthermore, in order to take into account the voltage drop in the stray inductance inside the power module and therefore obtain more accurate results, v_{DS} in (2) was replaced by the internal $v_{DS(i)}$ calculated as

$$v_{DS(i)} = v_{DS} - L_S\frac{di_D}{dt} \tag{4}$$

where L_S is half of the internal module inductance provided by the datasheet. The obtained results are presented in Figs. 11 and 13 for $R_{G(EXT)} = 3.3\ \Omega$ and without an external gate resistor, respectively.

As can be observed based on Figs. 11 and 13, the effect of the capacitor current on the power loss estimation is substantial. For the low current operation of the power module (100-A switched current), the resulting relative error of the switched energy because of capacitor current omission can be as high as 100%, while for a high current test (600 A), it reaches slightly above 7%. However, considering a system at several hundred kilowatts, or single megawatts of power, this is still a substantial value in terms of the thermal design of the system, and thus, the effects of C_{OSS} and its' current should not be omitted, and the suggested C_{OSS}–V_{DS} characteristic obtaining method can be an invaluable tool for improving the design of high-power converters.

VI. Discussion

A closer analysis of the i_{COSS} waveforms presented in Figs. 10 and 12 shows that they are almost independent of the switched drain current. Only at the lowest currents, the

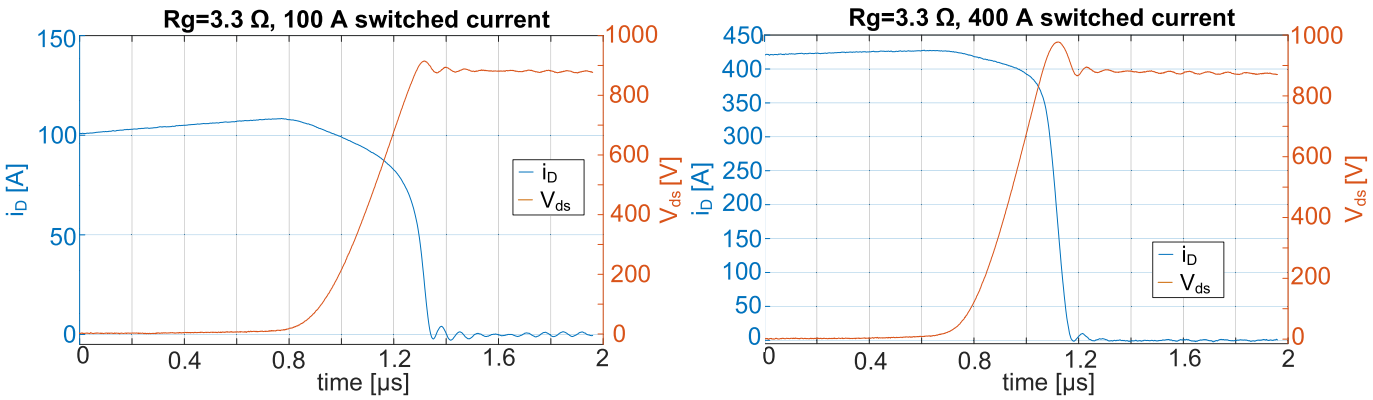

Fig. 10. Turn-off process for $R_{G(EXT)} = 3.3\ \Omega$ at 850 V and (a) 100 and (b) 400 A, measured values.

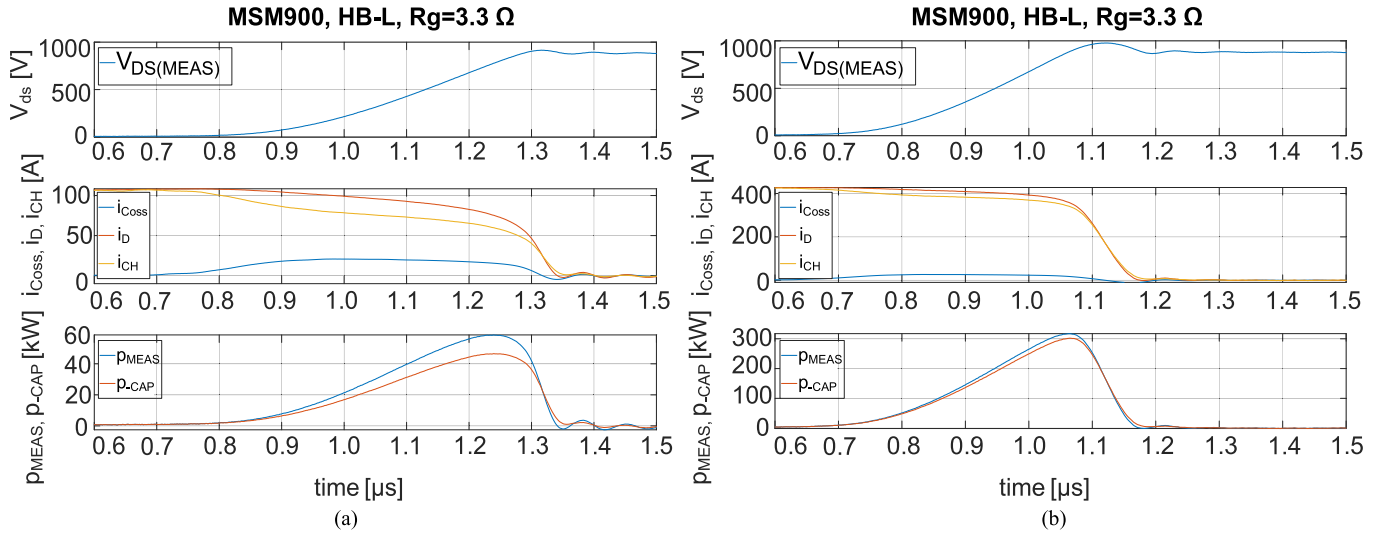

Fig. 11. Estimation of i_{COSS} and i_{CH} and resulting power losses for $R_{G(EXT)} = 3.3\ \Omega$ at 850 V and (a) 100 and (b) 400 A.

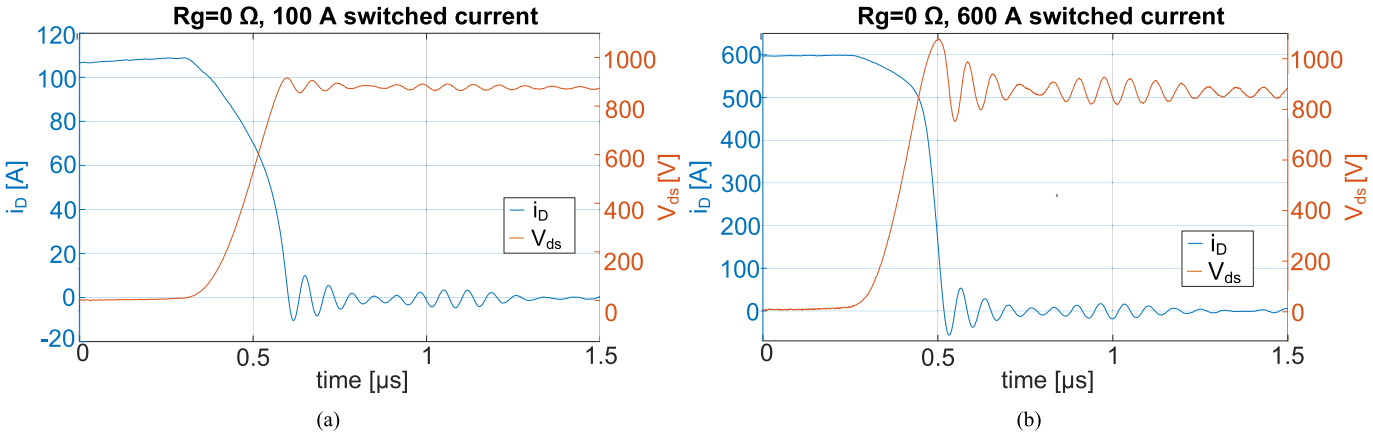

Fig. 12. Turn-off process for $R_{G(EXT)} = 0\ \Omega$ at 850 V and (a) 100 and (b) 600 A, measured values.

resulting i_{COSS} has presented differences, since the lack of switched current resulted in a longer voltage rising and a lower peak i_{COSS}. The major impact on the shape of i_{COSS} is the decrease of the gate resistance, resulting in a much higher switching speed. In particular, the peak value of the i_{COSS} is higher for faster switching. Both observations indicate that i_{COSS} is mainly the result of the charge displacement related to the changes in the drain potential. For the cases shown in Figs. 10 and 12 but also for two more gate resistance values [$R_{G(EXT)} = 1.6$ and 1 Ω], the waveforms of i_{COSS} were integrated to determine the charge Q_{OSS} (see results in Fig. 14). The values should be constant but vary between 8.9 and 9.7 μC (∼9% of the total error), which may be considered an acceptable value resulting from the measurement

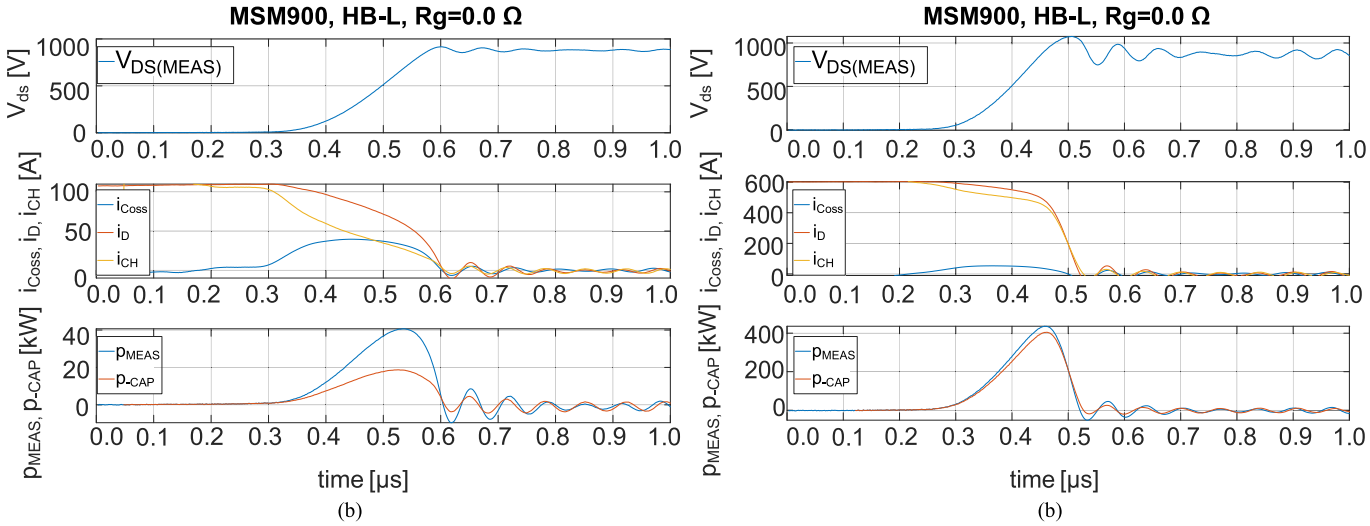

Fig. 13. Estimation of i_{COSS} and i_{CH} and resulting power losses for $R_{G(EXT)} = 0\ \Omega$ at 850 V and (a) 100 and (b) 600 A.

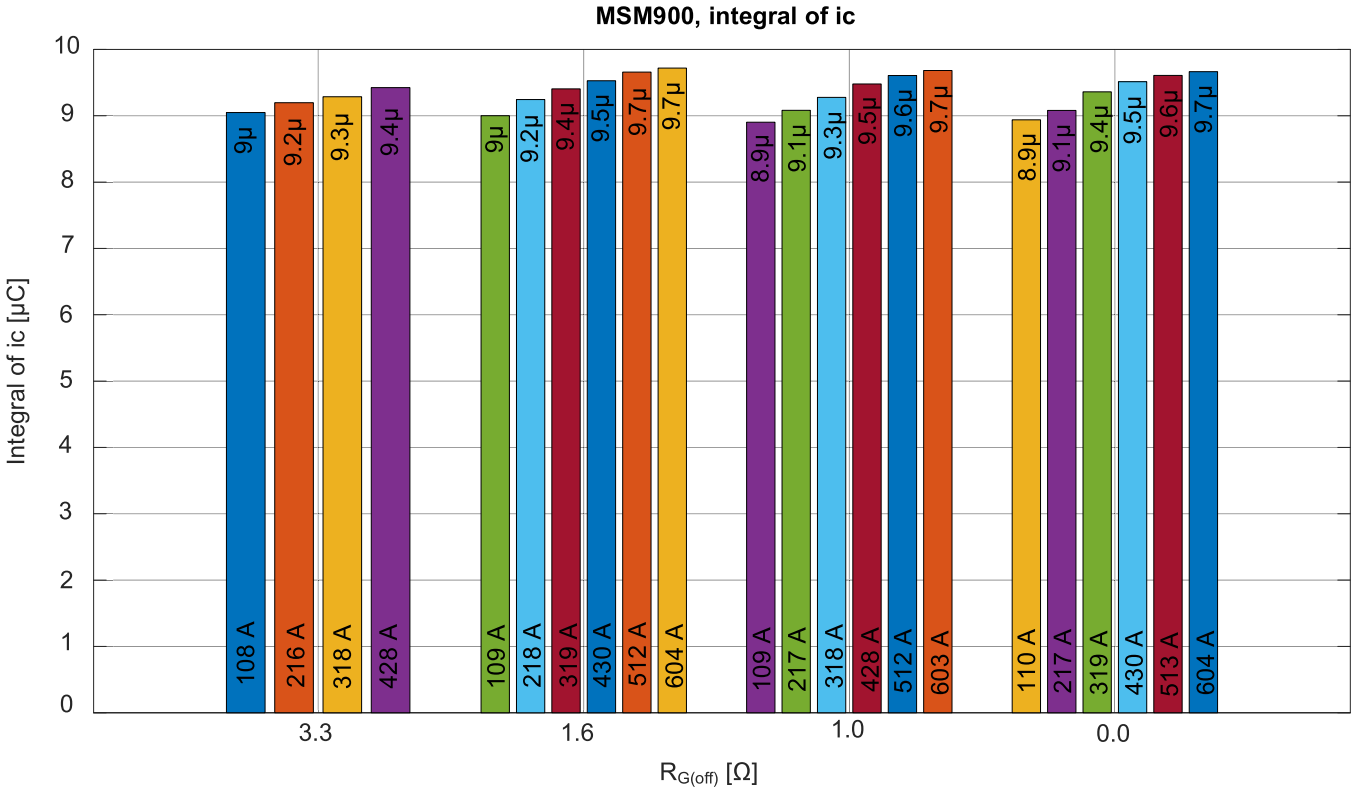

Fig. 14. Calculated Q_{OSS} at 850 V and different gate resistances and switched currents.

discrepancies. They rise with the switched current for all cases, which is, most likely, a result of higher voltage overshoot (increasing with the switched current and decreasing with the gate resistance). Note that the values for the same switched currents show minimal differences; thus, the obtained error from the measurements is in the half-bridge circuit rather than in the obtained $C_{OSS} - V_{DS}$ characteristic.

VII. Conclusion

This article presents a novel method for obtaining the $C_{OSS} - V_{DS}$ characteristics for SiC power modules. Its main advantage is a simple application within the half-bridge module without additional effort—a low-power, high-voltage power supply and typical voltage and current probes are necessary. The setup is very similar to the one required for double-pulse tests and power loss characterization of power devices. The test for the 1.2-kV/425-A module has shown very good agreement with the $C_{OSS} - V_{DS}$ characteristic provided by the manufacturer, and the method was also applied to the 1.7-kV/900-A module, for which the datasheet is unavailable.

Based on the measured characteristic, the capacitive current i_{COSS} has been calculated for this same module operating in the continuous mode at 850 V at different switching speeds with currents up to 600 A and switching frequencies up to

25 kHz. Then, Q_{OSS} was determined for all cases. Under the assumption that Q_{OSS} should be constant for all tested cases, the authors have determined errors in the whole procedure at the level of $\pm 4.5\%$. It is very likely that most of the error comes from the different voltage overshoots across the parasitic inductances. All in all, for the fast-switching SiC power devices, this is an acceptable value to increase the accuracy of power losses estimation of soft-switched dc–dc converters that can help to improve the design process of highly performant, high-power power electronic systems in medium voltage range.

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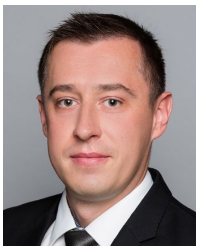

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