

Embedded Digital Phase Noise Analyzer for Optical Frequency Metrology

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Abstract—Digital signal processing (DSP) is supporting novel in-field applications of optical interferometry, such as in laser ranging and distributed acoustic sensing. While the highest performances are achieved with field-programmable gated arrays (FPGAs), their complexity and cost are often too high for many tasks. Here, we describe an alternative solution for processing optical signals in real-time, based on a dual-core 32-bit microcontroller. We implemented in-phase and quadrature (IQ) demodulation of optical beat-notes resulting from the interference of independent laser sources, phase noise analysis of deployed optical fibers covering intercity distances, and synchronization of remote acquisitions via optical trigger signals. The embedded architecture can efficiently accomplish a large variety of tasks in the context of optical signal processing, being also easily configurable, compact, and upgradable. These features make it attractive for applications that require long-term, remotely operated, and field-deployed instrumentation.

Index Terms—Digital signal processing (DSP), embedded system, frequency metrology, laser interferometry, lock-in amplifier, optical fiber sensing, phase measurement.

I. INTRODUCTION

IN RECENT years, coherent optical technologies are finding a growing number of applications outside the laboratories where they were first developed: optical clocks emerged as promising quantum sensors for probing the gravitational potential [1], [2]; optically coherent frequency combs suitable for in-field operation have been developed [3], with applications to environmental gas sensing [4], high-resolution ranging [5], [6], and transportable clock comparison [7]; coherent interferometry of narrow linewidth lasers on deployed optical cables proved to be a powerful tool for the remote distributed sensing of geophysical signals, opening new possibilities for the study of Earth dynamics [8], [9], with prospects of a future integration on data transmission networks [10], [11]; and finally, highly coherent laser sources in trusted communication nodes could improve the performances of advanced, quantum-secure communication protocols [12].

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Many of these applications require high-resolution and coherent measurements of the optical signal phase. While this is an easy task in a laboratory equipped with commercial instruments such as frequency counters or phase noise analyzers, the development of portable, reconfigurable, and scalable measurement setups equipped with remote control and alert systems is critical for in-field applications. Digital electronics and software-defined radio (SDR) greatly support this challenge, fulfilling sophisticated and time-critical tasks, and allowing preliminary signal processing onboard, before relevant data are transferred to remote control units at suitably reduced rates. So far, custom platforms based on field-programmable gate arrays (FPGAs) emerged as the best solutions for these tasks, with many applications in the context of optical frequency metrology [13], [14], [15]. Nevertheless, their high cost and the complexity associated with the board configuration make them a not obvious nor optimal choice in many cases, especially when compared with more affordable and practical architectures [16], [17], [18].

Here, we describe another approach, which makes use of a microcontroller unit (MCU) to implement optical phase measurements, based on the heterodyne demodulation scheme inherited from digital lock-in amplifiers [19], [20], [21]. The platform is based on the affordable yet high-performance STM32H7 unit, with dual-core 32-bit ARM architecture and integrated analog-to-digital converters (ADCs). Custom electronics and firmware were developed to realize a compact low-cost phase noise analyzer, with reconfigurable bandwidth and sampling rate. The optimized algorithm implements in-phase and quadrature (IQ) phase detection. Carrier frequency and amplitude of radio frequency (RF) signals can be measured with high resolution, at output data rates up to 20 kHz. The system is clocked with a stable quartz reference, and it includes synthesizers, digital-to-analog converters (DACs) and direct digital synthesizers (DDSs) for signal conditioning, resulting in a fully embedded stand-alone remote measurement unit.

Important features have been developed for the realization of long-term experiments with real-time acquisitions. In particular, we focused on developing a platform suitable for the frequency comparison of laser sources with spectral separation up to a few gigahertz, possibly varying over time, and the analysis of phase noise accumulated by a coherent signal as it travels a long-haul fiber. We implemented routines for synchronizing remote acquisitions within microseconds, suppressing common-mode noise processes. Our digital signal

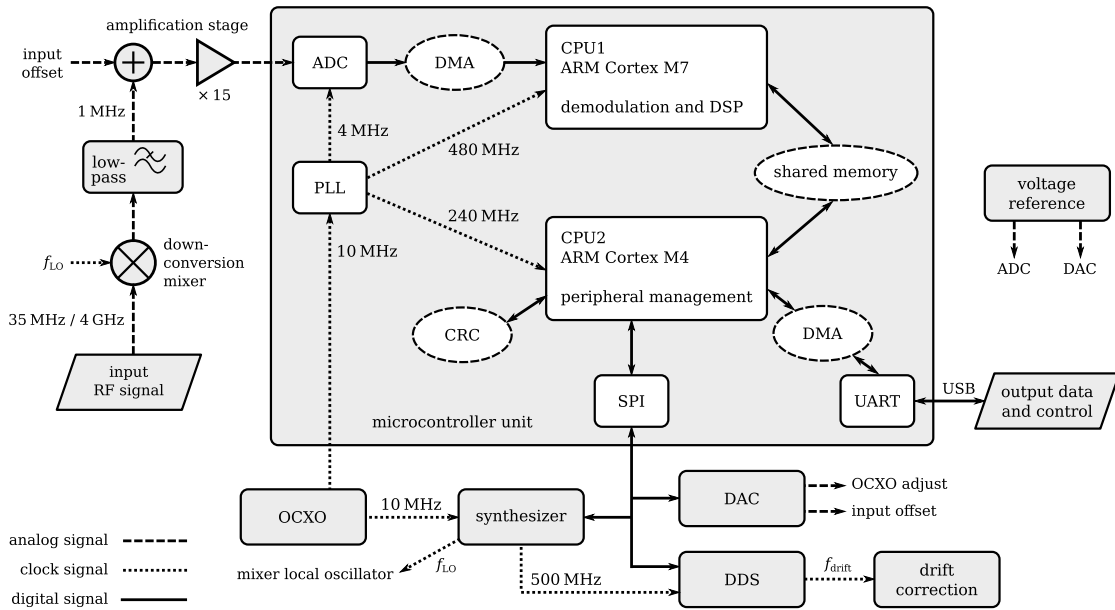


Fig. 1. Scheme of the acquisition system based on a dual-core microcontroller and its peripherals; the main elements of the input signal conditioning stage and other onboard components are also reported.

processing (DSP) solution addresses the typical challenges encountered in the processing of coherent optical signals, with proper handling of the amount of phase noise entering the demodulation steps, and combining high data rates with flexible and lightweight firmware algorithms.

II. SYSTEM ARCHITECTURE

A. Electronics and MCU

Our digital phase analyzer is implemented on a dual-core MCU from the STM32 series (STM32H745, STMicroelectronics), based on ARM Cortex central processing units (CPUs) with M7 and M4 32-bit architectures (CPU1 and CPU2, respectively). A custom printed circuit board (PCB) has been designed as a shield for the MCU development board NUCLEO-H745ZI-Q. The PCB includes the conditioning electronics for the input analog signals, as well as all the components required for the embedded system functioning. The electronic scheme of the microcontroller with its internal and external peripherals is sketched in Fig. 1.

The MCU includes three multichannel ADCs, having 16-bit nominal resolution and 12.2 effective number of bits (ENOB). The input signal is acquired using a fast ADC channel operated at 14 bits, which allows a maximum sampling rate of 5 MHz. To match the input bandwidth requirements, the signal to be measured is downconverted to the nominal frequency $\nu_0 = 1$ MHz using an external frequency mixer in combination with a low-pass filter (LPF) with 1.9 MHz cutoff. The RF signal is amplified and brought to the ADC voltage range of 0–2.5 V using a bipolar operational amplifier in noninverting configuration (AD8027, Analog Devices), with fixed gain 15, bandwidth from 0 to 8 MHz, and configurable voltage offset. This ADC input amplification scheme allows to acquire signals with different polarizations and frequencies, useful for debugging and general-purpose applications. For instance, when the external mixer is removed, this scheme also supports low-noise direct-coupling (DC) measurements.

The local oscillator (LO) signal for the frequency mixer is generated either by an embedded synthesizer (ADF4351, Analog Devices) in the range from 35 MHz to 4.4 GHz, or by a DDS (AD9912, Analog Devices) whose frequency is programmed with 48-bit resolution by the MCU via serial peripheral interface (SPI). This ensures on one side a broadband operating range for the input signal, and on the other the possibility of slowly tracking its low-frequency drifts by finely adjusting the DDS tuning word.

A 10-MHz oven-controlled crystal oscillator (OCXO) is integrated on the custom shield as the master clock source for the MCU and the other components. A good clock source is crucial for a high-performance phase measurement system. The chosen OCXO (HCD660/FTFN, Golledge) is characterized by 2×10^{-10} aging per day, short-term stability better than 1×10^{-12} (Allan deviation at 1 s), and phase noise lower than -155 dBc/Hz above 1 kHz. The MCU clock signals are generated from the 10-MHz reference using the internal phase-locked loops (PLLs). These include the 480-MHz clock of CPU1 and the 240-MHz clock for CPU2. A synchronous 4-MHz clock is generated by a MCU hardware timer and used to trigger the ADC acquisition. The synthesizer at the input downconversion stage is also referenced to the same OCXO, while the DDS is clocked at 500 MHz by the synthesizer. An external 10-MHz source can be provided for applications demanding a common clock architecture or higher accuracy, replacing the OCXO in all the above-mentioned tasks.

A 16-bit DAC (AD5686, Analog Devices) is used to generate the reconfigurable voltage offset for the signal conditioning stage and to fine-adjust the OCXO frequency through its dedicated tuning voltage input. The latter is used to compensate at the sub-mHz level the OCXO frequency offset and the quartz aging relatively to a reference oscillator.

The board is powered with ± 15 V and cooled with forced air flow. A low-noise precision voltage source at $V_{\text{ref}} = 2.5$ V (MAX6225-AE, Maxim Integrated) is used as analog reference

for the DAC and the MCU internal ADCs. Other sensors can be connected to the MCU shield by means of SPI, such as accelerometers and temperature sensors used to monitor the measurement environment conditions. Additional ADC channels can be used to acquire other experimental parameters at lower frequencies.

The MCU firmware is programmed in C language, exploiting the STM32 HAL and Low-Layer libraries. The dual-core architecture of the microcontroller is organized with the high-speed CPU1 being used for the computationally demanding DSP operations to be performed in real-time. These include ADC readout, IQ demodulation, digital filtering, and decimation to lower sampling rates. The computational cost is reduced by taking advantage of the direct memory access interface (DMA) for data transfer between the internal peripherals, which can operate without consuming CPU resources. Moreover, the data and instruction cache embedded in the MCU, in conjunction with a careful optimization of the firmware loops, reduces the memory access time while processing data. Finally, the 32-bit floating-point unit (FPU) allows faster calculations, with many floating-point operations being performed as single CPU cycles.

After decimation, the processed data are transferred to CPU2 exploiting a shared memory region and hardware semaphores. That secondary processor is dedicated to the continuous data streaming toward a computer unit, used for data storage. The connection is obtained with a universal asynchronous receiver-transmitter (UART) serial interface via universal serial bus (USB) at 4-Mbits⁻¹ baud rate. Data consistency is checked by means of the cyclic redundancy check (CRC) internal peripheral. CPU2 is dedicated also to the general system management: it parses the commands received from the computer to configure and control the acquisition, and it manages the external peripherals connected to the board via SPI. Operation priorities are managed by means of MCU hardware interrupts.

B. Digital Signal Processing

1) *Phase Demodulation*: The input signal phase is processed exploiting the IQ demodulation technique. This is a common approach to phase detection in digital systems, typically implemented on FPGAs to process the RF signals acquired with fast ADCs [22], [23], [24]. However, some algorithm optimizations have to be considered to maintain good performances also on a resource-limited MCU such as in our case [25], [26], [27], [28].

It is useful to first recap a few general concepts that will help illustrate our DSP operation. First, consider the general case of a RF voltage signal $V(t)$ at time t , characterized by nominal frequency ν_0 , and time-varying amplitude $A_s(t)$ and phase $\phi(t)$, expressed as

$$V(t) = A_s(t) \sin(2\pi \nu_0 t + \phi(t)). \quad (1)$$

The time-dependent fluctuations of the signal phase give rise to deviations of the instantaneous carrier frequency $\nu(t)$ from the nominal value ν_0 , and are the primary information of interest in our context, thus

$$\Delta\nu(t) = \nu(t) - \nu_0 = \frac{1}{2\pi} \frac{d\phi(t)}{dt}. \quad (2)$$

The two notations will be indifferently adopted throughout the text.

In a phase-sensitive detector, the input signal is demodulated by mixing with the IQ references $r_I(t)$ and $r_Q(t)$, here conveniently taken at frequency ν_0 and with unitary amplitude

$$r_I(t) = \cos(2\pi \nu_0 t) \quad (3a)$$

$$r_Q(t) = \sin(2\pi \nu_0 t). \quad (3b)$$

The mixed signals are low-pass filtered with transfer function H_{LPF} and cutoff frequency f_{BW} , to extract the IQ components

$$I(t) = H_{\text{LPF}}\{r_I(t)V(t)\} = \frac{1}{2} A_s(t) \cos(\phi(t)) \quad (4a)$$

$$Q(t) = H_{\text{LPF}}\{r_Q(t)V(t)\} = \frac{1}{2} A_s(t) \sin(\phi(t)). \quad (4b)$$

The filter suppresses the higher order frequencies and determines the demodulation bandwidth. The signal amplitude and phase are then calculated as follows:

$$A_s(t) = 2\sqrt{I^2(t) + Q^2(t)} \quad (5a)$$

$$\phi'(t) = \arctan2(Q(t), I(t)). \quad (5b)$$

It is worth to note that $\phi'(t)$ is a wrapped version of the original phase $\phi(t)$, since the domain of the four-quadrant inverse tangent function is defined between $-\pi$ and $+\pi$.

These same steps are implemented in our MCU firmware, as shown in Fig. 2(a). When the signal $V(t)$ is sampled by the ADC at frequency f_{smp} , the previous relations remain valid at discrete instants n/f_{smp} , with n integer, thus

$$V[n] = A_s[n] \sin(2\pi \nu_0 n/f_{\text{smp}} + \phi[n]). \quad (6)$$

The IQ references are generated numerically, hence driven by the OCXO clock and the MCU PLLs, such that

$$r_I[n] = \cos(2\pi \nu_0 n/f_{\text{smp}}) \quad (7a)$$

$$r_Q[n] = \sin(2\pi \nu_0 n/f_{\text{smp}}). \quad (7b)$$

The LPF with cutoff f_{BW} has been implemented as a finite impulse response (FIR) filter. Although with higher computational cost, only partially mitigated by the MCU cache and FPU, the choice of a FIR filter over a infinite impulse response (IIR) one is mainly justified by its linear phase response: this is a key feature for accurate phase measurements without distortion. Moreover, due to the absence of feedback, the intrinsic stability of FIR filters makes them the optimal solution for reliable acquisitions, avoiding effects of self-oscillations and coefficient quantization errors.

With a FIR implementation, the filtered signal becomes a weighted sum of $N + 1$ terms, with N the filter order, and the weight coefficients defining the frequency response. Consequently, the algorithm complexity can be reduced by exploiting the system linearity, specifically by combining the LPF transfer function H_{LPF} with the reference mixing operation in (4). This means that the demodulation of the signal components $I[n]$ and $Q[n]$ can be performed with

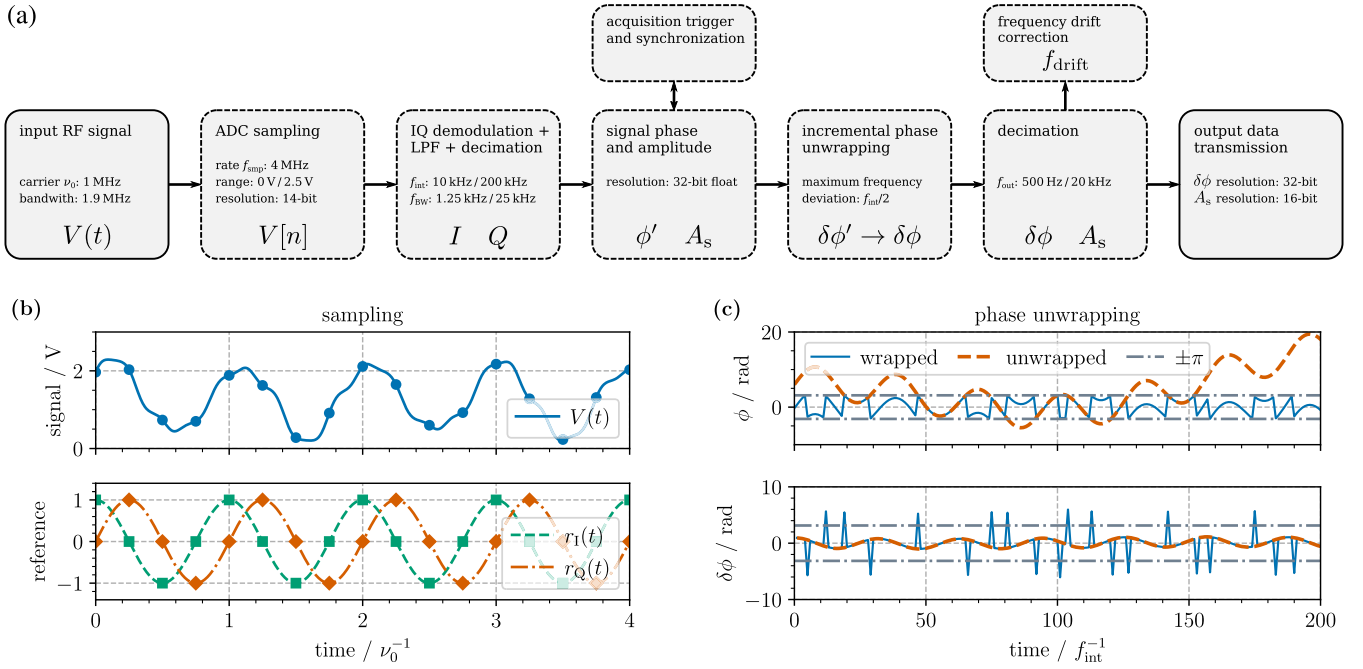


Fig. 2. (a) Scheme of the main DSP steps implemented in the microcontroller firmware for signal demodulation. (b) Sketch of the sampled input signal, demodulated relatively to internal IQ references. (c) Sketch of phase unwrapping to reconstruct the original absolute phase.

single FIR filtering operations, having transfer functions H_I and H_Q , respectively, such that

$$I[n] = H_I\{V[n]\} = \sum_{i=0}^N h_I[i]V[n-i] = \frac{1}{2}A_s[n]\cos(\phi[n]) \quad (8a)$$

$$Q[n] = H_Q\{V[n]\} = \sum_{i=0}^N h_Q[i]V[n-i] = \frac{1}{2}A_s[n]\sin(\phi[n]). \quad (8b)$$

Exploiting symmetry properties, the demodulation filter coefficients $h_I[i]$ and $h_Q[i]$ are calculated as the product between the LPF coefficients $h_{LPF}[i]$ and the references $r_I[i]$ and $r_Q[i]$, respectively

$$h_I[i] = r_I[i]h_{LPF}[i] \quad (9a)$$

$$h_Q[i] = r_Q[i]h_{LPF}[i]. \quad (9b)$$

It is worth to note that although sharing the same LPF coefficients and frequency response, characterized by bandwidth f_{BW} and center frequency ν_0 , the combination of filtering with IQ reference mixing allows to discriminate the two orthogonal signal components, shifted by $f_{smp}/4\nu_0$ samples. Compared with independent mixing and filtering, this demodulation approach requires fewer real-time computations for each sample.

Considering that the IQ components are limited to a bandwidth f_{BW} , they can be decimated without aliasing down to a reduced rate $f_{int} > 2f_{BW}$. Therefore, only one sample every f_{smp}/f_{int} needs to be processed, effectively reducing the data rate and CPU load. Amplitude $A_s[n]$ and wrapped phase $\phi'[n]$ are then calculated at the intermediate rate f_{int} using (5).

The algorithm is further optimized by choosing

$$f_{smp} = 4\nu_0. \quad (10)$$

In fact, as can be seen from (7) and Fig. 2(b), in this case half of the IQ coefficients are equal to zero. This means that the actual computational cost is halved, or that the filter order of H_I and H_Q can be doubled for a given CPU clock frequency.

2) *Phase Unwrapping*: Following the arctan2 function definition, $\phi'[n]$ wraps with $\pm 2\pi$ jumps when the signal phase exceeds the $\mp\pi$ domain bounds [29]. An unwrapping algorithm is required to recognize and compensate such phase discontinuities, recovering the continuous phase as sketched in Fig. 2(c).

The processing is performed on the phase increments, calculated from the absolute phase values

$$\delta\phi'[n] = \phi'[n] - \phi'[n-1]. \quad (11)$$

Phase wraps can be detected by searching for values of wrapped phase increments $\delta\phi'[n]$ larger than $\pm\pi$. Consequently, the unwrapped phase increments $\delta\phi[n]$ can be reconstructed

$$\begin{cases} \delta\phi'[n] > +\pi & : \delta\phi[n] = \delta\phi'[n] - 2\pi \\ -\pi \leq \delta\phi'[n] \leq +\pi & : \delta\phi[n] = \delta\phi'[n] \\ \delta\phi'[n] < -\pi & : \delta\phi[n] = \delta\phi'[n] + 2\pi. \end{cases} \quad (12)$$

The absolute phase can be retrieved by integration as

$$\phi[n] = \sum_{i=1}^n \delta\phi[i]. \quad (13)$$

Nonetheless, the samples are always treated in terms of phase increments during the whole DSP process, since the absolute phase could accumulate rapidly to big values, and

floating-point variables with 32-bit resolution would lose precision soon. On the contrary, phase increments are confined within the $\pm\pi$ interval.

Considering that unwrapping is performed for each new value of $\delta\phi[n]$ at the intermediate frequency f_{int} , from (2), it follows that the instantaneous frequency deviation from the nominal carrier ν_0 is proportional to the unwrapped incremental phase $\delta\phi[n]$, thus

$$\Delta\nu[n] = \nu[n] - \nu_0 = \delta\phi[n] \frac{f_{\text{int}}}{2\pi}. \quad (14)$$

In applications where optical signals are affected by phase noise processes, it is critical to preserve the coherence of the accumulated phase [30]. This can be broken by two distinct effects which are addressed in the following. First, big instantaneous frequency deviations, giving rise to $|\delta\phi[n]| > \pi$, can be mistakenly interpreted as phase wraps and cause aliasing. The maximum frequency deviation that can be unwrapped without ambiguity is

$$\Delta\nu_{\text{max}} = \pm \frac{f_{\text{int}}}{2}. \quad (15)$$

Phase undersampling can be avoided by increasing f_{int} . However, the intermediate frequency is typically limited by the computational power of the processing unit. A good demodulation filtering stage which attenuates the high-frequency components can mitigate the aliasing effects.

Another aspect that can cause phase unwrap failures is phase noise. In fact, high noise levels added to the original signal will cause wrong unwrap events. A solution would be a narrower demodulation bandwidth to suppress a wider part of the noise spectrum. On the other hand, f_{BW} must be chosen depending on the actual signal dynamics: if the demodulation filter band is too narrow, the demodulated signal can be distorted. Moreover, narrower filtering requires higher filter orders: at finite computational power, this can be achieved only at lower f_{int} values. Therefore, a compromise between this and the previous limits must be taken into account.

3) *Data Decimation*: Although phase unwrapping must be performed at high rate to avoid aliasing, the required output data rate and measurement bandwidth are typically much lower than f_{int} , which can be of the order of several tens of kHz. Therefore, after demodulation and phase unwrapping, amplitude and incremental phase are further decimated to frequency f_{out} by applying an anti-aliasing FIR filter, and by taking one sample every $f_{\text{int}}/f_{\text{out}}$. The decimated data are then packed into chunks of samples and transmitted to the control computer. The time consistency of samples is guaranteed by the OCXO clock over all the DSP steps.

4) *Acquisition Trigger*: The MCU supports external triggering through a digital input assigned to a hardware interrupt that starts the acquisition. Nevertheless, some applications require synchronous acquisitions at remote locations, without a direct access to the trigger signal: to meet this requirement, we enabled the system to accept trigger signals encoded as specific modulation patterns onto the acquired signal. A dedicated firmware routine manages the acquisition start: initially, the demodulation process is kept running in an idle state, where either amplitude or phase is continuously sampled

and compared with the required trigger level at rate f_{int} ; the actual data transmission, hence the acquisition timescale, is started only when the trigger condition is met. Therefore, the acquisition timescales of independent boards measuring a common signal can be synchronized, with a maximum relative delay of $\pm 1/f_{\text{int}}$ given by the condition check rate.

5) *Drift Correction*: Our implementation of IQ demodulation operates with a digital heterodyne reference, fixed by the OCXO clock. If the carrier frequency of the input signal differs significantly from the nominal value ν_0 or changes over time, namely, by more than a quantity f_{BW} , it can exceed the demodulation filter band, and the acquisition fails. To avoid this, a digital proportional–integral–derivative controller (PID) is implemented in the MCU firmware to track and compensate in real-time the slow carrier drifts. The PID takes as input the demodulated frequency deviation passed through an appropriate LPF, and it adjusts the DDS tuning word at frequency f_{drift} . This can be used as negative feedback to drive either the LO of the input downconversion mixer or, e.g., an external modulator that actually shifts the carrier frequency. The original signal frequency can be reconstructed deterministically in postprocessing by combining the measurements with the recorded f_{drift} values.

C. System Configuration

1) *DSP Parameters*: The carrier center frequency is designed as $\nu_0 = 1$ MHz. This is a compromise between the maximum ADC sampling rate and the DSP capabilities on one hand, and the lower electronic noise affecting the high-frequency spectrum. Higher central frequencies also enable wider dynamic ranges to be correctly demodulated. Following (10), the ADC sampling is triggered by an internal hardware timer at $f_{\text{smp}} = 4\nu_0 = 4$ MHz.

The demodulation FIR filter is obtained combining a low-pass Hamming window with the IQ references, skipping the samples corresponding to FIR coefficients equal to zero. An example is shown in Fig. 3(a). The filter order is limited by the MCU speed, with $8f_{\text{smp}}/f_{\text{int}}$ filter coefficients. The filter bandwidth is designed as $f_{\text{BW}} = f_{\text{int}}/8$. Different configurations, corresponding to f_{int} between 10 and 200 kHz, are preloaded in the MCU memory, to allow on-the-fly reconfiguration of the demodulation stage via software. Examples of filter magnitude responses are reported in Fig. 3(b). The optimal configuration in terms of dataflow processing stability and phase unwrap efficiency is typically obtained for $f_{\text{int}} = 100$ kHz.

The coefficients of the FIR LPF for the output data decimation to rate f_{out} are calculated considering an Hamming window, with $12f_{\text{int}}/f_{\text{out}}$ coefficients, and bandwidth close to $f_{\text{out}}/3$, optimized to reduce aliasing due to sidelobes of the filter transfer function. The coefficients are precalculated for f_{out} between 500 Hz and 20 kHz.

The LPF for the frequency drift correction is a first-order IIR kind. The filter and PID parameters can be configured by software, depending on the drift dynamics. The cutoff frequency is typically kept very low not to interfere with the signal high-frequency components of interest.

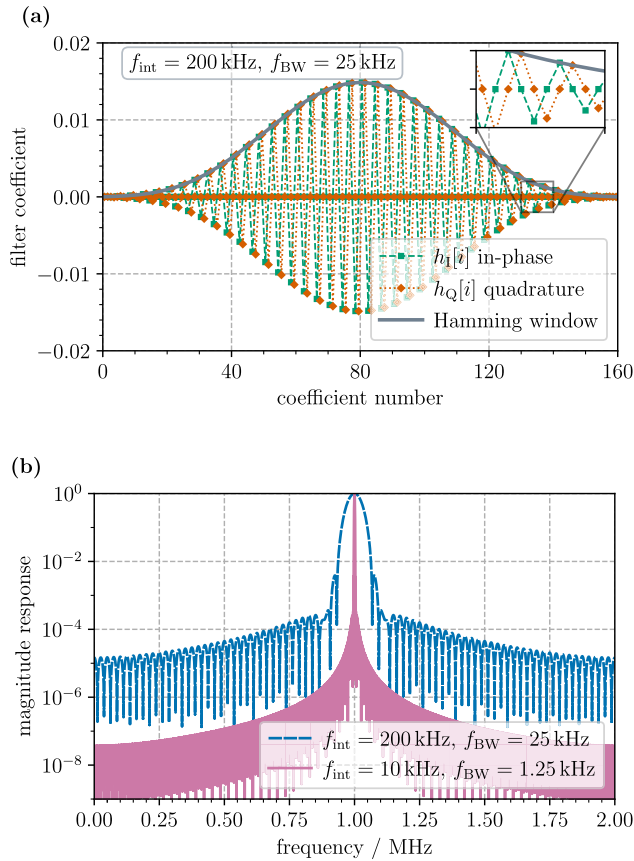


Fig. 3. (a) Example of coefficients for IQ demodulation and filtering. (b) Frequency response of the demodulation filter for two intermediate frequency values.

2) *Synchronization*: In the case of synchronization of remote systems, with the trigger event being encoded on the signal to be measured, the choice of f_{int} impacts on the achievable synchronization resolution. Therefore, during the triggering procedure f_{int} is set at the highest possible value, i.e., $f_{\text{int}} = 200$ kHz. In this configuration, the maximum jitter between independent trigger instances is ± 5 μs . Assuming an uniform uncertainty distribution, the expected standard deviation over the initial timescale is $\sigma_{\text{sync}} \sim 3$ μs .

After the trigger event is detected, each board switches to the desired f_{int} value and starts the acquisition. The loss of synchronization will depend solely on the frequency offset and drift for the independent clock sources, mostly due to temperature fluctuations and quartz aging. A firmware routine is dedicated to resynchronize the acquisitions on-the-fly, with a small latency of about 110 μs . The routine combines the trigger detection with a measurement of the relative delay accumulated since the last resynchronization event. This allows to compensate for the oscillator frequency fluctuations, fine-tuning the OCXO adjust voltage on a daily timescale.

The residual delay accumulated by the independent OCXOs can be estimated assuming a linear fractional frequency drift, which has been measured to be $D \sim 2 \times 10^{-13}$ s^{-1} . Accordingly, the time interval after which the cumulative clock delay reaches the time accuracy of σ_{sync} is $(2\sigma_{\text{sync}}/D)^{1/2} \sim 5000$ s. This means that performing a resynchronization procedure

every hour is sufficient to maintain the timescales synchronized to within σ_{sync} .

3) *Numerical Resolution*: Before unwrapping, $\delta\phi'_m[n]$ is defined between -2π and $+2\pi$. This means that the numerical resolution for calculations with 32-bit floating-point variables is always better than 0.5 μrad . This corresponds to a frequency resolution of 8 mHz at the typical intermediate frequency $f_{\text{int}} = 100$ kHz, stressing that this is a conservative estimation related to big $\Delta\nu$ values. Amplitude is defined between 0 V and $V_{\text{ref}}/2 = 1.25$ V, and hence, its 32-bit floating-point numerical resolution is better than 0.1 μV .

For transmission bandwidth optimization, the phase and amplitude samples are transmitted to the control unit as integers, with 32- and 16-bit resolution, respectively, corresponding to 1.5 nrad (or 23 μHz with $f_{\text{int}} = 100$ kHz) and 19 μV . The effects of numerical truncation can be expected beyond these limits.

D. Software Control

The acquired data are transmitted in real-time to a computer via USB connection. The decimated data are packed in chunks containing incremental phase, amplitude, frequency drift correction, and other monitoring variables, with an output data rate up to 20 kHz. The data are received by a software written in Python, checked for CRC integrity and stored incrementally in HDF5 binary files, together with the system settings. The software controls the embedded system functions via serial commands and allows to configure its parameters on-the-fly.

III. EXPERIMENTAL CHARACTERIZATION

Our measurement system has been characterized with RF signals generated by a commercial synthesizer (3352A, Agilent), externally referenced to a hydrogen maser. The board was also referenced to the same stable source, to exclude noise contributions due to the OCXO. The measurement noise was estimated by acquiring sinusoidal signals having 1 MHz nominal frequency. The acquisition was configured with $f_{\text{int}} = 100$ kHz and $f_{\text{out}} = 4$ kHz. Fig. 4(a) shows the power spectral density (PSD) $S_{\Delta\nu}(f)$, with f the Fourier frequency, of the frequency fluctuations $\Delta\nu$ measured at different signal amplitudes, up to $A_s = 1$ V. The noise spectra are characterized by white phase noise, with a negligible additional noise in the low-frequency region. Weaker signals exhibit higher phase noise floors, due to the lower signal-to-noise ratio in the demodulation band: notably, the noise power scales as $1/A_s^2$. This is consistent with the ADC noise expected considering the resolution given by its ENOB.

Fig. 4(b) shows the frequency instability calculated in terms of the overlapping Allan deviation $\sigma_{\Delta\nu}(\tau_a)$, with τ_a the averaging time, for a 1-MHz signal at amplitude 1 V, acquired for 2000 s with $f_{\text{int}} = 100$ kHz and $f_{\text{out}} = 10$ kHz. The curve exhibits the expected behavior for white-phase-limited measurements on a bandwidth of about 4 kHz. In particular, the impact of white phase noise on the Allan deviation could be reduced by reconfiguring the output filter to a lower measurement bandwidth. This considerably mitigates the aliasing effects which are often encountered with frequency

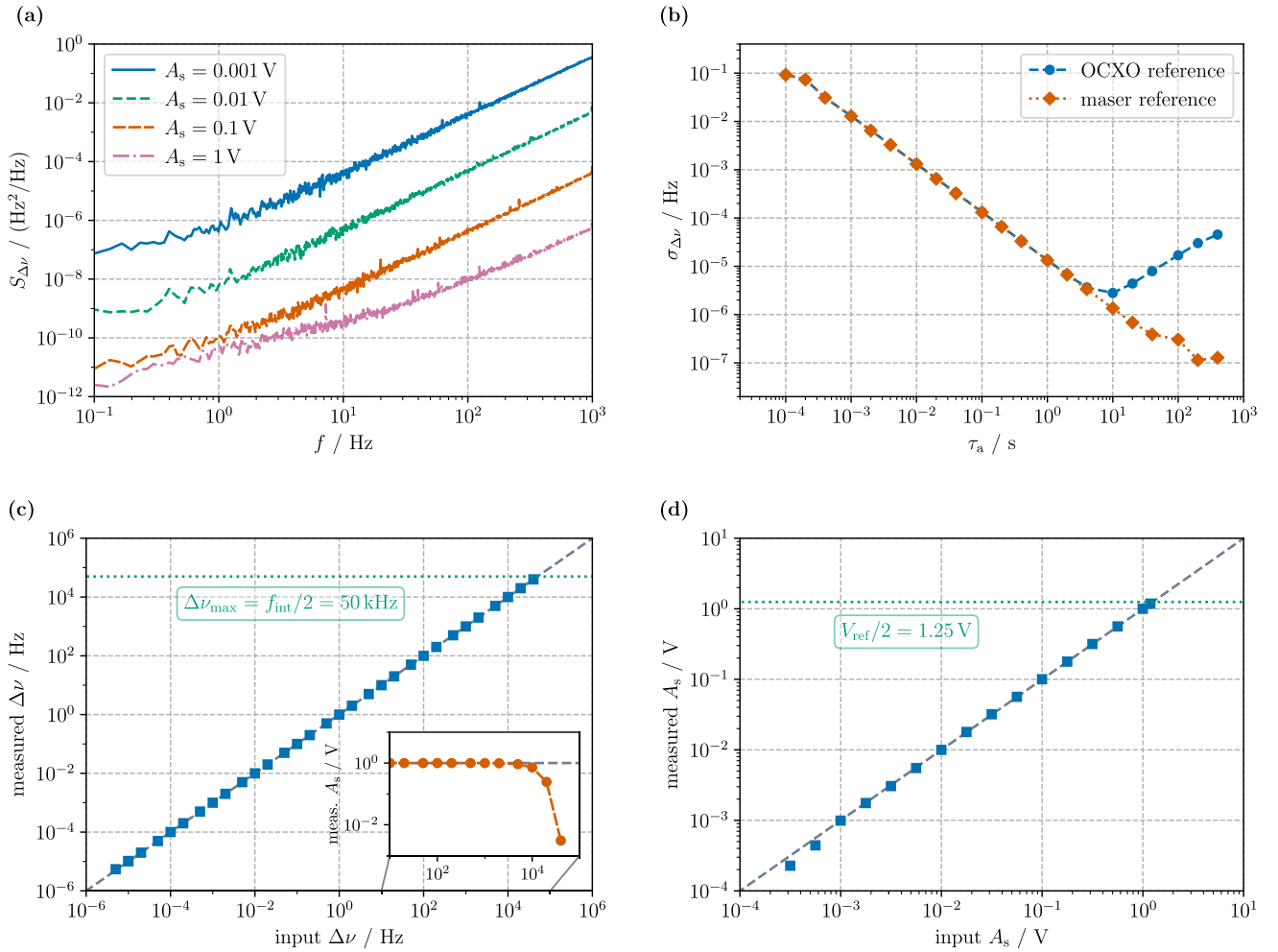


Fig. 4. (a) PSD of frequency signals acquired with the measurement board as a function of Fourier frequency; the signals are generated with 1-MHz carrier frequency and variable amplitude. (b) Allan deviation calculated for 1-MHz signals at 1-V amplitude as a function of averaging time, considering either maser or OCXO reference for the board clock. (c) Measured frequency as a function of nominal input frequency at 1-V amplitude; the dashed diagonal represents the expected correspondence; the inset shows the corresponding measured amplitude. (d) Amplitude measured as a function of nominal input amplitude for 1-MHz signals; the dashed diagonal represents the expected correspondence.

counters [31]. When the measurement is repeated with the acquisition system referenced to the onboard OCXO, the quartz drift becomes dominant for averaging times above $\sim 10 \text{ s}$.

When $f_{\text{int}} = 100 \text{ kHz}$, the maximum frequency that can be measured without aliasing is $f_{\text{int}}/2 = 50 \text{ kHz}$; actually, the demodulation filter has a cutoff of $f_{\text{BW}} = 12.5 \text{ kHz}$ and acts as anti-aliasing filter. To address the frequency response of the demodulation, signals at different carrier frequencies $\nu_0 + \Delta\nu$ were acquired, with $\Delta\nu$ between $5 \mu\text{Hz}$ and 40 kHz , and amplitude fixed to 1 V . The measured frequency was averaged over 50 s at $f_{\text{out}} = 10 \text{ kHz}$, and compared with the nominal input frequency as shown in Fig. 4(c). A linear fit to the data allows quantifying the measurement linearity, as well as an assessment of the demodulation process accuracy over ten orders of magnitude. The linearity coefficient is 1 within 2×10^{-8} , while the intercept of about $20 \mu\text{Hz}$ can be attributed to numerical resolution and truncation. The inset of Fig. 4(c) quantifies the signal amplitude attenuation as a function of the input frequency: it confirms that frequency components above 30 kHz are strongly suppressed by the demodulation filter,

by more than 20 dB . Aliasing effects at the phase unwrap stage are therefore negligible.

We characterized the linearity in the amplitude demodulation by acquiring signals with fixed $\Delta\nu = 0 \text{ Hz}$ and variable amplitude, between 0.3 mV and 1.2 V . The maximum amplitude that can be measured without distortion is half of the ADC voltage reference, hence $V_{\text{ref}}/2 = 1.25 \text{ V}$. The results are shown in Fig. 4(d). The corresponding linearity coefficient depends on the knowledge of the input amplification gain, which is about 15. Nonetheless, the linearity relative uncertainty of 7×10^{-4} and the bias of 0.3 mV give figures for the corresponding amplitude resolution over almost 4 orders of magnitude. We also verified that cross-talks between phase and amplitude are negligible, as long as the signal carrier lays within the demodulation filter band.

The mechanism of remote synchronization was tested by arming two different boards to wait for a trigger signal with amplitude greater than half the nominal amplitude. A common input signal was obtained through downconversion using the DDS, split and sent to the two boards. The signal frequency was stepped between 1.25 and 1 MHz , to bring it within

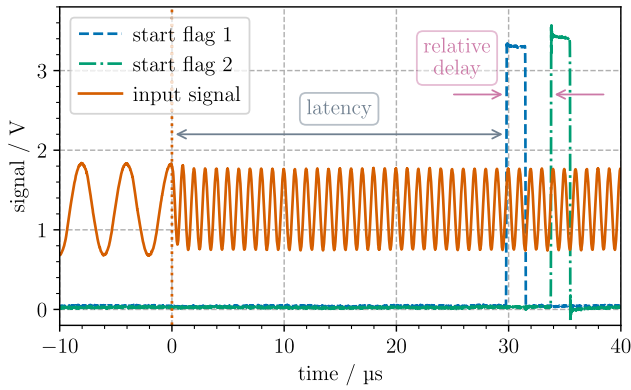


Fig. 5. Signals related to the acquisition with two synchronized boards, acquired with an oscilloscope. A common input RF signal is split and sent to each system. The carrier frequency is shifted to 1 MHz at time 0 s, and each board, 1 and 2, starts the acquisition after a latency interval.

the demodulation band and generate a rising amplitude edge, acting as trigger. The acquired signal was monitored with an oscilloscope, as shown in Fig. 5. The triggering instants on each board were detected by raising digital output flags when the acquisitions started. An average latency of $32 \mu\text{s}$ was measured between the instant at which the carrier is shifted into the demodulation band and the actual acquisition starts. This latency depends only on the system architecture, since it is caused by the deterministic initialization time required for the MCU peripherals and by the DSP algorithm, e.g., the intrinsic FIR filter delay. The average relative delay between the two boards over 30 synchronized acquisitions showed a synchronization uncertainty given by a standard deviation of $\sigma_{\text{sync}} = 2.9 \mu\text{s}$, as expected for $1/f_{\text{int}} = 5 \mu\text{s}$ and discussed in Section II-C2.

IV. OPTICAL PHASE SENSING

We now consider the case study of two ultrastable lasers placed in two distant locations, connected by a telecom fiber link established on a pair of unidirectional optical fibers, running parallel inside the same cable. At each location, we interfere the laser signals, measure the beat-note frequency, and synchronize the respective acquisition platforms by encoding a trigger event on the ultrastable carriers. We compensate in real-time the slow frequency drifts of the beat-note, and we demonstrate the possibility of measuring both the fiber and laser noises by suitably combining the synchronized acquisitions.

A. Optical Setup

We implemented an experimental layout that allows either the self-heterodyne interference of each laser source independently, exploiting the round-trip path in the fiber as a delay line, or the heterodyne interference of the two lasers on a two-way approach. The optical setup is shown in Fig. 6.

Each laser source (L1 and L2) is a commercial external cavity diode laser with 1542-nm wavelength and intrinsic 10-kHz linewidth, frequency stabilized to a 5-cm-long, high-finesse cavity, using the Pound–Drever–Hall technique [32], on a bandwidth of 200 kHz. The resulting short-term stability is 2×10^{-15} , with a drift of the order of 0.5 Hz s^{-1} .

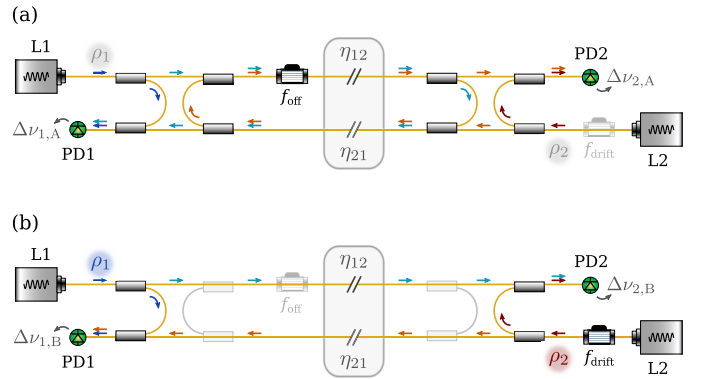


Fig. 6. Optical schemes for the comparison between two ultrastable lasers L1 and L2 through a fiber link. Fiber splitters are used to split and combine signals; AOMs are used to shift the carrier frequency by f_{off} and f_{drift} . The laser signals interfere on photodiodes PD1 and PD2, and the beat-notes are acquired with independent systems to extract the relative laser noise $\rho_2 - \rho_1$ and the fiber noise η . (a) Self-heterodyne detection. (b) Heterodyne detection.

The diode lasers are injected into single-mode optical fibers. Starting from L1, 5% of the laser light is split and used as local reference. The remainder 95% is sent to the remote location through the fiber. The link is 36-km long and covers both city and country areas, with a one-way light travel time of $\tau \simeq 180 \mu\text{s}$. At the remote location, the incoming light from L1 is split using a 50:50 coupler: half of the power is interfered with the L2 laser reference using a 50:50 coupler, the rest is routed back to the transmitting source, where it interferes with the L1 reference light. The light from L2 follows a symmetrical path.

An acousto-optic modulator (AOM) driven at $f_{\text{off}} = 40 \text{ MHz}$ is introduced on the fiber connecting L1 and L2, close to L1. Another AOM, driven at adjustable frequency f_{drift} , is placed at the L2 output, and it will be used as actuator for the carrier frequency drift correction.

The beat-notes are acquired on each side with high-speed photodiodes, PD1 and PD2. Two interference signals corresponding to two optical layouts are simultaneously present on each photodiode: self-heterodyne detection from the self-delayed interference of each laser and heterodyne detection from the interference between L1 and L2. In the self-heterodyne scheme the carrier frequency is determined by $f_{\text{off}} = 40 \text{ MHz}$. In the heterodyne configuration, each photodiode detects the beat-note between the reference signal and the incoming light from the remote laser: in our experiment, this is about 1.1 GHz. Accordingly, thanks to the spectral separation of the self-heterodyne and heterodyne beat-notes, the measurement scheme can be easily reconfigured to process one or the other by changing the LO frequency f_{LO} at the downconversion stages, i.e., to shift the RF signal of interest to the nominal frequency $\nu_0 = 1 \text{ MHz}$. The downconverted signals are acquired and demodulated by the respective measurement boards.

The optical phase is mainly affected by two kinds of noise contributions: the intrinsic noise of the laser sources, ρ_1 and ρ_2 , respectively, and the noise accumulated along the optical fiber link η , typically introduced by seismic or anthropic vibrations, acoustic noise, physical deformations, strains, and temperature variations. The measurement of these

noise signals for the two considered detection schemes will be discussed in the following paragraphs.

B. Self-Heterodyne Detection

Let us consider the self-heterodyne scheme of Fig. 6(a), where each laser interferes with its self-delayed light. The beat-notes at frequency f_{off} are downconverted to ν_0 using synthesizers set to $f_{\text{LO}} = 41$ MHz. In this configuration, the drift correction AOM is kept at fixed frequency, hence f_{drift} is neglected. The frequency fluctuations acquired by photodiodes PD1 and PD2 at the respective locations of L1 and L2 are

$$\Delta\nu_{1,A}(t_1) = \rho_1(t_1 - 2\tau) - \rho_1(t_1) + \eta_{12}|_{t_1-2\tau}^{t_1-\tau} + \eta_{21}|_{t_1-\tau}^{t_1} + \Delta f_{\text{off}}(t_1 - 2\tau) \quad (16a)$$

$$\Delta\nu_{2,A}(t_2) = \rho_2(t_2 - 2\tau) - \rho_2(t_2) + \eta_{21}|_{t_2-2\tau}^{t_2-\tau} + \eta_{12}|_{t_2-\tau}^{t_2} + \Delta f_{\text{off}}(t_2 - \tau). \quad (16b)$$

Here, t_1 and t_2 represent the local timescales, which are natively independent, $\rho_1(t_1)$ is the L1 laser frequency noise at time t_1 , and $\eta_{21}|_{t_1-\tau}^{t_1}$ is the one-way fiber frequency noise integrated over the path from L2 to L1 in the interval between $t_1 - \tau$ and t_1 , and correspondingly for the other terms. Δf_{off} is the AOM frequency deviation from its nominal value 40 MHz.

The acquisition timescales t_1 and t_2 are synchronized exploiting the triggering mechanism described in Section II-C2. A step frequency shift is imprinted on f_{off} , driven by the onboard synthesizer: the self-heterodyne beat-note at each terminal is momentarily shifted out of the detection band, and the resulting rising amplitude edge is used to trigger the two acquisitions. After the synchronization process, a fixed time relation can be established between the remote boards. This is defined as $t = t_1 - \tau = t_2$, where the relative delay τ accounts for the fact that the synchronizing pulse travels along the fiber before being detected at the other end. The variations in the propagation path delay are sufficiently smaller than the intrinsic synchronization uncertainty σ_{sync} , hence they can be ignored for the applications considered here. Therefore, after synchronization, the acquired signals are

$$\Delta\nu_{1,A}(t) = \rho_1(t - 2\tau) - \rho_1(t) + \eta_{12}|_{t-2\tau}^{t-\tau} + \eta_{21}|_{t-\tau}^t \quad (17a)$$

$$\Delta\nu_{2,A}(t) = \rho_2(t - 2\tau) - \rho_2(t) + \eta_{12}|_{t-\tau}^t + \eta_{21}|_{t-2\tau}^{t-\tau}. \quad (17b)$$

The AOM frequency fluctuations after the synchronization routine are considered negligible with respect to the other terms, and neglected through the rest of the analysis.

It can be assumed that to a first approximation, the laser noise cancels out, hence $\rho(t) \approx \rho(t - 2\tau)$, which is valid for frequency fluctuations with spectral components $f \ll 1/\tau$. With $\tau \simeq 180 \mu\text{s}$, this is justified for spectral analysis below 1-kHz Fourier frequency. Moreover, the phase perturbations η_{12} and η_{21} are expected to be mostly correlated, as the noise of the two fibers, laying in the same cable, is common to the first order. It follows that the interference signals are mostly affected by the common fiber noise $\eta \approx \eta_{12} \approx \eta_{21}$, and the round-trip frequency fluctuations can be approximated as follows:

$$\Delta\nu_{1,A}(t) \simeq 2\eta(t) \quad (18a)$$

$$\Delta\nu_{2,A}(t) \simeq 2\eta(t). \quad (18b)$$

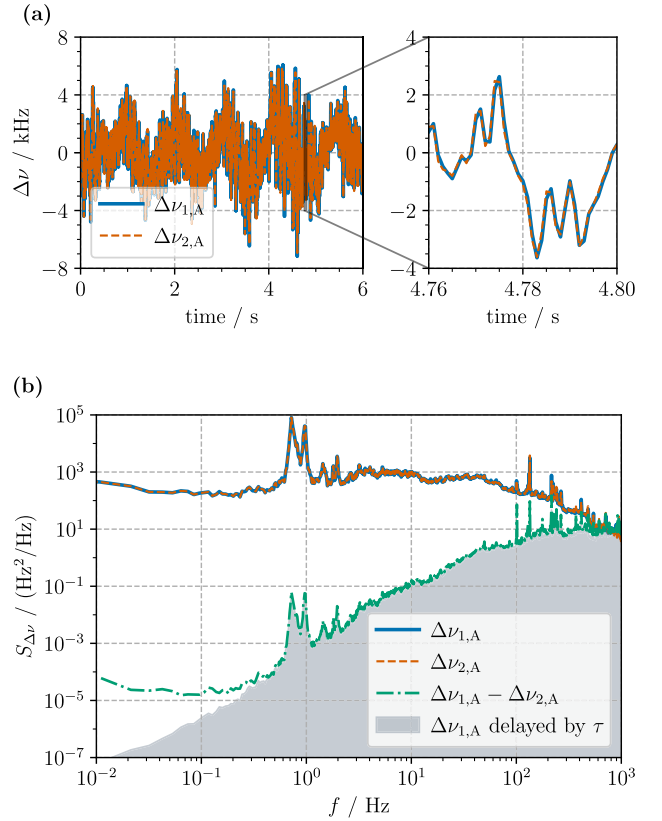


Fig. 7. (a) Synchronized acquisitions of frequency fluctuations over the optical fiber link, in the self-heterodyne interference scheme; the tracks mostly overlap. (b) PSD of the acquired signals; the noise spectrum of their difference is also shown, compared with the noise expected for a synchronization delay $\tau \simeq 180 \mu\text{s}$.

The degree of temporal correlation, as well as the quality of the synchronization process, can be appreciated from Fig. 7(a), showing the coincidence between frequency fluctuation signals acquired at 1 kHz by the two distant boards. Fig. 7(b) shows the PSD of the frequency noise for each of the two beat-notes, calculated for 50-min-long acquisitions. The spectra mostly overlap, since from (18) they refer to the same physical signals. The measurements are consistent with the noise expected for an urban fiber link, where the phase perturbations generated by different anthropic, seismic, oscillatory, or acoustic sources accumulate along the fiber path. Indeed, the measured white frequency noise level is compatible with other land-deployed cables reported in [33], [34], and [35], assuming a linear scaling of the noise PSD with the link length. Nevertheless, the actual scaling strongly depends on the specific deployment, which can cross data centers, bridges, buildings, and suspended fiber segments. The observation of daily fluctuations in the noise spectrum, 5–15 dB higher during the day compared with night, can be attributed to human activities, such as vehicle traffic along the roads adjacent to the fiber path. These aspects play an important role in applications where the dissemination of stable phase signals is required [36].

The spectrum of the difference between the two synchronized acquisitions is also shown in Fig. 7(b). The residual noise level that is observed for $\Delta\nu_{1,A} - \Delta\nu_{2,A}$ is consistent with the expectations for the difference between correlated, yet delayed, signals. Indeed, from (17), the acquisitions have

a relative delay equal to the light travel time τ , given by the synchronization procedure, and from [37], the spectrum of the round-trip fiber noise difference can be estimated as $(2\pi\tau f)^2 S_{\Delta\nu_{1,A}}(f)$, with $S_{\Delta\nu_{1,A}}(f)$ the PSD of $\Delta\nu_{1,A} \simeq \Delta\nu_{1,B}$ at Fourier frequency f . The measurement deviates from the expectations only at very low frequencies, where other effects emerge. We attribute this additional noise to optical length variations in the short fibers which are not common for the two paths.

C. Heterodyne Detection

In the heterodyne configuration, shown in Fig. 6(b), each local laser interferes with the light coming from the remote laser. The beat-notes between L1 and L2 are downconverted to ν_0 by setting f_{LO} to about 1.1 GHz. The AOM at f_{off} is driven at fixed frequency, hence it is neglected in this scheme. The optical carrier of L2 is shifted exploiting the AOM driven at f_{drift} by the onboard DDS, centered at 40 MHz, to correct the slow beat-note drifts that are due to uncorrelated length variations in the two optical cavities. Similar to the self-heterodyne case, in the heterodyne scheme the acquisitions are synchronized by imprinting a step frequency shift on f_{drift} , defining the common timescale $t = t_1 - \tau = t_2$. The following frequency fluctuations are expected to affect the PD1 and PD2 photodiode signals:

$$\Delta\nu_{1,B}(t) = \rho_2(t - \tau) - \rho_1(t) + \Delta f_{drift}(t - \tau) + \eta_{21}|_{t-\tau} \quad (19a)$$

$$\Delta\nu_{2,B}(t) = \rho_1(t - \tau) - \rho_2(t) - \Delta f_{drift}(t) + \eta_{12}|_{t-\tau}. \quad (19b)$$

The drift correction frequency results from the PID implemented in the MCU firmware, as described in Section II-B5. This tracks the low-frequency components of $\Delta\nu_{2,B}$, with a LPF cutoff of 0.01 Hz. In that spectral region, the relative drift between the independent lasers L1 and L2 dominates, hence Δf_{drift} mainly follows the low-frequency components of $\rho_1 - \rho_2$. Due to symmetry, any frequency offset cancels out for both $\Delta\nu_{1,B}$ and $\Delta\nu_{2,B}$.

Although in metrology the fiber link noise represents a limit for the comparison of optical frequency references and requires phase stabilization techniques [36], from a different perspective the fiber can be used as a sensor for earthquakes and other geophysical events occurring close to the fiber [9]. With the heterodyne scheme, the reference laser and fiber noise contributions can be distinguished. Under the same assumptions introduced for (18), the approximated frequency fluctuations on the two photodiodes become

$$\Delta\nu_{1,B}(t) \simeq \rho_2(t) - \rho_1(t) + \Delta f_{drift}(t) + \eta(t) \quad (20a)$$

$$\Delta\nu_{2,B}(t) \simeq \rho_1(t) - \rho_2(t) - \Delta f_{drift}(t) + \eta(t). \quad (20b)$$

It follows that from the combination of $\Delta\nu_{1,B}$ and $\Delta\nu_{2,B}$, it is possible to extract the fiber noise

$$\Delta\nu_{1,B}(t) + \Delta\nu_{2,B}(t) \simeq 2\eta(t) \quad (21)$$

and the relative laser noise

$$\Delta\nu_{1,B}(t) - \Delta\nu_{2,B}(t) - 2\Delta f_{drift}(t) \simeq 2(\rho_2(t) - \rho_1(t)). \quad (22)$$

The effects of frequency drifts can be seen from Fig. 8(a). Without activating the drift correction, $\Delta\nu_{1,B}$ and $\Delta\nu_{2,B}$ show

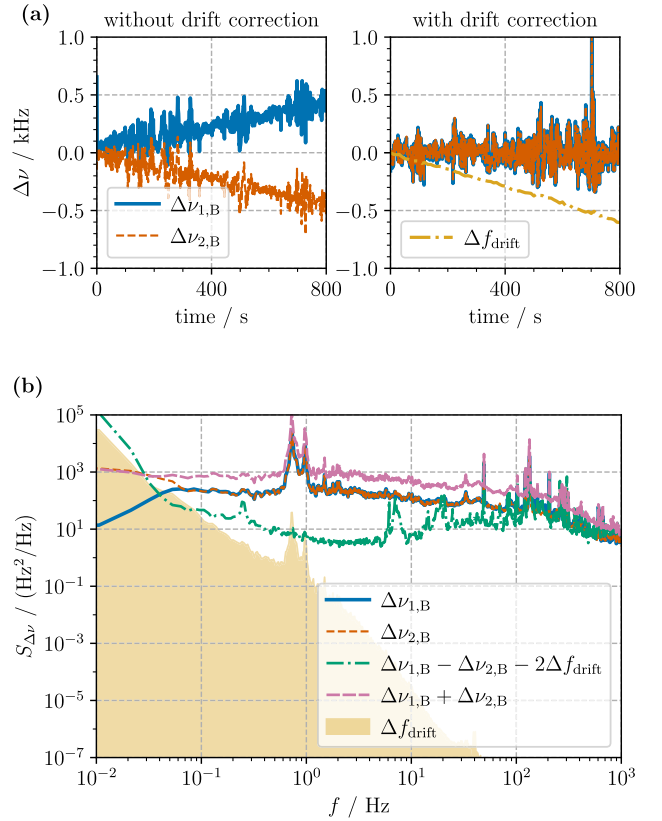


Fig. 8. (a) Synchronized acquisitions of frequency fluctuations over the optical fiber link, in the heterodyne interference scheme, without and with frequency drift correction; with drift correction the tracks mostly overlap. (b) PSD of the acquired signals, with drift correction; the noise spectra of their sum and difference are also reported.

significant offsets, variable in time. When the drift correction is enabled, the synchronized tracks are characterized by fast frequency fluctuations that lay around zero, with the low-frequency drift being tracked by Δf_{drift} .

The PSDs of the acquired signals is shown in Fig. 8(b), mostly overlapping except at low frequencies, where Δf_{drift} dominates. $\Delta\nu_{1,B}$ and $\Delta\nu_{2,B}$ are combined to show either the fiber noise or the relative laser frequency noise using (21) and (22). It can be seen that the fiber noise represents the main contribution in the measurements for our setup, and that it is similar to the self-heterodyne results presented in Fig. 7(b). The measured laser noise is consistent with the expectations for ultrastable sources [38], noting that the lasers are installed in suboptimal conditions, outside a laboratory and subject to environmental disturbances. For example, some acoustic spurs are present above 10 Hz, likely given by cooling fans close to the setups. The laser noise dominates at very low frequencies below 0.1 Hz, where the laser drift is compensated by the frequency drift correction.

V. CONCLUSION

In the current work, a phase-sensitive detector has been designed and implemented on a MCU. Dedicated electronic and firmware platforms have been realized and characterized. Following the approach of digital lock-in amplifiers, the system implements efficient algorithms for phase and amplitude heterodyne demodulation of RF signals downconverted

to 1 MHz. An output data rate of 20 kHz can be achieved, with a reconfigurable demodulation bandwidth between 1.25 and 12.5 kHz. The input frequency deviation from the 1-MHz carrier can be measured over almost ten orders of magnitude, from a few μHz up to 50 kHz. The accepted input signal amplitude spans over more than 3 voltage decades. Frequency instability at 1 s is about 10 μHz , and amplitude accuracy is better than 1 mV. A stable quartz oscillator is embedded as frequency reference for deployable operation.

The acquisition system is mainly designed for the demodulation of phase signals from coherent optical interferometry, hence for measurements of the optical carrier frequency. Its characterization confirmed that the board performances are suitable for the analysis of optical frequency signals. Taking advantage of the optical-to-rf leveraging, the relative impact of the reported frequency measurement errors is of the order of 10^{-19} , which is appropriate for many applications that do not require optical-clock-level accuracy. Notably, the operation principle provides this platform with all the typical advantages of a phase analyzer over, e.g., frequency counters. These include, among others, high sampling rates, intrinsically dead-time-free measurements, and well-defined user-selectable bandwidth. Moreover, the phase measurement is combined with amplitude demodulation as in lock-in amplifiers, allowing to monitor the dynamic evolution of the carrier strength and synchronization capabilities.

An in-field demonstration of remote fiber sensing using distant ultrastable laser sources has been performed. The optical phase was acquired as carrier frequency fluctuations exploiting the self-heterodyne and heterodyne interferometric schemes, allowing to measure the relative noise of the laser sources and the fiber link noise.

Compared with commercial benchtop systems or FPGAs, the presented system is characterized by higher flexibility, stand-alone operation, simpler architecture, compact footprint, and much lower costs. It allows for real-time and continuous monitoring applications, supporting wide ranges of amplitude and frequency of the input signal. The embedded triggering mechanism permits to synchronize distant boards at the level of a few μs without requiring additional channels or protocols, and allowing quantitative signal comparisons and correlation analysis. The DSP algorithm optimization enables high performances also on a cheap and reliable MCU. The platform represents an efficient possibility in deployable long-term experiments. Particularly interesting applications are related to fiber noise sensing, such as for earthquake monitoring, or metrological comparisons of distant laser sources using optical interferometry.

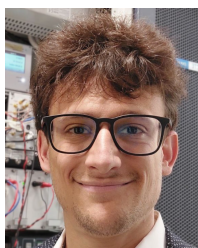
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