Stable Voltage Generation With a Josephson Voltage Standard Device Cooled at a 4 K Stage in a Dilution Refrigerator

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***Abstract*— We have demonstrated voltage generation in a dilution refrigerator using a Josephson voltage standard (JVS). A niobium-nitride (NbN)-based superconductor-normal metal-superconductor Josephson junction (JJ) array was placed hung directly under the 4 K stage of the dilution refrigerator. The thermal design of wiring was optimized to achieve stable operation of the JVS and temperature stability of the 4 K stage. After that, we measured the flatness of the quantized voltage steps. We obtained the combined relative uncertainty of 2.4 × 10^{-10} V/V within 40 min of accumulation and 2.1 × 10^{-8} V/V within 13 h of accumulation for 1028 and 2 mV generation, respectively.**

***Index Terms*— Dilution refrigerator, Josephson voltage standard (JVS), precise voltage measurement, thermal design, voltage reference.**

I. Introduction

JOSEPHSON voltage standards (JVSs) are used for supplying primary reference standards of voltage [1], [2], [3], [4], [5] because they can generate essentially stable voltage guaranteed by quantum mechanics. Based on the Josephson effect [6], the voltage value on the first Shapiro step is represented by the following equation:

$$V = \frac{h}{2e} N_{\mathrm{JJ}} f \tag{1}$$

where h is Planck's constant, e is the elementary charge, N_{JJ} is the number of Josephson junctions (JJs), and f is the microwave frequency applied to the JJs [7].

To generate quantum voltages by JVS with small uncertainty such as nV/V order or better, stable and appropriate temperature and low-noise environment and well-selected/adjusted electrical wirings for their operation are necessary. For usual JVSs, the devices themselves are mounted inside a dedicated cryostat cooled with liquid helium or a mechanical cooler, such as a Gifford McMahon cooler, to achieve suitable temperature [8], [9], [10], [11].

On the other hand, various experiments have been performed under cryogenic environments inside dilution refrigerators, such as the observation of a physical phenomenon below 1 K [12] and in the 10 mK range [13], developments of cryogenic voltage reference for electronic subsystems in close proximity to qubits using complementary metal oxide semiconductors (CMOSs) or Cryo-CMOSs [14], shot noise measurements using a high-electron-mobility-transistor (HEMT)-based cryogenic amplifier [15], and quantum metrology triangle experiments to realize mutual verification of the validity of quantum electrical standards based on the three quantum phenomena (Josephson effect, quantum Hall effect, and single electron tunneling effect) via Ohm's law [16], [17], [18], [19], [20]. Though the use of a JVS as a voltage reference in such experiments is appealing, the voltage errors due to large thermal electromotive force (emf) noise and other electrical noises are unavoidable as long as an independent cryostat of JVS system is used. One way to address this problem is to implement a JVS directly in a dilution refrigerator. Howe et al. [21] demonstrated qubit control using a pulse-driven JVS located at 3 K stage of a dilution refrigerator. In this study, we aim to implement a programmable JVS (PJVS) device in a dilution refrigerator as a cryogenic voltage reference in the range of 1 mV–1 V. The main challenges of installation of a PJVS module inside a dilution refrigerator are heat control of the module, heat-transfer design for wirings, and precise evaluation of the output voltage.

At the National Institute of Advanced Industrial Science and Technology (AIST), niobium-nitride (NbN)-based superconductor-normal metal-superconductor JJ array PJVS chips which are driven at around 10 K have been developed for the primary and practical dc voltage standards for calibration [11], [22], [23]. Note that the superconducting transition temperature of NbN is 16 K. Given the technology, we intend to realize a voltage reference by our PJVS chip in a dilution refrigerator under the operation condition of the circulation of ^{3}He/^{4}He mixture. Progress on the initial phase of this study has already been reported [24], [25]. This article reports detailed information and improved results on the thermal design and precise voltage measurement. In Section II, we describe the schematic of wiring of the PJVS module and operating system of it. Then, we report the optimization results of a heat balance between heat transfer from the wiring and cooling power of the dilution refrigerator. In Section III, we report the results of the optimization of operation conditions by changing microwave frequency and power as well as the evaluation of voltage accuracy by measuring the flatness of the first Shapiro steps.

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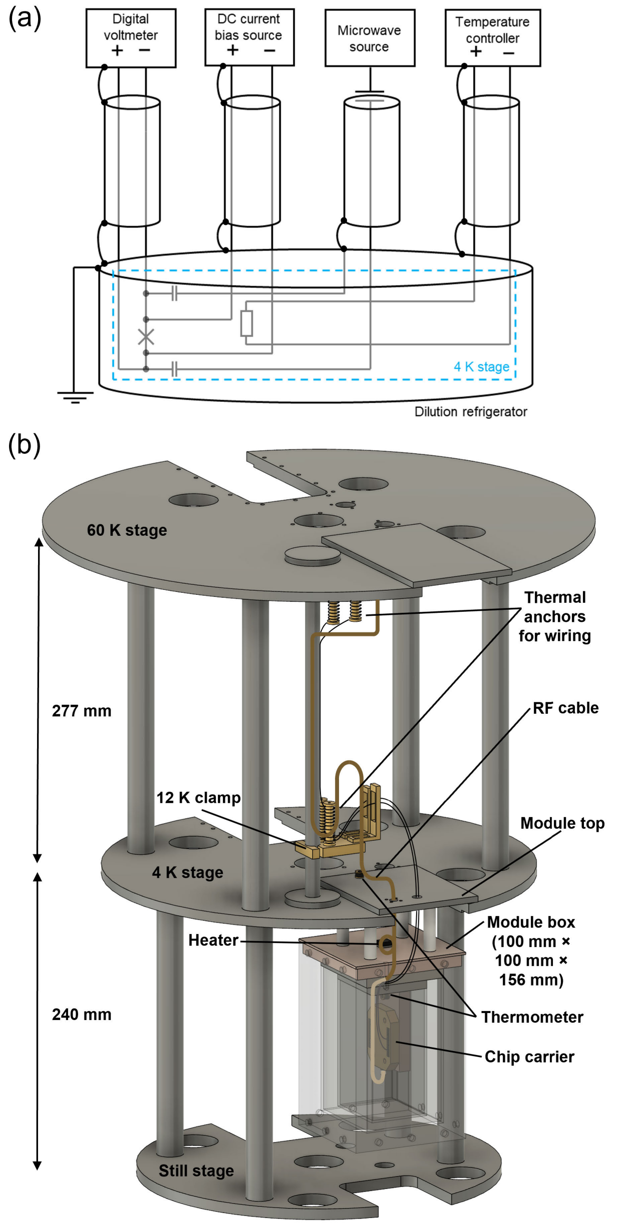

Fig. 1. (a) Block diagram of an operating system for generating quantized voltage using the PJVS module with the dilution refrigerator. The cross and rectangle indicate JJs and heater resistance, respectively. (b) Schematic of cooling stages and wiring around the PJVS module in the dilution refrigerator with a total height of ∼1.5 m. Two thermal anchors for wiring are placed on the 60 K stage and 12 K clamp.

II. Design and Optimization of PJVS Module

A. Installation of PJVS Module

Fig. 1(a) shows a block diagram of an operating system for generating a quantized voltage using the PJVS module, described in Introduction in the dilution refrigerator. In this system, a digital voltmeter (DVM, *Keysight 34420A*) as a null detector, a dc current bias source for the PJVS (custom-made), a microwave source (*Keysight E8257D*), a temperature monitor/controller (*Lake Shore Cryotronics Model 335*), and a heater (*Nikkohm RNP-50U C25 ohm FZ00*) are used.[1] As described in Fig. 1(a), the outer conductors of all cables in this setup are grounded to the same point through the top of the dilution refrigerator. The optimum temperature for generating quantized voltage with the chip used in this system is ∼12 K. Fig. 1(b) shows a schematic of wiring around the PJVS module in the dilution refrigerator. As illustrated in the figure, two thermometers are placed near the chip carrier and at the top of the module. The heater placed on the top of the module box is used for temperature regulation. Two thermal anchors are placed on the 60 K stage and on the 12 K clamp. The size of the module box is 100 mm in length, 100 mm in width, and 156 mm in height. Wiring from the 60 K stage to the module is thermally anchored at the 12 K clamp and passes through the hole thermally isolated by a glass-epoxy shield on the module top to reduce the heat inflow from the room temperature to 4 K stage. An RF cable is attached on a support of the dilution refrigerator, and then passes through the hole, which is thermally isolated by a plastic washer on the module top.

[1]Equipment model numbers and manufacture names are provided to identify experimental procedures. These statements are not intended as endorsements by the authors.

TABLE I
Heat Transfer From Wiring Calculated With Setpoint of 12 K

Factor	Heat inflow (mW)	DC : Joule heating / AC : Power consumption (mW)	
		N_{JJ} = 32 768 (1028 mV)	N_{JJ} = 32 (1 mV)
Bias line (DC)	0.824	3.79	0.47
Thermometer line (DC)	0.366	0.03	0.03
Voltage line (DC)	5.040	0.00	0.00
Heater line (DC)	2.397	0.02	0.04
Josephson device (DC)		7.56	< 0.01
Heater (DC)		1.51	3.36
RF line/signal (AC)	17.118	103.00*	103.00*
Total	25.75	115.9	106.9

* This value corresponds to total power consumption including dielectric losses. RF power input through the coaxial cable is converted to heat in the PJVS chip. Microwave power in this case is 66.45 mW.

B. Optimization of Heat Transfer

To minimize the heat load to the 4 K stage of the refrigerator, we first calculated the heat inflow through the wiring and the Joule heating from each component for driving the PJVS device. Our previous calculations were based on the use of copper for all wirings, resulting in a large heat inflow [26]. In this study, we optimized the wiring materials to balance the heat inflow and the Joule heating. The calculation assumes PJVS outputs of 1028 and 1 mV (corresponding to $N_{JJ} = 32\,768$ and 32, respectively, and $f = 15.17705784$ GHz).

Table I shows the result of the calculation of heat transfer. To reduce the heat inflow from room temperature, the thermal conductivity of each component should be sufficiently low. However, materials with low thermal conductivity also have low electrical conductivity, generating large Joule heat when an electrical current is applied. After the optimization of this trade-off, we selected phosphor bronze as a wiring material of the lines for bias currents (18 pcs), thermometers (8 pcs), and heaters (2 pcs) while a beryllium copper semi-rigid cable was selected for the RF line. For the voltage line, two copper wires were employed to achieve low voltage noise. It can be seen

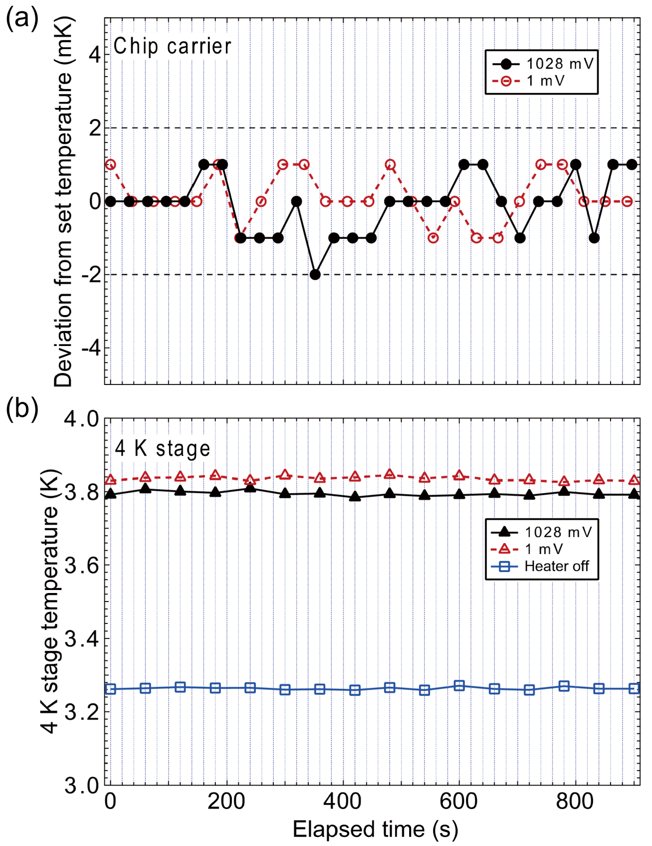

Fig. 2. (a) Deviation from a set temperature of 12.1 K during the measurement of voltage generation. Black solid circles and red open circles correspond to 1028 and 1 mV output, respectively. (b) 4 K stage temperature during the measurement of voltage generation and when the heater power is turned off. Black solid triangles, red open triangles, and blue open squares correspond to 1028, 1 mV output, and heater off condition, respectively.

from Table I that the major contribution is power consumption in the RF line (103.00 mW). The total values of heat transfer are 141.65 for 1028 mV output and 132.65 for 1 mV output. Note that Joule heating from the Josephson device at 1028 mV output is greater than that at 1 mV output. In contrast, the heating value required by the heater to maintain the setpoint of 12.1 K at 1 mV output is larger than that at 1028 mV output. The cooling power of the 4 K stage is ~1.3 W, which means that the refrigerator has enough room for the simultaneous operation of the PJVS module and other devices.

Using the optimized wiring, we then tested the temperature stability of the chip carrier and the 4 K stage. Fig. 2 shows the measured temperature fluctuation at the stages. We confirmed that the temperature deviation at the chip carrier was within ±2 mK and no considerable temperature deviation of the 4 K stage under 1028 and 1 mV outputs. Though the temperature of the 4 K stage increases by ~500 mK compared with that without operation of the PJVS module because of the heat transfer from that, the temperature is still kept below 4 K. From our experience in the PJVS operation in a primary standard system, it is known that the allowable temperature deviation of the PJVS chip is within ±50 mK for 10 V generation with 10 nV order uncertainty [11]. The results in Fig. 2 meet this criterion.

III. Generation of Quantized Voltage

A. Optimization of Operation Conditions

Our PJVS chip is composed of 65 536 NbN-based JJs and divided into 16 segments connected in series [22]. Each segment is assigned a channel number from Ch 1–16, and the number of junctions are binary from $N_{\text{JJ}} = 32$ (Ch 1 and 2) to 8192 (Ch 10–16 are the same). This corresponds to the voltage generation of 1 mV (Ch 1) to 257 mV (Ch 10) when a 15.1 GHz microwave and an appropriate dc bias current are applied to the corresponding channel.

To conduct proper operation of the PJVS, we measured the dependence of regions of bias currents where the voltage is constant in current-voltage characteristics (bias margin) on microwave frequency and power (Fig. 3). Microwave power changed from 26.5 to 74.6 mW (every 0.5 to 2 dB) at frequencies from 14.8 to 15.5 GHz (every 100 MHz). To decide the bias margin, we set the threshold value of 0.02 mV/mA in the differential resistance measured for applied currents. The bias margin for 1 mV output widened with increasing microwave power, reaching 2.2 mA at 15.0 GHz and 66.5 mW [Fig. 3(a)]. The bias margin for 1028 mV output also widened with microwave power, reaching 1.0 mA at 15.2 GHz and 70.0 mW [Fig. 3(b)]. At 74.6 mW [corresponds to 115.57 mW of RF signal (ac)] in the 1028 mV output, the temperature stability of the module was lost because the heater power reached 0%, meaning that the RF power consumption was too much to maintain the set temperature. Therefore, we can estimate the cooling power of the PJVS module to be 152.69 mW. Considering these results, the optimized measurement conditions were decided to be 15.17705784 GHz and 66.45 mW at 12.1 K.

Fig. 4(a) shows the current-voltage characteristics for the channel combinations corresponding to the 1028 and 1 mV outputs. Fig. 4(b) shows the bias margin for obtaining the quantized voltage in each channel measured at 12.1 K with the optimized measurement conditions. We confirmed existing of bias margin of more than 0.5 mA in all channels required for quantized voltage generation of 1 mV to 2 V.

B. Evaluation of Voltage Accuracy

To precisely validate the quantization of the voltage generated in the PJVS chip, we evaluated a flatness of the first Shapiro steps in a back-to-back configuration [8], [27], according to the following procedures:

1) Make two groups of channels, such that their nominal voltages (numbers of JJs (N_{JJ})) are the same (e.g., Ch 1–10: 514 mV versus Ch 11 and 12: 514 mV).
2) One group is biased positively (resp. negatively), and the other is set negatively (resp. positively), e.g., Ch 1–10: 7.3 mA versus Ch 11 and 12: −7.3 mA. In addition, apply an optimized microwave signal to the chip.
3) Measure the output voltage from the PJVS chip using the null detector, which is supposed to be zero (except for the external offsets, such as voltmeter offset and thermal emf in the wires), given the canceled-out quantized voltages due to the oppositely-biased two groups with the same number of JJs. Then, reverse the polarities, measure the voltage again, and obtain their absolute

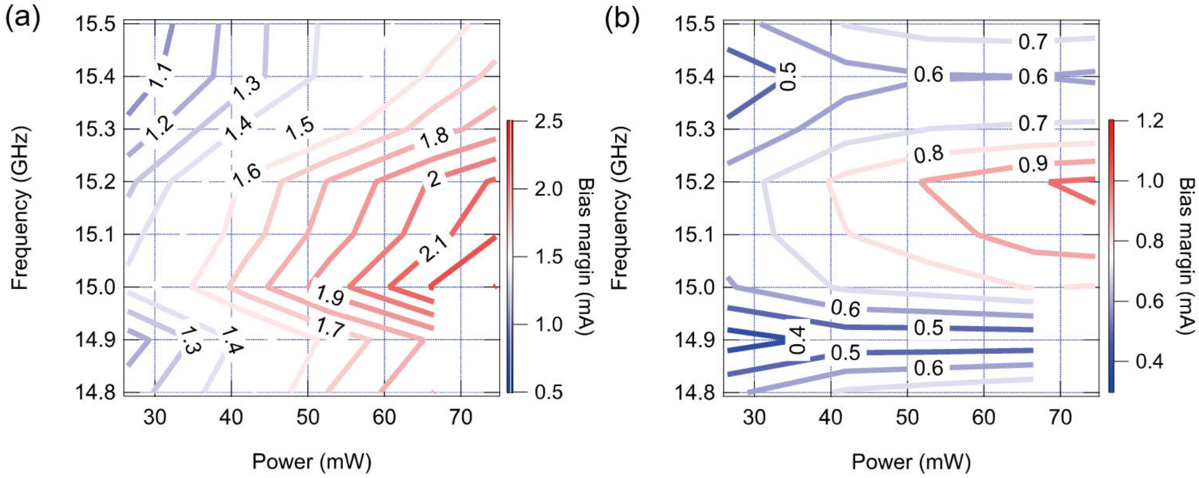

Fig. 3. Dependences of bias margin on microwave frequency and power at 12.1 K. Each value on the contour line indicates the step height (bias margin) at the first Shapiro steps for (a) 1 and (b) 1028 mV. Note that there are no data points above 66.5 mW at 14.8 and 14.9 GHz.

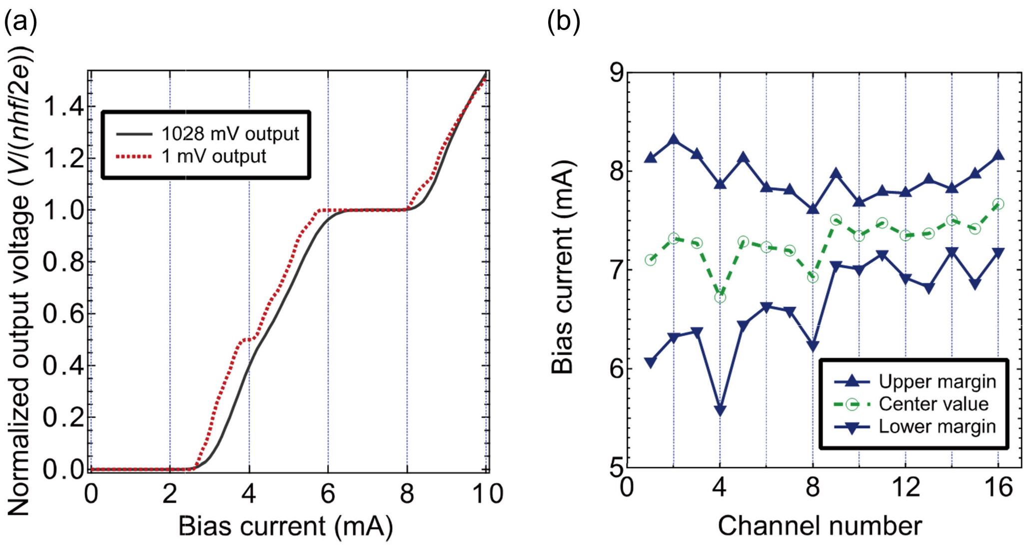

Fig. 4. (a) Current-voltage characteristics measured with microwave irradiation for 1028 mV (black solid line) and 1 mV (red dotted line) outputs. Each value of the measured voltage was normalized with the theoretical value of the first Shapiro step from Josephson's (1). (b) Bias margin for obtaining the quantized voltage in each channel measured at 12.1 K with the optimized measurement conditions (15.17705784 GHz and 66.45 mW).

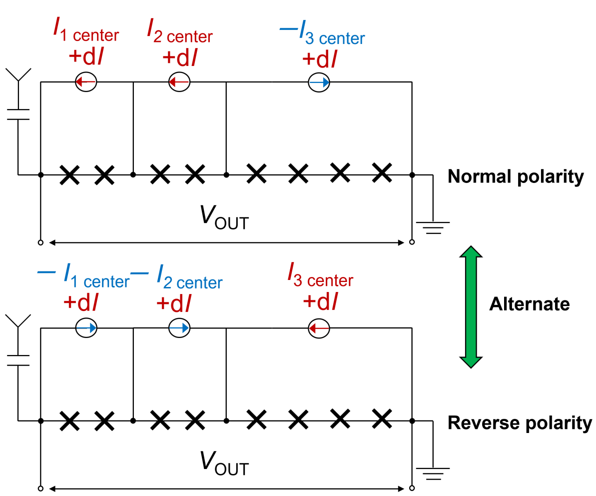

Fig. 5. Schematic equivalent circuit diagram of a back-to-back measurement. $I_{1\,\mathrm{center}}$–$I_{3\,\mathrm{center}}$ and dI indicate center values of bias margins [cf. Fig. 4(b)] and dither current (the offset currents from step centers), respectively [27].

average value as data to evaluate the external offsets (Fig. 5).

4) Repeat Step 3) along with applying the dither current (the offset currents from step centers). If the current-setting position is out of the Shapiro step, a finite residual voltage is detected by the null detector.

Fig. 6(a) shows the measurement results for the output settings of 514 versus 514 mV (total: 1028 mV) and 1 versus 1 mV (total: 2 mV) in the dither current range of ±1.0 mA. From these results, we confirmed the proper quantization of the output voltage within a measurement noise level of ±5 nV for both channel settings. The current widths of the flat regions are ±0.1 and ±0.6 mA for 1028 and 2 mV outputs, respectively.

To obtain precise information on uncertainty in voltage generation, long-time data accumulation was performed for the points in the quantized region via back-to-back measurements. Fig. 6(b) shows the results obtained at three points (dither current of 0 and ±20 μA). As the setting resolution of bias current is 5 μA, these data points are guaranteed no overlapping of bias currents. To avoid the effect of time-dependent drift of the voltage offsets due to thermal emf, the measurement was performed while changing the bias polarities in the sequence of positive, negative, negative, and positive.

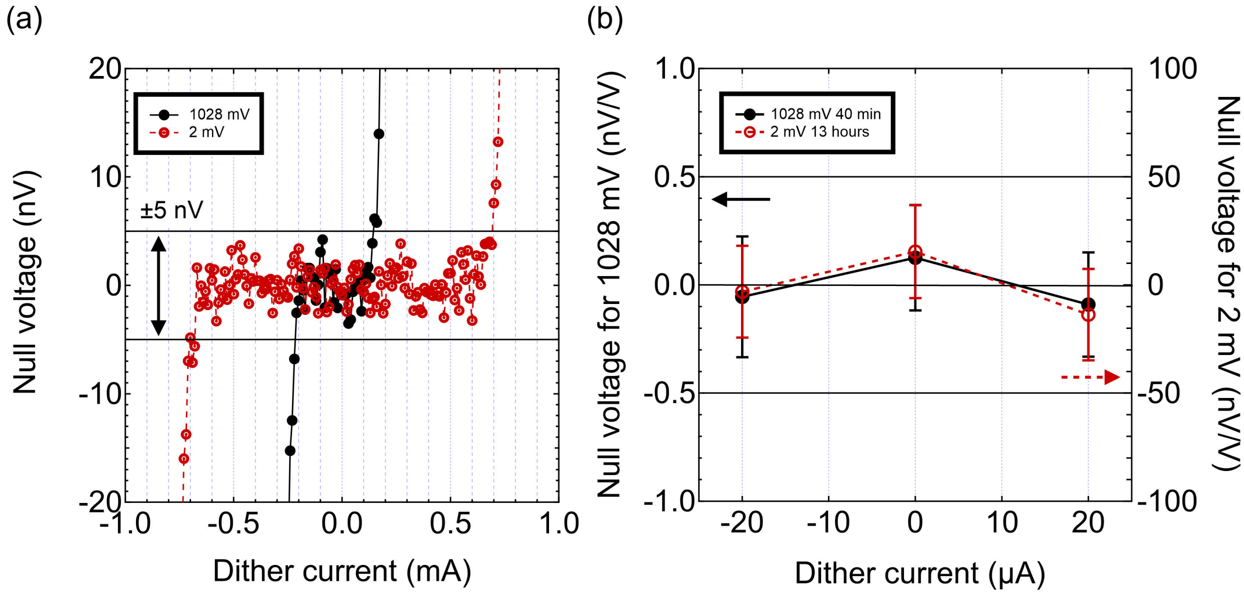

Fig. 6. Results of back-to-back measurements for checking the flatness of the first Shapiro steps. Dither current indicates the offset currents from the bias center of the first Shapiro step. Black solid circles correspond to the total 1028 mV output (−514 versus 514 mV) and red open circles correspond to the total 2 mV output (−1 versus 1 mV). (a) Raw data plotted in the current range of ±1.0 mA. (b) Averaged data in the range of ±20 μA by accumulating each data point from 40 min to 13 h. The error bars indicate the relative standard uncertainty as evaluated in Table II.

TABLE II
UNCERTAINTY BUDGET FOR GENERATION OF QUANTIZED VOLTAGE

Factor	Type	Standard uncertainty N_{JJ} = 32 768 (1028 mV)	Standard uncertainty N_{JJ} = 64 (2 mV)
Standard deviation of the mean	A	0.247 nV	0.032 nV
DVM resolution	B	0.029 nV	0.029 nV
Microwave frequency	B	0.031 nV	0.000 nV
Combined uncertainty		0.251 nV	0.043 nV
Relative uncertainty		2.4×10^{-10} V/V	2.1×10^{-8} V/V

Repeating this sequence, we accumulated the data for 40 min and 13 h for 1028 and 2 mV outputs, respectively. The error bars shown in Fig. 6(b) indicate the relative standard uncertainties listed in Table II. Relative uncertainty was calculated by dividing combined standard uncertainty by the output voltage (theoretical value).

In Fig. 6(b), we confirmed the excellent flatness of the quantized steps with the uncertainty of 2.4×10^{-10} and 2.1×10^{-8} for 1028 and 2 mV outputs, respectively. The major contributions are due to null voltage measurement (i.e., the standard deviation of the mean and the DVM resolution). It is expected that the measurement uncertainty can be improved using voltmeters with a higher resolution, particularly for the 2 mV output. During the measurement, the temperature deviation was within ±2 mK, thus maintaining a stable temperature as shown in Fig. 2. Additionally, even under the PJVS voltage generation, the base temperature reached near 20 mK at a mixing chamber plate of the dilution refrigerator.

IV. CONCLUSION

We conducted voltage generation with a PJVS device cooled at a 4 K stage in a dilution refrigerator. For temperature stabilization and reduction of heat load to the 4 K stage, we optimized the thermal design of the wiring and structure of the PJVS module for its stable operation. In voltage generation of 1028 and 1 mV, we have confirmed temperature stability within ±2 mK and no significant temperature deviation of the 4 K stage. We also evaluated the uncertainty of voltage generation of 1028 and 2 mV in optimized conditions. After the accumulation of data for 40 min and 13 h, the relative standard uncertainty was evaluated to be 2.4×10^{-10} V/V and 2.1×10^{-8} V/V for 1028 and 2 mV outputs, respectively. We emphasize that all experiments using PJVS were performed under the full operation of circulation of mixture of the dilution refrigerator. Even under the voltage generation of the PJVS, the base temperature was near 20 mK at a mixing chamber plate of the dilution refrigerator, which is the base temperature without the PJVS. This means that our PJVS can be utilized as a precise reference voltage generator placed in a cryogenic environment of a dilution refrigerator.

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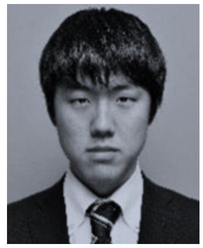

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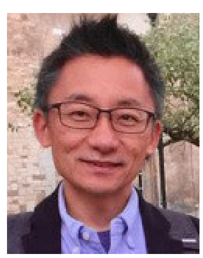

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