Simplifying Capacitive Sensor Readout Using a New Direct Interface Circuit

José A. Hidalgo-López and Julián Castellanos-Ramos

***Abstract*— Direct interface circuits (DICs) are efficient for reading resistive, capacitive, or inductive sensors in a digital format. The simplest DICs consist of just a few passive elements that connect a digital processor (DP) to a sensor. When reading capacitive sensors, one or several calibration capacitors and/or several charging and discharging cycles are needed to make the estimation, and the result usually requires complex arithmetic operations. This article presents a new type of capacitive DIC that is simple in terms of hardware, needing only two resistors of known value and the DP in order to make the capacitance estimation. In addition, the reading method requires a single sensor charging and discharging cycle, which reduces acquisition time and power consumption. Two time measurements are taken during the discharge, which, through a linear transformation of their subtraction (using two constants stored in the DP), give the value of the capacitance. These arithmetic operations are easily implemented on any DP and consume fewer resources than the divisions required on other capacitive DICs. The design has been tested for a wide range of capacitances (from 100 pF to 561 nF), including the value of several capacitive sensors. The average relative error for the entire range is 0.41%, the linearity errors are below 0.3%, and the minimum signal-to-noise ratio (SNR) value is 64 dB.**

***Index Terms*— Capacitance to digital, capacitive sensors, direct interface circuits (DICs).**

I. Introduction

CAPACITIVE effect sensors are based on variations in capacitance due to changes in the charge storage processes, the capacitor's dielectric, or its dimensions (area or thickness). Such sensors can be classified into two groups: floating sensors (where none of the electrodes need to be grounded to function properly) or grounded sensors (due to sensor manufacturing processes, one of the terminals must be connected to the ground). Grounded capacitive sensors generally present greater problems related to stray capacitors. However, their use is unavoidable in many applications (such as for level measurement of a conductive liquid or the distance/proximity measurement to a grounded metallic object). In other cases, they must be used for safety and/or operating limitations of floating capacitive sensors [1].

In general, a capacitive effect sensor has impedance in the Laplace domain

$$Z = 1/Cs^{\alpha_f} \tag{1}$$

where $-1 \leq \alpha_f \leq 1$. If α_f is different from one, these sensors are called in the literature constant phase sensors (CPSs). CPS is of increasing importance in the control of various physiological processes [2], monitoring microbial growth [3], or food adulteration [4].

However, the name of capacitive sensor is reserved for those in which $\alpha_f = 1$ and is the most widely used to measure physical and chemical parameters. Measurements made with these capacitive sensors include liquid levels [5], pressure [6], strain [7], humidity [8], and organic substance analysis [9]. Sensor capacitance in such applications varies from tens of picofarads to just a few nanofarads. Furthermore, interesting new applications have recently been proposed for this type of sensor, such as DNA detection [10], position and displacement [11], dew point measurement [12], water in crude oil [13], and sensing hemolysis [14], where capacitance varies in a wide range, from hundreds of picofarads to hundreds of nanofarads.

Nowadays, capacitive sensors are often designed as smart sensors that include additional blocks, such as conditioning circuits with operational amplifiers (OAs), analog-to-digital converters (ADCs), and digital processors (DPs) with communication interfaces. The DP performs more or less complex local processing of the information provided in a digital format by the ADC, transmitting the parameters obtained to a higher unit, thus reducing its workload. These capacitive smart sensors have become widespread as portable devices that can increasingly be part of wireless networks. This means that the readout circuit designs for these sensors are becoming more and more demanding, both in terms of the cost of the device (the number of elements used and their complexity) and power consumption [15].

To meet these needs, this article introduces a new grounded capacitive sensor readout circuit that minimizes the hardware required by using a new direct interface circuit (DIC) with only passive components. Therefore, the estimate of the sensor capacitance, C_X, does not need ADCs, OAs, analog comparators, or voltage references. The new DIC is very simple since, in addition to C_X, only two resistors of known value are used, avoiding the need for calibration capacitors and reducing hardware requirements and size. The estimation uses just two time measurements, obtained during the only discharging

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process. A single discharging process reduces both acquisition time and energy consumption. The arithmetic operations in calculating C_X are simple and easily implementable in the DP, thus freeing up resources. Despite the simplicity of the proposal, the error in the estimation of C_X is lower than that of other more complex readout circuits. These results are obtained for a much larger range of capacities, allowing the new DIC to be used in applications where it was impossible to use this type of circuit until now, as in [9], [10], [12], [13], and [14].

II. State of the Art

Capacitors are energy storage elements. Thus, whatever the method chosen to measure its capacitance, measurements related to time intervals are necessary for its determination. One type of circuit makes these measurements indirectly by estimating the frequency or magnitude of a given periodic output signal. Other circuits make time measurements directly in the charging–discharging processes of the capacitors.

Among the first type of circuits, some use analog blocks to perform the readout of capacitive sensors. In [16], an RLC resonant circuit has been used to convert the capacitance variation of an angular position sensor into a voltage. The maximum angular position error is about 6%. In [17], oscillation periods of a relaxation oscillator consisting of an OA-based integrator and a comparator are used for capacitance measurements. Measuring the time in which the output signal is in each of the two possible states allows us to determine the value of C_X. The system enables measurements in the range of 1–100 pF with errors of 3%.

Another circuit with a similar operating principle and using OAs is presented in [18]. The circuit needs an ac sinusoidal signal and a triangular reference signal. These elements mean high power consumption, around 140 mW; however, the circuit presents a maximum nonlinearity error (NLE) of only 0.7% for C_X in the range of 200–300 pF. The readout circuit in [19] comprises an active capacitive bridge and a relaxation oscillator to convert capacitance changes into frequency. The circuit uses two OAs, along with several additional capacitors and resistors. Error in determining C_X varies between 1% and 2.3%.

To reduce power consumption in [20], OAs are replaced with a switched-capacitor amplifier. The circuit also needs a calibration capacitor and several switches. Two-step autocalibration is applied to eliminate the offset from nonideal effects of the switched-capacitor amplifier and comparator. The capacitive sensor ranging from 8 to 12 pF can achieve 10.4-bit resolution while consuming only 3 μW during 640 μs conversion time. A similar solution is used in [21] for a micro-g accelerometer.

Another capacitance-to-digital converter based on the switched-capacitor integrating technique is presented in [22]. This implementation shows a maximum 0.08% full-scale range (FSR) error when measuring capacitances in the interval 10–400 pF. Again, the circuit uses an OA, a comparator, various switches, and capacitors for calibration. In [23], with the same switched-capacitor integrating technique but replacing

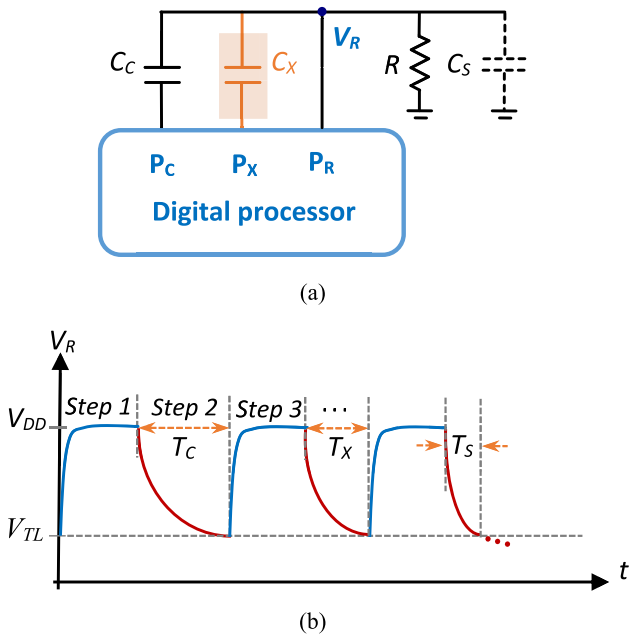

Fig. 1. DIC for the readout of capacitive sensors in [25]. (a) Circuit and (b) time evolution of the signal to be measured.

OAs with a successive approximation register (SAR), capacitive sensors in the range of 1–3.6 pF are measured with a sampling clock of 18.51 kHz. In [24], a novel closed-loop switched-capacitor circuit for capacitance-to-frequency converter (CFC) is presented with a maximum NLE of 0.24%.

Apart from a variable number of analog blocks, another drawback of these circuits is the long normalized acquisition time, defined as the quotient between the maximum acquisition time and the maximum value of C_X. For example, in [23], this figure of merit reaches 255 ms/nF (one of the lowest values for these types of circuits).

In a different approach, DICs connect the sensor directly to a DP (mainly a microcontroller, μC) to reduce the number of circuit components, power consumption, and acquisition time. Capacitance-to-digital conversion in a DIC is performed without any external circuit for signal conditioning or ADC, adding just a few passive elements, meaning that DICs are compact and inexpensive. Based on this design philosophy, Reverter et al. [25] and Reverter and Casas [26] used a calibration capacitor and a resistor, in addition to the sensor, to build the complete readout circuit, see Fig. 1(a).

The reading procedure consists of a charging and discharging process for each circuit's capacitor: the calibration capacitor, C_C, the sensor, C_X, and the stray capacitor of the readout node, C_S. These processes are performed by controlling pins P_C, P_X, and P_R. It must be possible to configure these pins as outputs or inputs (equivalent to high impedance state, HZ). The discharge processes start from the high-level voltage of V_R in Fig. 1(a) (for simplicity and without any loss of generality, we will assume that this is the supply voltage, V_{DD}, while the low output level will be 0 V). V_R will be stored in one of the capacitors in Fig. 1(a). The discharge process is carried out by placing the readout pin, P_R, in the HZ state. The process continues through R until voltage V_R reaches, and

TABLE I
STEPS TO OBTAIN T_C, T_X, AND T_S IN (2)

STEPS	STATE OF PINS		
	P_C	P_X	P_R
1 – Charging $C_C + C_S$	'0'	'HZ'	'1'
2 – Obtaining T_C	'0'	'HZ'	'HZ'
3 – Charging $C_X + C_S$	'HZ'	'0'	'1'
4 – Obtaining T_X	'HZ'	'HZ'	'0'
5 – Charging C_S	'HZ'	'HZ'	'1'
6 – Obtaining T_S	'HZ'	'HZ'	'HZ'

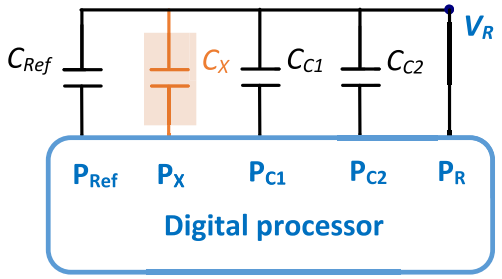

Fig. 2. DIC for the readout of capacitive sensors based on charge transfer mode [29], [30], [31].

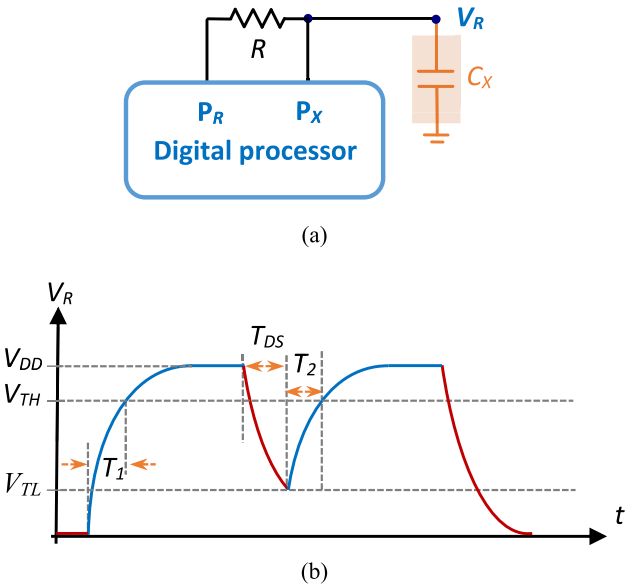

Fig. 3. (a) DIC for capacitive sensors in [34] and for the calibration-less method of [35]. (b) Voltage across C_X during charging and discharging stages in [35].

at the trigger instant, the value V_{TL}. V_{TL} is the threshold voltage to detect a logical 0 input in the P_R pin starting from a logical 1 level. The length of the discharge processes of each capacitor is measured in DP clock cycles with period T_{CK}, obtaining three values: T_C, T_X, and T_S (the subscript indicates the capacitor being discharged), which determines the value of C_X [25]

$$C_X = \frac{T_X - T_S}{T_C - T_S} \cdot C_C. \tag{2}$$

Because of this method, C_X is obtained independently of the value of R, V_{TL}, and V_{DD}, thus ensuring higher precision while avoiding thermal or aging drifts.

Table I shows the pin configuration in each of the steps necessary to obtain (2), while Fig. 1(b) shows the variation of V_R with time.

In [25], the deviation was below 1.5 pF for a measurement range from 10 to 100 pF. The design is simple but uses three charging processes to find C_X, increasing power consumption and acquisition time. Furthermore, part of the current is lost through R during charging, although this loss is negligible as R has a very high value. For example, this methodology was recently used in [27] to measure the water content in paper pulp. A slight modification of the method proposed in [25] is shown in [28], where one more cycle of measurement is used to obtain the errors of less than 2% for C_X in the range of 100 pF–2.2 nF.

An alternative circuit based on the so-called charge transfer method [29], [30], [31], [32] does not require external resistors, although it does use two calibration capacitors, C_{C1} and C_{C2}, and a reference capacitor, C_{Ref}, see Fig. 2.

In this method, C_X, C_{C1}, or C_{C2} is charged with a logical 1, and the charge is transferred to C_{Ref}, initially discharged, also fulfilling $C_{Ref} \gg C_X$, C_{C1}, and C_{C2}. By measuring the number of charge transfer cycles, it takes for the voltage stored in C_{Ref} to reach V_{TH} (V_{TH} is the threshold voltage to detect a logical 1 input starting from a logical 0 level), and C_X can be found using [29]

$$C_X = \frac{1}{N_X} \frac{N_{C1} \cdot N_{C2}}{N_{C1} - N_{C2}} (C_{C2} - C_{C1}) - \frac{N_{C2} \cdot C_{C2} - N_{C1} \cdot C_{C1}}{N_{C1} - N_{C2}} \tag{3}$$

where N_X, N_{C1}, and N_{C2} are the number of charge transfer cycles needed for C_X, C_{C1}, and C_{C2}, respectively. This method can obtain maximum errors of 0.8% FSR for the range 100 pF–1 nF [32], but, unfortunately, calibration processes are also needed (in [33], an application of the methods proposed in [29], [30], [31], and [32] to detect urine leakage is shown).

An offline calibration is proposed in [34] to avoid calibration processes during regular DIC operation (online calibration). This proposal only uses a resistor and the sensor together with a microcontroller, see Fig. 3(a). However, the microcontroller must have a digital-to-analog converter (DAC), a comparator, and an additional reference voltage. In essence, the method measures the discharging times of a series of known capacitors and establishes a set of linear approximations to the function discharging time C_X. The coefficients of these approximations are stored in a lookup table in the microcontroller. The results show a maximum relative error of 0.05% but in a minimal range of 7.6 dB (100–240 pF). Due to the values stored in the lookup table, only a single charging and discharging process of C_X is required during regular DIC operation. If the additional elements needed by this method are already present in a microcontroller, this is not a problem. However, the microcontrollers that can be used are restricted to those with these elements, and their cost and power consumption will be higher. To this, the memory resources occupied by the lookup table must be added.

For a broader range of capacitances without the need for calibration processes, Lopez-Lapeña et al. [35] proposed the same simple DIC as in Fig. 3(a). Moreover, the microcontroller

TABLE II
PIN CONFIGURATIONS IN THE NEW PROPOSAL

STEP	STATE OF PINS		
	P_A	P_B	P_O
1 – Charging C_X	'1'	'1'	'1'
2 – Discharging C_X	'HZ'	'HZ'	'0'

used as DP does not need ADCs, analog comparators, voltage references, or lookup tables. The reading process only requires four steps: two to charge C_X and two to discharge it. The steps and the three time measurements needed to find C_X (T_1, T_2, and T_{DS}) are shown in Fig. 3(b). Unfortunately, the equation used to find C_X is nonlinear. Lopez-Lapeña et al. [35] proposed simplifying the equation using a Taylor second-order polynomial approximation, finding

$$C_X \approx \frac{1}{R}\frac{B+\sqrt{B^2+4AD}}{2A} \tag{4}$$

where $A = (2 + \ln(2))\cdot\ln(2)$, $B = (1 + \ln(2))\cdot(T_1 - T_2 + T_{DS})$, and $D = -0.5\cdot[(T_1 - T_2)^2 + T_{DS}^2]$.

While this method reduces the number of charges and discharges and the errors associated with calibration capacitors, it also has some drawbacks. First, the arithmetic operations involved in (4) are challenging to perform in a DP and increase both acquisition time and power consumption, providing only an approximate solution to the value of C_X. Second, different resistors are needed for different intervals in the range of C_X to reduce errors. The result is that errors reach a maximum of 2% in the 4.7–220 nF range with $R = 200$ kΩ.

III. NEW CAPACITIVE DIC PROPOSAL

A. Description of the Method and Circuit Analysis

The new DIC is shown in Fig. 4(a). As mentioned above, the circuit performs a single charging process of C_X followed by a single discharging process. During discharge, the DP uses two pins, P_A and P_B, to detect V_{TL} in the nodes with voltages V_A and V_B in Fig. 4(a). It must be possible to configure these pins as inputs (HZ state) or outputs, while the pin P_O in Fig. 4(a) could always be an output pin (thus simplifying DP operation). All pins are configured as output pins with a logical 1 output for charging C_X to voltage V_{DD} during the charging process such that $V_A = V_B = V_{DD}$. Pins P_A and P_B are configured as inputs for the discharging process, while P_O is configured as a logical 0 output. The configuration of the pins in the two steps is shown in Table II.

Fig. 4(b) shows the time evolution of voltages V_A and V_B. During discharge, the moments when V_A and V_B reach the value V_{TL} are the trigger instants, T_A and T_B, respectively. The expressions of V_A and V_B during the discharging process are given by

$$V_A(t) = V_{DD}\cdot e^{\frac{-t}{(R_A+R_B)\cdot C_X}} \tag{5}$$

$$V_B(t) = \frac{R_B}{(R_A+R_B)}\cdot V_{DD}\cdot e^{\frac{-t}{(R_A+R_B)\cdot C_X}} \tag{6}$$

where $t = 0$ is the instant at which the discharging process begins. Fig. 4(b) shows how $V_A = V_B = V_{DD}$ at the end of the charging process. However, (6) shows that voltage in V_B

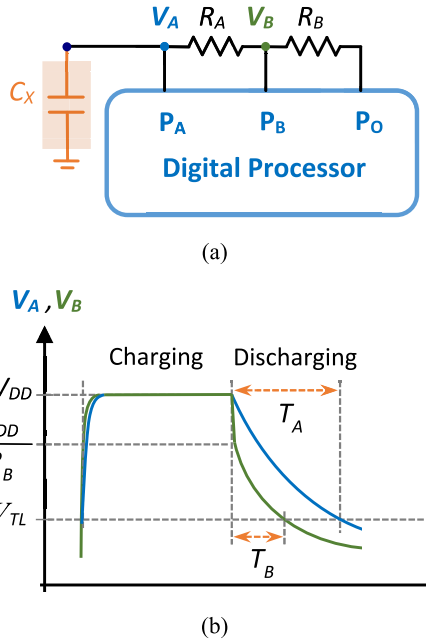

Fig. 4. (a) New capacitive DIC. (b) Time evolution of signals V_A and V_B during the charging and discharging processes and the times required to obtain the estimates, T_A and T_B.

drops sharply at the initial instant of the discharging process due to the voltage divider formed by resistors R_A and R_B, see Fig. 4(b). These resistors must ensure that $V_B(0) > V_{TL}$, so P_B recognizes V_B as a logical 1 at the start of the discharge process.

Expressions (5) and (6) can be used to find T_A and T_B

$$T_A = (R_A + R_B)\cdot C_X \cdot \ln\left(\frac{V_{DD}}{V_{TL}}\right) \tag{7}$$

$$T_B = (R_A + R_B)\cdot C_X \cdot \ln\left(\frac{R_B}{R_A+R_B}\cdot\frac{V_{DD}}{V_{TL}}\right). \tag{8}$$

These times are measured by the DP and are therefore numbers of cycles of the DP's internal clock. C_X can be found trivially by subtracting T_A and T_B

$$C_X = \frac{T_A - T_B}{(R_A+R_B)\cdot\ln\left(\frac{R_A+R_B}{R_B}\right)}. \tag{9}$$

Since R_A and R_B are known values, the DP can store the constant, k, which multiplies the subtraction of times in (9)

$$k = \left\{(R_A+R_B)\cdot\ln\left(\frac{R_A+R_B}{R_B}\right)\right\}^{-1}. \tag{10}$$

Thus, we obtain the expression that uses the new estimation method for C_X

$$C_X = k\cdot(T_A - T_B). \tag{11}$$

From an arithmetic point of view, this is a straightforward expression requiring just one subtraction and one multiplication. Moreover, since one of the multiplicands is a constant, the operation can be performed faster than the multiplication of two variables if the DP is a microcontroller. When using an application-specified integrated circuit (ASIC) or field-programmable gate array (FPGA), the operation is faster

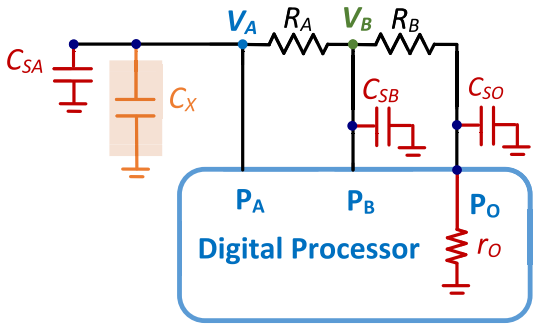

Fig. 5. Parasitic elements, in red, of the new proposed DIC affect the estimate of C_X using (11).

and requires simpler hardware [36] (note that the circuit of Fig. 4(a) could be completely included in an ASIC, if the sensor can also be integrated). Acquisition time and power consumption are also reduced, as there is only one charging and one discharging process. Finally, only two time measurements are required, thus reducing the storage of values in the DP and the sources of uncertainty in the estimation.

B. Increasing Resolution

Increasing resolution in the estimate of C_X using (11) requires the range of values in the operation T_A–T_B to be as wide as possible. This can be achieved without increasing circuit power consumption by increasing the quotient R_A/R_B to maximize the difference between the initial values $V_A(0)$ and $V_B(0)$, obtained from (5) and (6). However, as mentioned, there is an upper limit to the value of this quotient: given that $V_B(0)$ must be greater than V_{TL}, R_A and R_B must fulfill

$$\frac{R_A}{R_B} < \frac{V_{DD}}{V_{TL}} - 1. \tag{12}$$

By the very definition of V_{TL}, $V_{TL} < V_{DD}$, and it will always be possible to find values of R_A and R_B that verify (12). The designer needs only take the precaution of considering that V_{TL} is subject to small deviations derived from the operating conditions of the circuit and, consequently, consider R_A and R_B values such that R_A/R_B is the maximum possible value and, in the worst case, (12) continues to be fulfilled.

C. Error and Uncertainty Analysis

There are different sources of error in the estimate provided by (11). First, we have the parasitic elements that appear in the implementation of the circuit. These elements are shown in red in Fig. 5. There are the stray capacitors due to the DP pins and circuit routing C_{SA}, C_{SB}, and C_{SO}, along with the output resistance of pin P_O when configured as a logical 0 output, ro.

Resistor ro modifies the value of the constant k in (11), which would become

$$k = \left\{(R_A + R_B + ro) \cdot \ln\left(\frac{R_A + R_B + ro}{R_B + ro}\right)\right\}^{-1}. \tag{13}$$

According to this expression, the variation in the value of k with respect to that shown in (10) depends on the relationship between the three resistors. Error decreases as R_A and R_B increase in value with respect to ro. Element ro takes typically values ranging from just a few to several dozen ohms. Therefore, the effect of ro on k is negligible as of a few kilo-ohm when choosing R_A and R_B. The only limitations on R_A and R_B are that they must verify (12) and that the acquisition time increases as R_A and R_B do so. It is worth noting that it is trivial to verify that the relative error in k when disregarding ro is lower than the relative error in the approximation $R_A + R_B + ro \rightarrow R_A + R_B$.

Careful circuit routing will reduce the values of the three stray capacitors. However, these capacitors are inherent to the circuit, so their effects will always be present and increase as C_X decreases, imposing a lower limit for the capacitances that can be estimated with (11). However, if necessary, it is possible to improve the accuracy and, at the same time, extend the measurement range with a simple offline autocalibration. This only requires two measurements: T_A and T_B, without placing C_X in the circuit of Fig. 5 (this is a simpler process than the one performed in [34], which requires a large number of offline measurements for various calibration capacitors). The subtraction of these times multiplied by k will give the value of a parameter, C_{off}, which will be stored in the DP and offers the new estimate of C_X

$$C_X = k \cdot (T_A - T_B) - C_{off}. \tag{14}$$

Another possible source of error comes from the difference between the threshold voltages of the P_A and P_B pins of Fig. 4(a). Fortunately, in current manufacturing processes and transistors with large areas in the same die (such as those connected to pins on DPs), these differences can be less than millivolts, and the influence on the estimate is minimal.

Uncertainty in the estimate provided by (11) or (14) comes from the uncertainties in the time measurements T_A and T_B, $u(T_A)$ and $u(T_B)$, and from the uncertainty of C_{off}, $u(C_{off})$. There are two causes of $u(T_A)$ and $u(T_B)$ [37]. The first cause is that quantization in clock cycles of the time measurements produces quantization uncertainty, u_q. The second cause is electronic noise in the trigger instant in V_A and V_B, creating the trigger uncertainty, u_{trigger}. Quantization uncertainty is constant throughout the value range of C_X since it only depends on the DP's clock period. Meanwhile, u_{trigger} depends inversely on the slope of the discharge curve when it reaches voltage V_{TL} [38]

$$u_{\text{trigger}}(T) = \alpha \Big/ \left|{}^{\mathrm{d}V}/_{\mathrm{d}t}\right|_{V=V_{TL}} \approx \frac{\alpha(R_A + R_B) \cdot C_X}{V_{TL}} \tag{15}$$

where α is a constant related to the noise level in the circuit's node. Equation (15) is valid for both V_A and V_B and thus also for u_{trigger} (T_A) and u_{trigger} (T_B), simply replacing α with α_A or α_B. Since u_q is constant and u_{trigger} increases its value in line with the discharging time constant, $u_{\text{trigger}} \gg u_q$ and $u \approx u_{\text{trigger}}$ for sufficiently large values of this time constant. Regardless of the value of C_X, this situation comes about whenever enough large values of R_A and R_B are chosen. In terms of uncertainty, for (14), we can find a measurement

of quality in the estimate of C_X, $u(C_X)/C_X$

$$\frac{u(C_X)}{C_X} = \frac{1}{C_X}\sqrt{\left(\frac{\partial C_X}{\partial T_A}\right)^2 u^2(T_A)+\left(\frac{\partial C_X}{\partial T_B}\right)^2 u^2(T_B)+\left(\frac{\partial C_X}{\partial C_{off}}\right)^2 u^2(C_{off})}. \tag{16}$$

This expression becomes

$$\frac{u(C_X)}{C_X} \approx \sqrt{\left(\frac{u(T_A)}{T_A-T_B}\right)^2+\left(\frac{u(T_B)}{T_A-T_B}\right)^2+\frac{u^2(C_{off})}{C_X^2}} \approx \sqrt{\left(\frac{u(T_A)}{T_A-T_B}\right)^2+\left(\frac{u(T_B)}{T_A-T_B}\right)^2} \tag{17}$$

where we consider $u(C_{off}) \ll C_X$. Using (15), the terms inside the square root are given by

$$\frac{u(T_i)}{T_A-T_B} \approx \frac{\alpha_i}{V_{TL}\cdot \ln\left(\frac{R_A+R_B}{R_B}\right)}; i=\{A,B\}. \tag{18}$$

If the noise levels in the circuits are constant, then quotient $u(C_X)/C_X$ is constant regardless of C_X

$$\frac{u(C_X)}{C_X} \approx \frac{\sqrt{\alpha_A^2+\alpha_B^2}}{V_{TL}\cdot \ln\left(\frac{R_A+R_B}{R_B}\right)}. \tag{19}$$

IV. Experimental Results and Discussion

To test the new capacitive DIC, we have chosen an FPGA, the Xilinx Artix 7 XC7A35T, as the DP. This FPGA is included in a CMOD A7 board from Digilent (Pullman, WA, USA), together with a USB-UART bridge, a clock source, 512-kB SRAM, 4-MB Quad SPI Flash, and several I/O devices. The clock used in the DIC is a 50 MHz frequency clock generated internally in the FPGA; however, both the rise and fall edges of the clock have been used to detect the trigger instantly, meaning that counts during discharging are increased every 10 ns. The supply voltage is $V_{DD} = 3.3$ V and $V_{TL} = 1.26$ V for P_A and P_B pins of Fig. 4(b), and this was measured with a DPO 3052 digital oscilloscope from Tektronix (Beaverton, OR). It is important to note that the proposed method works in the same way as any other type of DP, as long as it has the appropriate pins (tristate pins) and hardware to measure discharging times. However, using an FPGA allows to simultaneously perform capacitive sensor readout and any other digital signal processing in parallel.

Twenty-eight discrete NP0 capacitors ranging from 100 pF to 561 nF were used for the measurements of C_X. This wide range of values (almost four orders of magnitude) includes the operating ranges of a large number of capacitive sensors. The resistors $R_A = 75\ 054\ \Omega$ and $R_B = 54\ 933\ \Omega$ have been selected to meet the design considerations outlined in Section III. With these values, $R_A/R_B = 1.37$, while the right-hand side of (12) takes the value 1.62, thus ensuring the correct operation of the circuit. Accuracy in the estimations is also guaranteed since R_A and R_B are much larger than ro (of the order of tens of ohms), and times T_A and T_B are large enough to ignore the quantization effects. With these resistors, the maximum value of T_A is 70.96 ms or a count value of approximately 7 096 000 (a 23-bit counter has been necessary to generate T_A and T_B). The minimum value of $T_A - T_B$, in a number of cycles, is obtained for the smallest capacitor in the range and is approximately 4800 (high enough to ignore quantization error). For C_{off}, $T_A - T_B = 238$, a count value considerably lower than that obtained for the lowest value of C_X. Hence, for values of C_X greater than a few hundred picofarads (pF), the influence of C_{off} in (14) is negligible and (11) can be used instead. In any case, with these data and using (14), the normalized acquisition time is approximately 0.12 ms/nF (70.96 ms/561 nF), more than three orders of magnitude smaller than in [23].

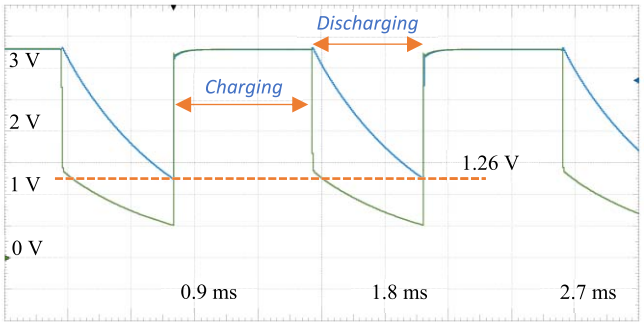

Fig. 6. Observed experimental waveform for the circuit in Fig. 4(a). V_A is in blue and V_B is in green.

Fig. 6 shows the real waveforms of V_A and V_B in the circuit of Fig. 4(a) obtained in a Digilent Analog Discovery 2 data acquisition system when $C_X = 4.67$ nF. The horizontal dashed line shows the value $V_{TL} = 1.26$ V. Due to the resistance of R_A and R_B, it can be seen from Fig. 6 that T_B is very small compared to T_A, maximizing the resolution of the system. It should be noted that, for a better observation of the waveforms in Fig. 6, a charging process time close to 0.6 ms has been selected. However, in normal circuit operation, this time is less than 0.1 ms.

Twenty series of 500 estimates were made for each capacitor, with approximately 2 s between each series. The results shown below have been obtained considering the 10 000 measurements made for each capacitor using (14) for the estimate.

Several figures of merit are used to analyze the results; the first one is shown in Fig. 7, where the maximum relative error for the estimate of C_X is defined by

$$e_R = \text{Max}\left(\frac{|C_X(i)-C_{X,a}|}{C_{X,a}}\times 100\%\right); i=\{1,2,\ldots,10^4\}. \tag{20}$$

$C_X(i)$ is each of the estimates of C_X using (14), and $C_{X,a}$ is the actual capacitance value measured by the impedance analyzer. Due to the wide range of C_X values, Fig. 7 shows the X-axis in a log scale. Fig. 7 shows that e_R is contained in a band of 0.09%–1.01%, with an average of 0.41%. These errors are distributed more or less homogeneously along the X-axis. The slight increase in e_R for lower capacitance values is mainly due to the presence of stray capacitors since, although C_{off} offsets much of its effects, it does not completely nullify them.

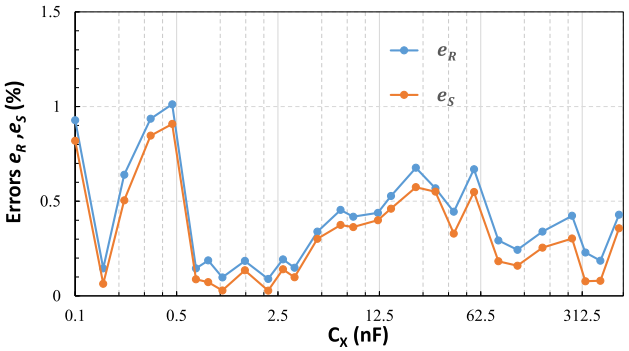

Fig. 7. Relative and systematic errors, e_R and e_S, for the new proposed DIC. The X-axis, in log5 scale, shows the capacitors under test.

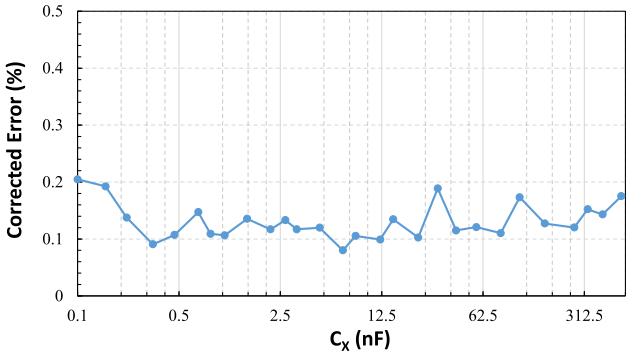

Fig. 8. Corrected error that appears in the estimate of C_X due to eliminating the systematic error shown in Fig. 7.

It should be noted that the circuit used has not been designed ad hoc, so the value of stray capacitors will probably be higher than would be obtained in a specific design. However, the authors have decided to use the configuration described in this section to demonstrate the possibilities of the new estimation method in an actual development environment. In any case, the maximum e_R is 1.01% for a wide range of more than three orders of magnitude, 75 dB.

Fig. 7 also shows the (in orange) systematic error, e_S, of the new capacitive DIC, defined as

$$e_S = \frac{\left|\overline{C} - C_{X,a}\right|}{C_{X,a}} \times 100\% \tag{21}$$

where $\overline{C}$ is the average of all $C_X(i)$. The most important aspect to note about e_S is that these values are very close to e_R throughout the range. This indicates that errors in the estimate of C_X are mainly due to the stray elements shown in red in Fig. 5 and to the simplification that occurs in (13) when disregarding ro. Therefore, relative errors due to uncertainties in the time measurements should be much more minor, confirming the suitability of the values chosen for R_A and R_B.

This can be verified in Fig. 8, which shows the relative error resulting from eliminating systematic error contribution in e_R. We call this corrected error, and as shown in the figure, it is significantly smaller than e_R (below 0.21% for all C_X values). In [34], it is proposed that this parameter be the measure of the system error. As discussed in Section II, the mean of the estimations of several C_X values obtained in the offline calibration process of [34] is stored in the DP, ready to be used when correcting $C_X(i)$ during real-time operation of the system. However, caution is required in applications where this methodology is applied since the conditions under which offline calibration is performed may differ significantly from the circuit's normal operating conditions. In any case, the almost constant values of the corrected errors indicate that uncertainties in the time measurements must have a similar form.

Fig. 9 shows the quotients of $u(T_A)$ and $u(T_B)$ with $T_A - T_B$, which we will call normalized time uncertainties. As predicted in (18), these quantities are approximately constant over the entire range of C_X. The results shown in Fig. 9 indicate that $u(T_A) < u(T_B)$ for practically all C_X values. This result stems

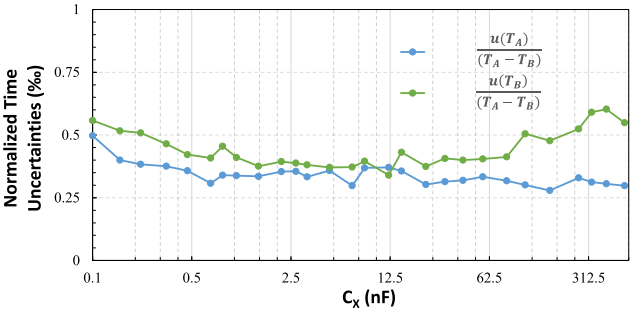

Fig. 9. Relative uncertainties in time measurements for nodes A and B in Fig. 4(a) (both quantities expressed in ‰).

from the capacitive nature of node A in Fig. 4(a), which helps reduce noise in this node with respect to node B in Fig. 4(a).

Thus, $u(T_B)$ values show higher dispersion than those of $u(T_A)$. The same is also true for the two normalized time uncertainties in (17) when establishing relative uncertainty in the estimate of C_X. Consequently, to reduce the value of this parameter and improve the estimation, special care must be taken in the routing of node B whenever a specific design is chosen for the new DIC, striving to reduce any noise sources that may affect it.

Since the normalized time uncertainties remain approximately stable over the entire range of C_X, according to (18), the same should be true for relative uncertainty in the estimate of C_X. Fig. 10 confirms this, showing a narrow variation range, with a minimum of 0.29‰ for $C_X = 12.21$ nF and a maximum of 0.60‰ for $C_X = 100$ pF. Thus, the quality of the estimates of C_X is very uniform in terms of uncertainty, as predicted by (19).

Fig. 11 shows another parameter of interest, namely, linearity error, e_L, defined as

$$e_L = \frac{\Delta_{\max}}{C_U - C_L} \times 100\% \tag{22}$$

where $\Delta_{\max}$ is the maximum difference between the fit linear relationship and all $C_X(i)$, while C_U and C_L are the upper and lower limits of the measurement range of C_X, respectively. As shown in Fig. 11, the e_L values are very small (less than 0.03%) up to about 50 nF. From here, e_L grows, but always very smoothly, with a maximum of less than 0.3% for 561 nF.

TABLE III
COMPARISON

Work	DC Source	Capacitor Range	Calibration	Charging-Discharging Processes, N_{CD}	e_R	Normalized Acquisition Time (ms/nF)	Additional Passive Elements	DP type / Used Pins / DP Requirements	Arithmetic Operations
[25]	5 V	149 pF – 206 pF (2.8 dB)	Online	3	5.61%	2.5	2 Resistors + 1 Capacitor	µC / 3 / Timer	1 Division + 2 Subtractions
[30]	5 V	300 pF – 10 nF (30.5 dB)	Online	1	10 %	0.65	1 Resistor + 1 Capacitor	µC / 4 / Timer Voltage comparator V_{TL} and V_{TH} known	3 Multiplications + 1 Division + 2 Additions + 1 Subtraction
[32]	5 V	100 pF – 1 nF (20 dB)	Online	3	1.1%	125	3 Capacitors	µC / 5 / Timer	5 Multiplications + 2 Divisions + 4 Subtractions
[34]	3.3 V	100 pF – 240 pF (7.6 dB)	Multiple Offline Measurements	1	1.3%	8.45	3 Resistors	µC / 4 / Timer DAC Voltage comparator Voltage reference source	1 Multiplication + 1 Subtraction
[35]	3.3 V	47 nF – 220 nF (13.4 dB)	No	2	2%	–	1 Resistor	µC / 2 / Timer	Square root + 5 Multiplications + 1 Division + 1 Addition
This Work	3.3 V	100 pF – 561 nF (75 dB)	Two Offline Measurements	1	1.0%	0.12	2 Resistors	FPGA / 3 / Timer	1 Multiplication + 2 Subtractions

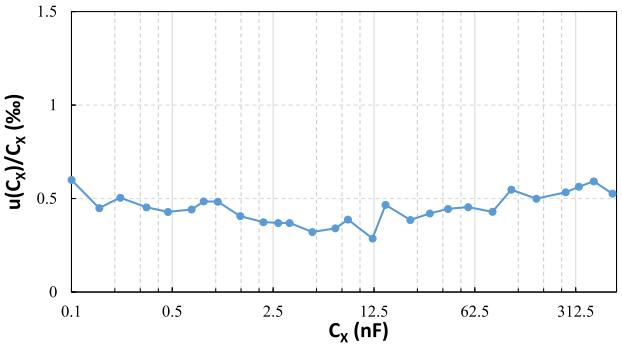

Fig. 10. Relative uncertainty in the estimate of C_X expressed in ‰. As with the normalized time uncertainties in Fig. 9, the values move in a very narrow band for any C_X.

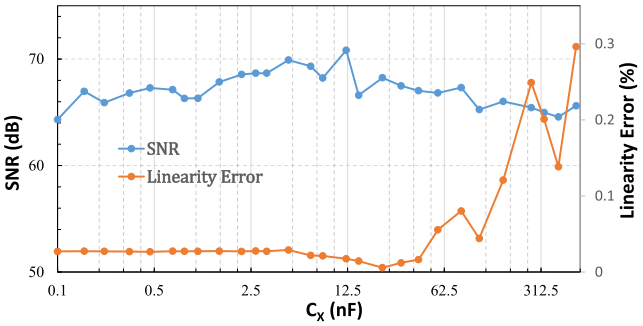

Fig. 11. Linearity error and SNR of the proposed DIC.

Fig. 11 also shows the results for the signal-to-noise ratio (SNR) of the new capacitive DIC, which is calculated as

$$\mathrm{SNR} = 10 \cdot \log\left(\frac{\sum_i C_X(i)^2}{\sum_i \left[C_X(i) - \overline{C}\right]^2}\right). \tag{23}$$

As expected from the results presented in the figures above, SNR is also very stable. The minimum SNR is 64.3 dB for the 100 pF capacitor, while the maximum is 71 dB for a 12.21-nF capacitor.

Although the V_{TL} values measured for P_A and P_B have been the same, small differences (not detected with the instruments used) may affect the results presented. The circuit connections to these pins in Fig. 4(a) (pins T_2 and R_2 of the FPGA) were swapped to assess this. The C_X estimates obtained for the new circuit configuration show a maximum variation of 0.17% in e_S compared to the results shown in Fig. 7 (this maximum variation occurs for $C_X = 1$ nF). In any case, the maximum e_R remains at 1.0% for the entire range.

The main characteristics of the new circuit have been analyzed in comparison with others existing DIC schemes and presented in Table III. As shown in Table III, the new proposal shares with [30] and [34] that they only require a single charging–discharging process. Thus, the proposed circuit is among those that allow a higher reading frequency. Besides, the selected R_A and R_B (with the only restriction given by (12)) achieve the fastest normalized acquisition time, as can be seen in the seventh column of Table III.

The energy consumption of the measurement system, E_T, depends on two terms: the energy consumed by the capacitor to be measured and that consumed by the DP, E_{DP}

$$E_T = \frac{1}{2} C_X V_{DD}^2 \cdot N_{CD} + E_{DP} \tag{24}$$

where N_{CD} is the number of charging–discharging processes. As in our proposal $N_{CD} = 1$, the energy consumption in the capacitor is the minimum possible. For example, for a capacitance of 1 nF, the first term on the right-hand side of (24) is 5.45 nJ. $N_{CD} = 1$ also happens in [30] and [34]; however, in [30], the maximum errors are 10%, and in

[34], multiple offline measurements are needed. E_{DP} mainly depends on the DP's choice, which depends on the application for which the system is intended (as mentioned above, in our case, we have selected an FPGA as DP). It is difficult to experimentally measure the power consumption of the FPGA since it is included in a PCB with other components. However, the manufacturer's programming tool provides an estimate of 0.179 mW. This power consumption comprises, in addition to the resources used for reading the capacitor (counters, arithmetic unit, and state machine), the resources used for the communication of the CMOD A7 board with a personal computer (RAM and serial communications port).

On the other hand, as shown in the eighth column of Table III, only the DIC proposed in [35] needs one less element (one resistor) than the new DIC. Nevertheless, in [35], performing the most demanding arithmetic operations on the DP is necessary. Furthermore, the arithmetic operations in the new DIC are amounting the simplest. Regarding the hardware resources needed on the DP (penultimate column of Table III), this proposal only needs one timer and uses only three pins.

Finally, it must be considered that the C_X range is practically 45 dB larger in the new proposal than any other range of the rest of the proposals (third column of Table III).

V. Conclusion

Many different circuits can be used to read a capacitive sensor, of which so-called DICs stand out for their simplicity. These designs can perform capacitance-to-time-to-digital conversion with just a few passive components and a DP without the need for ADCs. The DP is responsible, first, for controlling the charging and discharging processes of the capacitive sensor as necessary to establish its capacitance, C_X, and, second, for measuring the duration of these processes. The time measurements, quantified in DP clock cycles, produce an estimate of C_X. However, many capacitive DICs proposed in the literature require different calibration capacitors and/or several charging and discharging cycles to perform the estimation, with the consequent increase in acquisition time and power consumption. Furthermore, the arithmetic operations required to obtain the estimates are often complex, increasing the time and the resources used by the DP.

This article proposes a new DIC for reading capacitive sensors that aim to overcome these drawbacks. The circuit is very simple, as it only requires two additional resistors apart from the DP, without any calibration capacitors. This decreases the cost and size of the DIC. Furthermore, selection criteria have been established for these resistors to ensure the correct operation of the circuit and minimize errors. The new DIC proposal requires only a single charging and discharging cycle to obtain the two time measurements used in the calculations to find C_X, thus reducing the time and energy consumption needed to estimate C_X. The estimate is obtained by a linear transformation of the subtraction of these measurements, using two constants stored in the DP. Consequently, the operations performed on the DP and the memory requirements are minimal.

The circuit has been tested using a state-of-the-art FPGA as the DP. The results show that the circuit works correctly for a vast range of capacitance values, 100 pF–561 nF (75 dB). Relative errors in the estimates present a maximum of 1.01% and an average over the entire range of 0.41%, with relatively stable values. Linearity errors are below 0.3% at the top of the range, but for most of the range, they are below 0.03%. SNR is also relatively stable, varying between 64 and 71 dB.

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