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Impact of Interface Traps in Floating-Gate Memory Based on Monolayer MoS_2

G. Giusi, G. M. Marega, A. Kis, *Senior Member, IEEE*, and G. Iannaccone, *Fellow, IEEE*

***Abstract*— Two-dimensional materials (2DMs) have found potential applications in many areas of electronics, such as sensing, memory systems, optoelectronics, and power. Despite an intense experimental work, the literature is lacking of accurate modeling of nonvolatile memories (NVMs) based on 2DMs. In this work, using technology CAD simulations and model calibration with experiments, we show that the experimental program/erase characteristics of floating-gate (FG) memory devices based on monolayer molybdenum disulphide can be explained by considering bandgap trap states at the dielectric–semiconductor interface. The simulation model includes a classical approach based on drift-diffusion longitudinal channel transport and on nonlocal Wentzel–Kramers–Brillouin (WKB) tunneling for transversal transport (responsible of FG charging/discharging) and for tunneling at contacts. From hysteresis and pulse programming simulations on scaled devices, we find that the long-channel programming window is still maintained at ∼100 nm and that process improvements aimed at reducing the concentration of interface traps in the semiconducting bandgap could significantly optimize memory operation.**

***Index Terms*— Bidimensional materials, device simulation, experimental measurements, floating-gate (FG) memories, modeling, MoS_2, nonvolatile memories (NVMs), transition metal dichalcohenides.**

I. INTRODUCTION

MANY nonvolatile memory (NVM) concepts, such as resistive random access memories (RRAMs), phase-change memories (PCMs), and magnetic random access memories (MRAMs), are under investigation as alternatives to the conventional silicon-based flash memories [1]. The continuous advancements in fabrication processes and the discovery and synthesis of new materials have triggered new directions for research in NVMs. In particular, transition metal dichalcogenides (TMDCs), such as MoS_2 and WSe_2, are semiconducting two-dimensional materials (2DMs) that have been used as channel materials in FETs with near ideal subthreshold slope, high ON/OFF ratio ($>10^6$), and relatively large mobility ($>50\div100$ $cm^2/V/s$) [2], [3]. The broad spectrum of interesting physical, chemical, and electrical characteristics of 2DMs makes them attractive for the development of NVMs [4], [5]. In the first experiments of using 2DMs in NVMs, graphene has been used as a storage layer of a floating-gate (FG) memory due to its low conductivity along the transversal direction (useful for reducing the charge leakage) [6], [7]. After the demonstration of the first monolayer MoS_2 FET in 2011 [2], extensive research has been done in FG memories fully or partially based on 2DMs [4]. In these works, 2DMs have been experimented as storage node, semiconducting channel, insulator, and electrode [8], [9], [10], [11], [12], [13], [14], demonstrating memory windows up to 60 V by using black phosphorous as an active layer and MoS_2 as a storage layer [12], or current switch ratio up to 10^5 and 10-year retention loss of 40% by using metal nanocrystals in the gate dielectrics as a storage layer and MoS_2 as an active layer [10]. Despite this intense experimental work, there are few results in the literature about the modeling of NVMs based on 2DMs. One reason might be the fact that the electrostatics and the dynamics of the program and erase operations of a cell are strongly affected by the presence of traps localized in the 2-D layer, at the interfaces, or into the dielectric layer and that a complete defect characterization is not available. Defects are responsible for additional variability of the transport characteristics and for reliability issues, such as hysteresis and bias temperature instability. In particular, hysteresis can increase the measured memory window in FG memories and has been attributed to both intrinsic traps in the channel material (such as sulfur vacancies in MoS_2 [15], [16]) and/or to slower dielectric traps [17], [18], [19]. In addition, geometry and process have a large impact on device characteristics. The great diversity of trap sources makes modeling of 2DM-based devices a hard task, especially in the case of NVMs, where longitudinal and vertical transport are intertwined. In this work, we propose a device modeling approach that includes semiconductor bandgap traps and Wentzel–Kramers–Brillouin (WKB) tunneling that is able to reproduce the program/erase operation during the hysteresis of backgated FG devices based on a monolayer MoS_2 channel with HfO_2 dielectric recently demonstrated in [14] and [20]. We also show that memory

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G. Giusi is the with Engineering Department, University of Messina, 98166 Messina, Italy (e-mail: ggiusi@unime.it).

G. M. Marega and A. Kis are with the Institute of Electrical and Microengineering, École Polytechnique Fédérale de Lausanne (EPFL), 1015 Lausanne, Switzerland (e-mail: guilherme.migliatomarega@epfl.ch; andras.kis@epfl.ch).

G. Iannaccone is with the Dipartimento di Ingegneria dell'Informazione, Università di Pisa, 56122 Pisa, Italy (e-mail: giuseppe.iannaccone@unipi.it).

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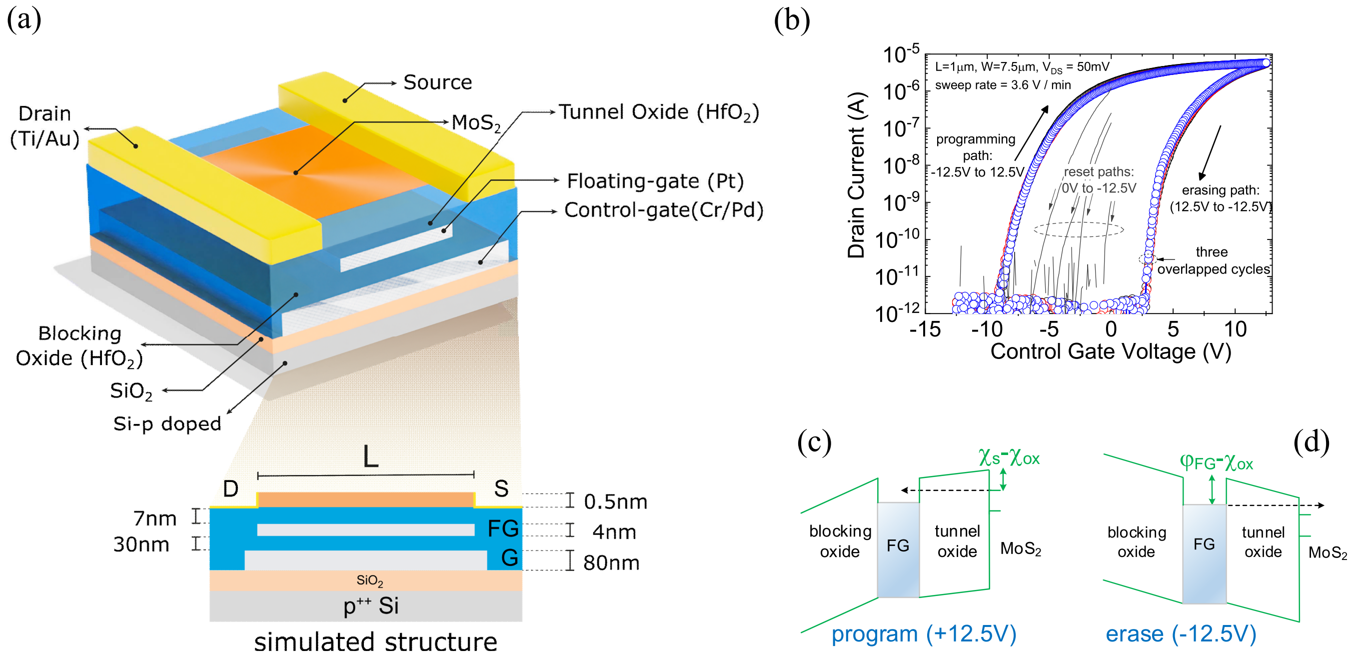


Fig. 1. (a) Three-dimensional view of the FG memory device based on a MOCVD-grown MoS_2 monolayer with evaporated source and drain Ti/Au (2/80 nm) contacts. The platinum FG (~4 nm thick) is separated from the MoS_2 channel by a 7-nm-thick HfO_2 tunnel oxide layer and from the bottom control gate made by Cr/Pd (2/80 nm) by a 30-nm-thick HfO_2 blocking oxide layer. The gate length and width are $L = 1$ μm and $W = 7.5$ μm, respectively, while the FG region is $L_{FG} = 800$ nm. (b) Three measured hysteresis cycles (symbols) in the investigated devices. A large memory window (>10 V) is measured, which is due to electron charging/discharging of the FG. The large voltage difference necessary to switch off the channel is due to the presence of interfacial semiconductor traps. (c) and (d) Energy barrier profile along the tunneling direction during programming at (c) +12.5 V and erasing at (d) −12.5 V showing electron injection to/from the FG.

performance can be greatly enhanced by suppressing interface traps and that it is preserved if the channel length is scaled down to 100 nm.

II. Device Fabrication

Fig. 1(a) (top) presents a three-dimensional illustration of the fabricated memory devices. The fabrication process is based on *E*-beam lithography for regions patterning over a SiO_2/p^{++} Si substrate. After the metal evaporation of the bottom gate made with Cr/Pd (2/80 nm), the blocking dielectric made of HfO_2 (30 nm) is deposited by atomic layer deposition (ALD). Then, the FG made with platinum (~4 nm) is evaporated and the HfO_2 tunnel oxide (7 nm) is deposited by ALD. Final steps are the transfer of a single-crystal MoS_2 monolayer, grown by metal–organic chemical vapor deposition (MOCVD), onto the patterned substrate, and source–drain metallization by the evaporation of Ti/Au (2/80 nm). Devices are not passivated, but electrical measurements are performed in vacuum after an *in situ* annealing (VA) of the devices at 135 °C. The VA has been shown to be an effective technique to remove possible water and oxygen adsorbents on the surface of the material [42]. The gate length and width are $L = 1$ μm and $W = 7.5$ μm, respectively, while the length of the FG region is $L_{FG} = 800$ nm. Basic electrical characterization, reliability, and further processing details can be found in [14] and [20].

III. Electrical Measurements

Our FG transistor works by tunneling charges from and to the metal trap layer [see Fig. 1(c) and (d)], creating a change in the number of charges in the trap layer and a shift of the threshold voltage of the transistor (ΔV_T). More details on device operation can be found in [20]. The threshold voltage shift can be experimentally investigated by doing a round trip drain-current (I_{DS}) versus gate-voltage (V_{GS}) measurements. Fig. 1(b) shows such measurements with V_{GS} bounded between −12.5 and 12.5 V at a sweep rate of 3.6 V/min and $V_{DS} = 50$ mV. As can be observed, a hysteresis cycle with a large memory window (>10 V) is measured, which is explained as due to electron charging of the FG during the programming path (V_{GS} from −12.5 to +12.5 V) and due to electron discharging of the FG during the erasing path (from +12.5 to −12.5V), as confirmed by device simulation discussed in the following sections. Because each point measured in a hysteresis cycle depends on the previous measurement history, it is important to fix a reference state in the FG prior to the start of the measurement/simulation. This is also particularly important because the initial charge in the FG after fabrication is unknown. Gray lines in Fig. 1(b) show the initial reset paths with V_{GS} from 0 to −12.5 V after different measurement cycles and at different times. While the reset paths are different, due to a different initial charge in the FG, the subsequent programming paths are quite similar, indicating that a control gate voltage of −12.5 V is sufficiently negative to fix a reset condition in the FG. The measurement in Fig. 1(b) starts with the initial RESET path from the idle state at 0 V to the erasing voltage of −12.5 V. Three consecutive hysteresis cycles are therefore measured from the erasing voltage of −12.5 V to the programming voltage of +12.5 V and from +12.5 to −12.5 V. As can be observed from Fig. 1(b), the three cycles overlap one to the other, confirming that −12.5 V is sufficiently negative to completely deplete

the FG from the charge stored during the programming path (at least up to +12.5 V). Because the longitudinal dimension (channel length $L = 1$ μm) is much larger than the vertical dimension (total dielectric thickness $\approx$37 nm) and because the semiconductor region is a monolayer, the electrostatics is expected to be well controlled (as confirmed by device simulation in the next sections) and cannot be responsible of the poor current–voltage slope. This measured behavior has been observed in literature in the cases of back gate, SiO_2 dielectric and/or CVD process, and is attributed to the presence of traps at the semiconductor/dielectric interface and/or in the dielectric itself [21]. Likewise, in the next sections, we explain the large 0 V current and the low current–voltage slope as due to the presence of bandgap traps at the semiconductor/dielectric interface.

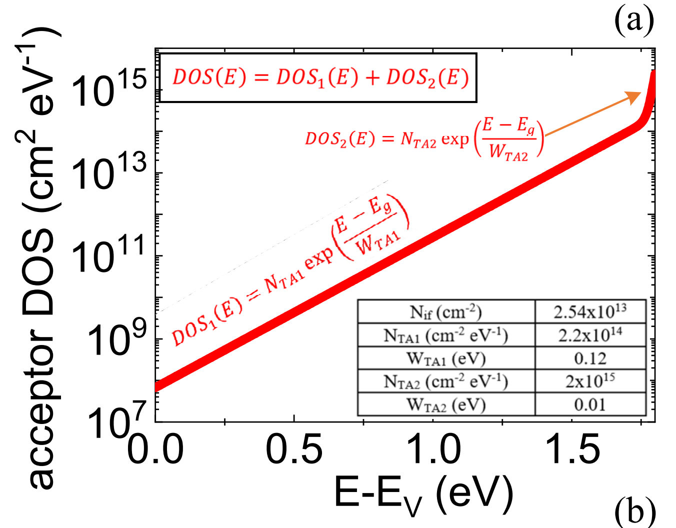
IV. Device Structure, Simulation, and Traps Modeling

A. Device Structure

The simulated structure is shown in Fig. 1(a) (bottom side). The thickness of the semiconductor region (energy gap $E_g = 1.8$ eV and relative dielectric constant equal to 4) is chosen to be 0.5 nm and must be considered a fitting parameter, as discussed in the following, while the gate length (L) ranges from the experimental 1 μm to a scaled value of 20 nm. Source and drain contact regions have a length of 100 nm. The tunnel and control dielectric regions are 7 and 30 nm thick, respectively, with a relative dielectric constant equal to 22. The FG region is simulated as a metal region with a thickness of 4 nm and a length of $L_{FG} = 800$ nm for $L = 1$ μm and scaled accordingly for lower L.

B. Simulation Model

Transport in lateral and vertical heterostructures based on 2DMs is normally handled by quantum transport approaches [22]. However, in monolayer TDMCs, due to the parabolicity of the energy dispersion at band minima [23], despite the relative large mean free path ($\lambda \approx 15$ nm) [24], the modeling of the longitudinal transport in long channels ($L \gg \lambda$) does not need this degree of sophistication and is complicated by the inclusion of scattering in quantum transport models. In fact, experimental data have been successfully reproduced in terms of an effective mass/diffusive approach by means of continuum-based physical/compact modeling [25], [26], [27], [28], [29], [30] and TCAD simulation [31], including the effects of traps, contacts, and velocity saturation. In this work, two-dimensional device simulations [32] have been used to reproduce the measured hysteresis cycles in Fig. 1(b). The simulation model is based on a conventional 3D-density of states (DOS) drift-diffusion approach, Fermi-Dirac statistics, and Shockley–Read–Hall (SRH) recombination (Scharfetter) for the longitudinal transport, while nonlocal WKB tunneling is used for the charge injection from the semiconducting channel into the FG (with tunneling mass $m_t = 0.19$ m_0). Transport at source–drain contacts is modeled by nonlocal WKB tunneling with Schottky boundary conditions. Because a monolayer MoS_2 has a relatively large gap (1.8 eV in this



(b)

	MoS_2	HfO_2
bandgap	1.8 eV	
electron affinity	χ_s=3.95 eV	χ_{ox}=2.5 eV
dielectric constant	$4\varepsilon_0$	$22\varepsilon_0$
Source/Drain barrier	0.3 eV	
effective mass	m_n=0.54m_0 m_p=0.44m_0	m_t=0.19m_0
	Floating Gate	**Control Gate**
workfunction	φ_{FG}=4.65 eV	φ_{CG}=5 eV

Fig. 2. (a) Interface trap density used in device simulation is composed of a constant fixed component N_{if} and an acceptor bandgap component DOS(E) $= N_{TA1} \exp(E - E_g/W_{TA1}) + N_{TA2} \exp(E - E_g/W_{TA2})$ and (b) relevant simulation parameters [see energy band modeling in Fig. 1(c) and (d)].

work) and because it is undoped, a significant electron current can flow only at sufficient high gate voltage, and at a sufficient low Schottky barrier (300 meV in this work), the low Schottky barrier setting the Fermi level close to the conduction band allowing a significant mobile electron charge. Electron and hole effective masses are $m_n = 0.54$ m_0 and $m_p = 0.44$ m_0 [41], respectively, where m_0 is the free electron mass. Relevant simulation parameters are summarized in Fig. 2.

C. Traps Modeling

The very thin channel region and the very long channel length would make the electrostatics of a similar made device ideal with a strong switch-off and negligible current at $V_{GS} = 0$ V [see dashed curves in Fig. 4(b)]. However, this is not the case in many experiments and, in particular, is not the case of the investigated devices as discussed in Section III. In order to reproduce the low current–voltage slope and the large current observed at 0 V, interface semiconductor bandgap traps are used. The presence of defects in 2DM-based devices has been widely experimentally demonstrated by the observed variability, hysteresis, time-dependent temperature-bias instability, and temperature activation. Defects can stay at the dielectric interface and/or in the dielectric itself. Although

the picture is far to be clear, it is believed that sulfur vacancies in MoS_2 layers are a major source of instability [15], [16]. These defects introduce interfacial bandgap states with a D_{it} peak of the order of $10^{12} \div 10^{13}$ cm^{-2}eV^{-1} regardless of the gate dielectrics [16], [19], [33], [34], [35], [36]. Some work [34], [37] reported that sulfur vacancies introduce localized donor states around 0.35 eV from the midgap. In this work, the interface traps are modeled with a positive fixed charge $N_{if} = 2.5 \times 10^{13}$ and with a double exponential acceptor tail in the semiconductor bandgap with DOS $N_{TA1} \exp(E - E_g/W_{TA1}) + N_{TA2} \exp(E - E_g/W_{TA2})$ as reported in Fig. 2, where W_{TA1} and W_{TA2} are the exponential decay factors. Bandtail exponential states are typically used to reproduce the electrostatics in thin-film transistors [38] and have been reported also for MoS_2-based FETs [30], [39]. The fixed interface charge N_{if} has been included to adjust the flatband bias point. This value is in line with an effective interface trap density extracted by CV/IV measurements [16], [19], [33], [34], [35], [36] [37]. In this continuum-based context, the thickness of the simulated semiconductor layer (0.5 nm) must be considered a fitting parameter of the traps and of the MoS_2 DOSs.

V. Simulation Results

A. Hysteresis

Fig. 1(c) and (d) shows the band profile, along the tunneling direction, at the programming (erasing) bias of +12.5 V (−12.5 V). During programming, channel electrons direct tunnel, through the tunnel oxide thickness (7 nm), with a barrier height χ_s-χ_{ox} (=1.45 eV in the proposed model), being χ_s and χ_{ox} the electron affinities of the semiconductor (MoS_2) and of the oxide (HfO_2), respectively. In the same way during erasing, electrons stored in the FG direct tunnel into the semiconductor through a barrier of height ϕ_{FG}-χ_{ox} (=2.15 eV in the proposed model), being ϕ_{FG} the workfunction of the FG, allowing the discharge of the FG. This charging/discharging phenomena is the responsible of the measured hysteresis in Fig. 1(b). Fig. 3 shows the good agreement between measurements (solid lines) and simulation (symbols) of hysteresis cycles that share the same minimum erasing voltage of −12.5 V but have different maximum programming voltages V_{PRG} ranging from 5 to 12.5 V. Let us stress that the dynamics of the introduced semiconductor traps does not contribute to the measured hysteresis, as traps are fast (simulated capture cross section is 10^{-15} cm^2) with respect to the very slow sweep rate (3.6 V/min), meaning that the simulated programming window is totally due to the FG charging/discharging phenomena. From Fig. 3, we can observe that while the simulated erasing path reflects a shifted version of the simulated programming path, as expected for FG charge storing, the measured erasing path is slightly steeper than the measured programming path in the lower current region, probably indicating the presence of an additional charge transfer mechanism. A possible source of the distortion observed in the erasing path is the presence of traps inside the tunnel dielectric. Tunneling between the channel and dielectric traps

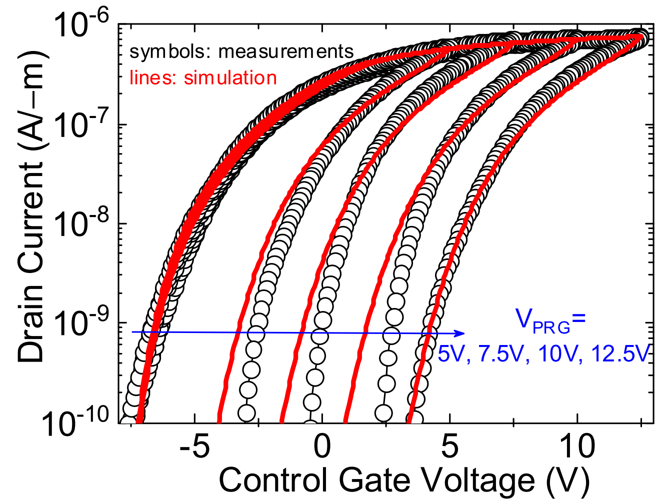


Fig. 3. Measured (black symbols) and simulated (red lines) hysteresis cycles with fixed erasing voltage at −12.5 V and variable maximum programming voltage V_{PRG} from 5 to 12.5 V. The sweep rate in experiments and simulations is 3.6 V/min.

could occur with a slow time constant—due to the small transmission coefficient—comparable with the measurement sweep rate. Indeed, some experiments [17], [18], [19] have shown that slow dielectrics traps can play an important role in the measured hysteresis and instability in 2DMs-based devices.

B. Pulse Programming

While hysteresis cycles are useful from the experimental point of view to understand memory effects, they do not reproduce actual device operation in circuits because the measured programming window is a function of the measurement history. Moreover, it is noteworthy that the memory window measured from pulse programming is significantly lower than that measured by hysteresis [40]. In order to highlight the memory effect in normal operating conditions, we have simulated I_D–V_G characteristics after the application of programming pulses [see Fig. 4(a)] with variable amplitude V_{PRG} and variable width t_{PRG}. Fig. 4 (plots with solid lines) shows the shift of the characteristics [see Fig. 4(b)] and the calculated threshold voltage shift ΔV_T for different pulse amplitudes V_{PRG} [see Fig. 4(d)] and widths t_{PRG} [see Fig. 4(c)]. The threshold voltage shift ΔV_T (with respect to the fresh curve) is calculated at the constant current $I_D = 10^{-10}$ A/μm, and during I_D–V_G simulation, the programming mechanism is turned off in order to have a noninvasive read operation. Results show that reasonable programming windows can be obtained with programming times in the order of tens of nanoseconds and that the program operation is more sensitive to an increase of the programming voltage (in particular above ~10 V) rather than to an increase of the programming time. In particular, from Fig. 4(d), an exponential like behavior (with a threshold) of ΔV_T with respect to the programming voltage V_{PRG} is observed. This expected behavior is due to the

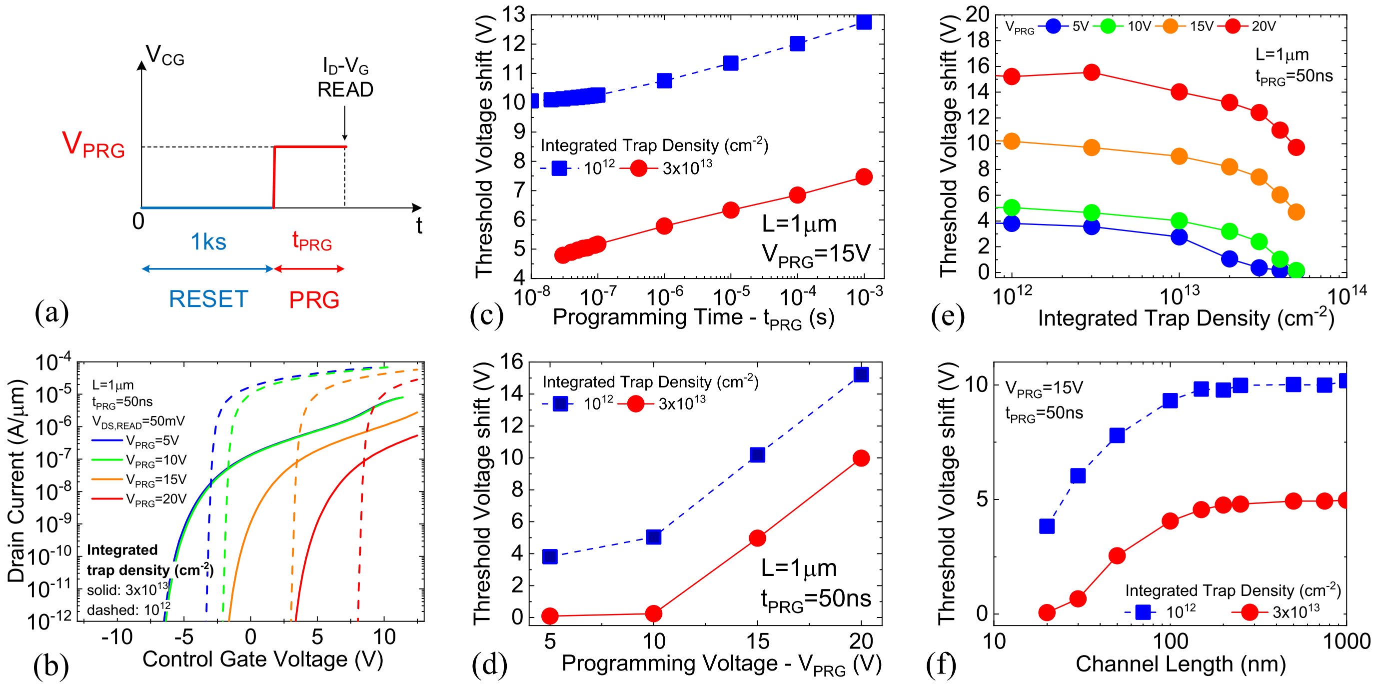


Fig. 4. Simulations with programming pulses (a) with variable programming time t_{PRG} and programming voltages V_{PRG} to show the memory effect. (b) Drain current versus gate voltage characteristics after programming for $L = 1\ \mu$m and $t_{PRG} = 50$ ns and for different $V_{PRG} = (5, 10, 15, 20\text{ V})$. Shift of the threshold voltage, calculated at $I_D = 10^{-10}$ A/μm, as a function of (c) programming time, (d) programming voltage, (e) integrated trap density, and (f) gate length.

exponential like behavior of the tunneling current with respect to the tunneling oxide field and control gate voltage.

C. Bandgap Traps Influence

Another key aspect is the influence of bandgap traps on the programming window. Fig. 4(e) shows the threshold voltage shift ΔV_T calculated from pulse programming with $t_{PRG} = 50$ ns and different values of V_{PRG} as a function of the "integrated trap density" N_t, defined as the semiconductor DOS integrated over the bandgap. At the reference values of N_{TA1} and N_{TA2} reported in Fig. 2, $N_t \approx 3{\cdot}10^{13}$ cm^{-2}. The value of N_t in the x-axis of Fig. 4(e) is calculated by scaling the values of N_{TA1} and N_{TA2} by the same factor. As can be observed from Fig. 4(e), a high concentration of bandgap traps significantly reduces the programming window and the threshold voltage shift ΔV_T. In particular, it is interesting to note that the programming window degradation can be considered negligible below $\sim N_t = 10^{12}$ cm^{-2}. This result can be of great interest in view of material and process improvements to optimize memory performance. Fig. 4(b) also shows the I_D–V_G characteristics, and Fig. 4(c) and (d) shows the related threshold voltage shift ΔV_T when $N_t = 10^{12}$ cm^{-2}(dashed plots), which is equivalent to the case of negligible bandgap traps concentration. In particular, from Fig. 4(b), one can observe the strong switch-off caused by the near ideal electrostatics, as discussed in the previous sections.

D. Gate Length Scaling

Finally, Fig. 4(f) (solid line) shows the shift of the threshold voltage as a function of the gate length using programming pulses with $t_{PRG} = 50$ ns and $V_{PRG} = 15$ V. As the gate length is scaled down, the programming window is narrowed due to the increased semiconductor potential and reduced transverse field across the tunnel oxide, which in turn induces a lower tunnel injection into the FG. Pulse programming simulations show that a gate length of about 100 nm still preserves most of the long-channel memory window. The same figure shows the threshold voltage shift ΔV_T (dashed line) when bandgap traps are negligible (i.e., when $N_t = 10^{12}$ cm^{-2}). Although traps reduce the programming window, as discussed above, they do not significantly affect the ΔV_T roll-off, hence the device electrostatic degradation induced by the shorter channels.

VI. Conclusion

We have investigated the impact of interface traps on the memory behavior of back gated FG devices based on a monolayer MoS_2 channel with high-k dielectric (HfO_2) by using device simulation and model calibration with experiments. Simulations are based on drift-diffusion longitudinal channel transport and WKB direct tunneling for transversal transport for FG charging/discharging and for tunneling at contacts. Despite the thin and long ($L = 1\ \mu$m) channel region, experiments show highly degraded electrostatics, which is successfully modeled considering a proper bandgap interfacial acceptor trap distribution in the semiconductor. The combination of such DOS and of band parameters for the transversal transport allows to well reproduce the measured hysteresis of the investigated devices. We find that bandgap traps significantly reduce the programming window, suggesting that material and process improvements are expected to optimize

memory performance. Finally, the scaling analysis reveals that the long-channel programming window is still maintained at ∼100 nm and that traps do not significantly affect the threshold voltage shift roll-off. The presented results suggest that NMVs based on 2DMs are a promising option for the integration of 2DMs-based electronic systems. Future works include the effect of traps on time retention and reliability.

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