Trench Split Gate MOSFET's Inductive Switching

H. Kang^D

Abstract—A trench split gate metal-oxidesemiconductor field-effect transistor (MOSFET) inductive switching is analyzed by adopting six-terminal method. Owing to the buried source terminal in the trench oxide, conventional three-terminal (gate, source, and drain) analysis has a limitation for investigating the detailed time-dependent current flow in the drift region, channel, as well as each terminal. However, a mixed-mode simulation tools enable us to look into the complicated current flow mechanisms in the device by dividing the gate terminal into the gate-to-source and the gate-to-drain terminals and the source terminal into the n+, the p+, and the shielded source terminals. The six-terminal method enables us to understand the fundamental turn-on and turn-off switching mechanisms that we have not found out so far from the measurement.

Index Terms—Inductive switching, medium voltage, power metal-oxide-semiconductor field-effect transistors (MOSFETs), split gate.

I. INTRODUCTION

EDIUM voltage power metal-oxide-semiconductor field-effect transistors (MOSFETs) have been mainly targeted at dc-dc power supplies, and ac-dc converters [1]–[3]. To reduce the specific resistance (R_{sp}) and the breakdown voltage (BV) by enhancing the drift region's doping concentration, the depth of the trench gate structure was prolonged toward the deep drift region. The poly gate in the deep trench helps the drift region to form a trapezoidal electric field shape acting as a field plate. Although the poly gate below the channel (in the deep trench) is surrounded by relatively thick oxide which would be able to lower the parasitic capacitance value, the gate-to-drain capacitance ($C_{GD,Sh}$) will not be ignorable owing to the large shielded area [1]. For this reason, the poly field plate is separated from the poly gate by a thick oxide (split-gate) and it is connected to the source terminal

Manuscript received 2 May 2022; revised 11 June 2022; accepted 30 June 2022. Date of publication 21 July 2022; date of current version 23 August 2022. This work was supported in part by KENTECH under Research Grant KRG2021-01-001, in part by the Korea Institute of Energy Technology Evaluation and Planning (KETEP) funded by the Korea Government under Grant 20224000000100 (GAMS Convergence Course for Intelligent Electricity Safety Human Resources), and in part by the National Research and Development Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Science and Information and Communications Technology (ICT) under Grant NRF-2022M3I8A1077252. The review of this brief was arranged by Editor S. N. E. Madathil.

The author is with the KENTECH Institute for Grid Modernization, Korea Institute of Energy Technology (KENTECH), Naju, Jeollanam 58330, Republic of Korea (e-mail: h.kang@kentech.ac.kr).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2022.3190827.

Digital Object Identifier 10.1109/TED.2022.3190827

(a) (b) I_{c} I_{p} I_{p} I_{c} I_{c

Fig. 1. (a) Schematic circuit configuration of trench MOSFETs' inductive switching. (b) Impossible current flow path in power electronics model.

instead of the gate as shown in Fig. 1(a). Therefore, a splitgate configuration, which is now very popular in industries, finally lowers both the R_{sp} and the $C_{GD.Sh}$.

It is believed that the inductive switching behaviors of splitgate MOSFETs are well known because the switching characteristics are very similar to the conventional planar gate power MOSFETs. However, in reality, the knowledge is very limited to the parasitic capacitance models which have been widely used in power electronics [4]. More specifically, power MOS-FETs in power electronics features only three representative capacitance: gate-to-source (C_{GS}), gate-to-drain ($C_{GD.Sh}$), and drain-to-source ($C_{\rm DS}$). During the turn-off inductive switching, as the drain voltage increases, some portion of the drain current will flow from the drift region to the shielded source region across the thick oxide [dotted arrow, $C_{\rm DS}$ displacement current in Fig. 1(a)]. At the same time, a part of the $C_{\rm DS}$ displacement current will be transformed into a source-to-gate displacement current because the gate and the shielded source region are separated by an oxide. If the displacement current path (dotted arrow) shown in Fig. 1(a) is redrawn to the conventional power electronics model, the current path will be like Fig. 1(b), i.e., with a conventional three-terminal measurement, those complicated current paths are nearly impossible to be detected. In 2014, Roig et al. [5] schematically modeled the shielded gate with a parasitic $C_{\text{GD,Sh}}$. However, the detailed current flow mechanism across the shielded gate was not explained. Other studies have been focusing on mostly lowering the static and dynamic figures of merits (FOMs) or improving the dynamic ruggedness [6]–[8].

To secure a thorough understanding and deeper insight into the split-gate's switching behavior, the contact of the device needs to be specified as six terminals as shown in Fig. 1(a). The gate current (I_G) is consisting of the gate-to-source (I_{GS}) and gate-to-drain (I_{GD}) current, respectively [9], [10],

1

$$G = I_{\rm GS} + I_{\rm GD.Sh}.$$
 (1)



Fig. 2. Schematic figure of the split-gate and split-source system. In the simulation, the gate region is divided into "GS" and "GD.Sh" terminals. The GS and GD.Sh terminal are separated by 0.1 nm gap.

The source current (I_S) is consisting of the drain-to-source (I_{p+}) , channel $(I_{ch} = I_{n+})$, and shielded source current $(I_{S,S})$, respectively,

$$I_{S} = I_{p+} + I_{ch} + I_{S.S.}$$
(2)

Fig. 2 shows the magnified image of the split-gate system. The gate terminal is divided into GS and GD.Sh regions and the two regions are separated by 0.1 nm gap. The gap must be small enough not to affect the device's performance. The split boundary of the gate region is determined by the boundary between the p-body and the n-drift regions.

II. SIMULATION SETTINGS

The trench gate structure is simulated based on the real fabrication process including the thermal budgets in Magnachip semiconductor. The voltage of the device is 60 V and the driving current density is 500 A/cm².

For inductive switching, device-circuit mixed-mode simulation is employed in sentaurus workbench (SWB) provided by Synopsis Inc. The applied drain-to-drain voltage (V_{DD}) is 40 V and the gate voltage is 10 V. To investigate the device's pure inductive switching, an ideal diode (without reverse recovery) is used on the inductive load. The external gate resistance, R_G , is 10 Ω and the stray inductance at each terminal is ignored. The operating temperature is 300 K.

The physical models in the simulation include Shockley– Read–Hall recombination, doping, and electric field-dependent mobility.

Fig. 3 shows the schematic circuit configuration of the trench gate MOSFET where two capacitance components, $C_{\text{DS,S}}$ (drain-to-shielded source) and $C_{\text{GS,S}}$ (gate-to-shielded source) are added. A portion of the gate current (I_G) directly flows across the thick oxide region and shielded source contact as a form of $I_{\text{GS,S}}$. Therefore, the $I_{\text{GS,S}}$ actually does not account for the gate-to-drain displacement current. The I_D and the $I_{\text{GD,Sh}}$ can be transformed into the displacement current between the drain-to-shielded source current. It should be noted that I_{GS} in this article is the current across the gate terminal and n+ source and p-body region. The current across the gate and the shielded source does not account for the I_{GS} .

III. TURN-ON SWITCHING

For turning on the trench MOSFET, as shown in Fig. 4, the gate current, I_G , and the drain current, I_D , flow through the



Fig. 3. Schematic circuit configuration of the trench MOSFET with six terminal current.



Fig. 4. (a) Schematic current flow path in the trench MOSFET during the turn-on inductive switching. (b) Kirchhoff's current rule in power electronics model.

source, I_S

$$I_G + I_D = I_S \tag{3}$$

i.e., according to Kirchhoff's rules, the sum of the input current $(I_G + I_D)$ is the same as the sum of the output current (I_S) .

Fig. 5 shows the voltage and the current waveforms during the turn-on inductive switching.

 t_0-t_1 : The gate voltage increases from 0 V to the threshold voltage, V_{TH} (1.5 V). Both the I_{GS} and $I_{\text{GD.Sh}}$ flow into the gate terminal to charge the gate oxide. The gate displacement current ($I_G = I_{\text{GS}} + I_{\text{GD.Sh}}$) from the gate oxide flows through the source terminal ($I_G = I_S$). It should be noted that a part of the gate current flows across the thick split gate oxide and the current flows through the buried source terminal ($I_{\text{S.S}}$). The detailed current flows in the trench MOSFET in this period are shown in Fig. 6.

 t_1-t_2 : The gate voltage exceeds the V_{TH} and the drain current starts flowing across the channel. The drain current continuously increases until it reaches 50 A (500 A/cm²). The gate current (I_G) keeps flowing into both the GS and GD.Sh terminal to charge the gate-to-source and the gate-todrain capacitance. Meanwhile, a part of the $I_{\text{GD.Sh}}$ flows across the thick shielded oxide and reaches the shielded source (S.S)



Fig. 5. Current and voltage waveforms during the turn-on inductive switching of the trench MOSFET.



Fig. 6. Schematic turn-on current flows in the trench MOSFET during t_0-t_1 .



Fig. 7. Schematic turn-on current flows in the trench MOSFET during t_1-t_2 .



Fig. 8. Schematic turn-on current flows in the trench MOSFET during t_2-t_3 .

terminal. Unlike t_0-t_1 period, the $I_{GD.Sh}$ current on the shielded source terminal flows into the drift region rather than grounded source. This can be explained by the slightly lowered potential on the interface between the shielded oxide and the drift region owing to the drain current flow. The detailed current flow in the trench MOSFET is shown in Fig. 7.

 t_2-t_3 : When the drain current level reaches 50 A (500 A/cm²), the drain voltage starts decreasing and the most of the gate current flows through the GD.Sh terminal. Due to the decrease in the drain voltage, the depletion in the drift region is continuously removed. The recession of the depletion in the drift region can be established by two displacement current (charging the parasitic capacitances): 1) the capacitance between the shielded source terminal and the drift region and 2) the capacitance between the p-body (p+ terminal on the source) and the drift region. Therefore, the source current flows into both the p+ and the S.S terminal. As shown in Figs. 4 and 7, the current direction of the I_{p+} and the $I_{S.S}$ is negative. These displacement current finally flow across the channel ($I_{n+} = I_{CH}$). This is why the channel

current level is higher than the source current level (I_S). Fig. 8 shows the current flow in the trench MOSFET during t_2-t_3 .

After t_3 : Once the drain voltage reaches its turn-on voltage level, the recession of the depletion in the drift region stops, and the gate voltage increases until it becomes the driving voltage level (10 V). A part of the gate charging current (displacement current) flows across the channel, and the other part flows through the shielded source terminal as shown in Fig. 9.

IV. TURN-OFF SWITCHING

For turning off the trench MOSFET, as shown in Fig. 10, the drain current, I_D , flows through the source, I_S , and the gate, I_G

$$I_D = I_S + I_G \tag{4}$$

i.e., according to Kirchhoff's rules, the sum of the input current (I_D) is the same as the same of the output current $(I_S + I_G)$.

Fig. 11 shows the voltage and the current waveforms during the turn-off inductive switching.



Fig. 9. Schematic turn-on current flows in the trench MOSFET after t_3 .



Fig. 10. (a) Schematic current flow path in the trench MOSFET during turn-off inductive switching. (b) Kirchhoff's current rule in power electronics model.



Fig. 11. Current and voltage waveforms during turn-off inductive switching of the trench MOSFET.

 t_0-t_1 : The gate voltage decreases until it reaches the plateau voltage (t_1) and both the I_{GS} and the $I_{GD,Sh}$ flow out from the gate terminal. The gate current ($I_G = I_{GS} + I_{GD,Sh}$) is a part of the drain current. Due to the decrease in the gate potential, a displacement current from the shielded source terminal flows through the GD.Sh terminal. Fig. 12 shows the current flow in the trench MOSFET during this period.



Fig. 12. Schematic turn-off current flows in the trench MOSFET during t_0-t_1 .



Fig. 13. Schematic turn-off current flows in the trench MOSFET during t_1-t_2 .

 t_1-t_2 : Once the gate voltage reaches its Miller potential, the drain-to-source voltage (V_{DS}) starts increasing and the depletion in the drift region continuously expands. The expansion of the depletion in the drift region requires the displacement current to charge the two parasitic capacitances: 1) the capacitance between the drift region and the shielded source terminal and 2) the capacitance between the p-body (p+ terminal on the source) and the drift region. Therefore, some part of the drain current flows through the S.S and the p+ terminal. The detailed current flow profiles are shown in Fig. 13.

 t_2-t_3 : When the V_{DS} reaches V_{DD} level (40 V), the expanding of the depletion in the drift region stops and the displacement current from the drift region to the S.S and the p+ terminal becomes zero. The gate potential decreases from the plateau voltage to its V_{TH} . Following the decrease in the gate voltage, the drain current (the channel current and the source current) decreases. It should be noted that the decrease in the gate potential leads to a flow of a displacement current from the p-body (p+ terminal) to the gate terminal. This is why the I_{p+} direction is negative as shown in Figs. 11 and 14.



Fig. 14. Schematic turn-off current flows in the trench MOSFET during t_2-t_3 .



Fig. 15. Schematic turn-off current flows in the trench MOSFET after t_3 .

After t_3 : The gate potential falls below the V_{TH} , and the drain current, as well as the channel current, stops flowing. However, there is a negative inflow of the source current from the n+ and p+ terminal. This phenomenon can be explained by the continuously decreasing gate potential. The decrease in the gate potential causes a displacement current from the n+ to GS terminal, and from the p+ to GD.Sh terminal. The potential between gate and the shielded source also decreases presenting a current across the thick oxide between the gate and shielded source. Therefore, the negative inflow of the source current flow process is in Fig. 15.

V. CONCLUSION

Six-terminal analysis for the inductive switching of a trench split gate MOSFET was carried out by adopting a mixed-mode simulation. The six-terminal approach gave us insight into the detailed current flow across the shielded source terminal. More specifically, the displacement current flow from the drain and gate terminals to the shielded source terminal is nearly impossible to be depicted in the conventional power electronics model. From the thorough investigation of the detailed current flows, the understanding of the inductive switching mechanism in a trench split gate MOSFET was improved.

REFERENCES

- R. K. Williams, M. N. Darwish, R. A. Blanchard, R. Siemieniec, P. Rutter, and Y. Kawaguchi, "The trench power MOSFET: Part I—History, technology, and prospects," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 674–691, Mar. 2017, doi: 10.1109/TED.2017.2653239.
- [2] R. Bojoi, F. Fusillo, A. Raciti, S. Musumeci, F. Scrimizzi, and S. Rizzo, "Full-bridge DC–DC power converter for telecom applications with advanced trench gate MOSFETs," in *Proc. IEEE Int. Telecommun. Energy Conf. (INTELEC)*, Oct. 2018, pp. 1–7, doi: 10.1109/INTLEC.2018.8612309.
- [3] P. Anthony, N. McNeill, and D. Holliday, "High-speed resonant gate driver with controlled peak gate voltage for silicon carbide MOSFETs," *IEEE Trans. Ind. Appl.*, vol. 50, no. 1, pp. 573–583, Jan. 2014, doi: 10.1109/TIA.2013.2266311.
- [4] R. J. E. Hueting, E. A. Hijzen, A. Heringa, A. W. Ludikhuize, and M. A. A. Zandt, "Gate-drain charge analysis for switching in power trench MOSFETs," *IEEE Trans. Electron Devices*, vol. 51, no. 8, pp. 1323–1330, Aug. 2004, doi: 10.1109/TED.2004.832096.
- [5] J. Roig, C.-F. Tong, F. Bauwens, R. Gillon, H. Massie, and C. Hoggatt, "Internal self-damping optimization in trench power FETs for high-frequency conversion," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2014, pp. 137–142, doi: 10.1109/APEC. 2014.6803300.
- [6] C. Park, S. Havanur, A. Shibib, and K. Terrill, "60 V rating split gate trench MOSFETs having best-in-class specific resistance and figureof-merit," in *Proc. 28th Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, Jun. 2016, pp. 387–390, doi: 10.1109/ISPSD.2016. 7520859.
- [7] C. F. Tong, I. Cortes, P. A. Mawby, J. A. Covington, and F. Morancho, "Static and dynamic analysis of split-gate RESURF stepped oxide (RSO) MOSFETs for 35 V applications," in *Proc. Spanish Conf. Electron Devices*, Feb. 2009, pp. 250–253, doi: 10.1109/SCED.2009.4800478.
- [8] A. Ferrara, R. Siemieniec, U. Medic, M. Hutzler, O. Blank, and T. Henson, "Evolution of reverse recovery in trench MOSFETs," in *Proc.* 32nd Int. Symp. Power Semiconductor Devices ICs (ISPSD), Sep. 2020, pp. 549–552, doi: 10.1109/ISPSD46842.2020.9170155.
- [9] H. Kang, E. M. Findlay, and F. Udrea, "Mechanisms of asymmetrical turn-on and turn-off and the origin of dynamic CGD hysteresis for hard-switching superjunction MOSFETs," *IEEE Trans. Electron Devices*, vol. 67, no. 6, pp. 2478–2481, Jun. 2020, doi: 10.1109/TED.2020.2989741.
- [10] H. Kang and F. Udrea, "True origin of gate ringing in superjunction MOSFETs: Device view," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5362–5370, May 2021, doi: 10.1109/TPEL.2020.3027663.