Improvements to the Analytical Model to Describe UIS Events

Philipp Steinmann, Satyaki Ganguly, *Member, IEEE*, Brett Hull, Khiem Lam, Daniel Lichtenwalner, *Member, IEEE*, Jae-Hyung Park, Rahul Potera, Jim Richmond, Sei-Hyung Ryu, Shadi Sabri, Charles Van Brackle, Edward Van Brunt, and Elizabeth Williams

***Abstract*— We generalize and refine an analytical model to describe unclamped inductive switching (UIS) events in power MOSFETs and derive a novel, fast method to extract thermal impedance and series resistance from the UIS waveform. We show excellent agreement between model and measurement for SiC MOSFETs. The method allows for the comparison of thermal impedance measurements of packaged parts to that of formerly not easily accessible waferlevel die. The model allows to evaluate UIS ruggedness and provides insight into the nature of ruggedness limitations. A figure of merit for UIS ruggedness is provided and different MOSFET architectures are compared with respect to UIS ruggedness.**

***Index Terms*— Power MOSFET, SiC, thermal model, UIS modeling, unclamped inductive switching (UIS) ruggedness.**

I. Introduction

RUGGEDNESS during unclamped inductive switching (UIS) in power MOSFETs is receiving increasing attention due to their application in the ongoing electrification of many energy processes, especially in the automotive industry [1].

Accurate modeling of UIS events is important for the improvement of UIS ruggedness. The UIS pulse primarily results in a temperature rise due to self-heating, which is determined by the thermal impedance (see Section II). First efforts to model UIS pulses were presented by Blackburn [2] using a square root dependency for the transient thermal impedance. This model was refined by McGloin and Sdrulla [3] by including the breakdown voltage dependencies and expanded by Agnone *et al.* [4] and Ren *et al.* [5].

UIS failure in Si has been shown to be primarily due to parasitic bipolar turn-on [6]. In SiC, it is believed that melting of the backend metallization is the relevant failure mode [5], [7]. We provide strong evidence to further corroborate this theory.

Manuscript received March 4, 2022; revised April 21, 2022; accepted May 6, 2022. Date of publication May 18, 2022; date of current version June 21, 2022. The review of this article was arranged by Editor D. Sheridan. *(Corresponding author: Philipp Steinmann.)*

The authors are with Wolfspeed Inc., Research Triangle Park, NC 27709 USA (e-mail: philipp.steinmann@wolfspeed.com).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2022.3174516.

Digital Object Identifier 10.1109/TED.2022.3174516

In this article, we generalize the UIS model as described, e.g., in [5] for any possible transient thermal impedance functions and show how to retrieve the relevant parameters from the UIS waveform, namely, thermal impedance and series resistance. Hereby, the temperature coefficients of UIS avalanche voltage, BVDSS, and series resistance are measured, compared, and used as input parameters for the model. Next, we apply the model to establish a formula that describes UIS failure dependency on peak current and voltage rating. Finally, we compare the model to measured UIS events and show excellent agreement. This will allow screening of weak parts and can be used to confirm the abovementioned UIS failure mechanism in SiC.

II. Model

The voltage waveform $V(t)$ of a UIS event is primarily a function of the temperature rise $\Delta T(t)$ due to self-heating and the current $I(t) = I_p(1 - (t/\tau_{\text{av}}))$ [2], where I_p is the peak current and τ_{av} is the duration of the UIS pulse. Okuto [8] proposed to write $V(t)$ as

$$V(t) = V_{\text{br}}(1 + \beta \Delta T) + r_s I(t)(1 + \gamma\, \Delta T) \tag{1}$$

whereby V_{br} is the voltage of avalanche onset and β its temperature coefficient. Here, ohmic behavior is assumed for the voltage drop along the current path with a series resistance r_s. The temperature coefficient of r_s is marked by γ. We will use this formula as have several authors before [3], [5]. When we substitute $I(t)$ by $I_p(1 - (t/\tau_{\text{av}}))$ in (1), we can simplify the temperature dependency of the resistance by ignoring second-order effects: $\gamma\, \Delta T(1 - (t/\tau_{\text{av}})) \approx (1/2)\gamma\, \Delta T$ (see Appendix A)

$$V(t) = V_{\text{br}}(1 + \beta \Delta T) + r_s I_p\left(1 - \frac{t}{\tau_{\text{av}}}\right) + \frac{1}{2} r_s I_p \gamma\, \Delta T. \tag{2}$$

The temperature waveform $\Delta T(t)$ during a UIS event is a solution of the heat equation, which can be integrated with the help of the transient thermal impedance z_{th} [4], [9]

$$\Delta T(t) = \int_0^t P(t') \frac{d}{dt} z_{\text{th}}(t - t') dt' \tag{3}$$

where $P(t) = V(t)I(t)$ is the power dissipated at the junction and t' is the variable of integration. The integral in (3) can be integrated by parts. Then, we take advantage of

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

$z_{\text{th}}(0) = 0$ and replace $V(t)$ by its average $\overline{V} = \int V dt/\tau_{\text{av}}$, which is an excellent approximation for voltage ranges of practical relevance. This allows us to rewrite (3)

$$\Delta T(t) = V(0) I_p z_{\text{th}}(t) - \frac{\overline{V} I_p}{\tau_{\text{av}}} \int_0^t z_{\text{th}}(t') dt'. \tag{4}$$

We use this expression for ΔT in (2), differentiate, and get a differential equation for z_{th}

$$\frac{d}{dt} z_{\text{th}}(t) - \frac{\overline{V}}{\tau_{\text{av}} V(0)} z_{\text{th}}(t) = \frac{1}{\left(\beta V_{\text{br}} + \frac{1}{2}\gamma r_s I_p\right) V(0)} \left(\frac{\frac{d}{dt} V}{I_p} + \frac{r_s}{\tau_{\text{av}}} \right) \tag{5}$$

which can be solved for z_{th}

$$z_{\text{th}}(t) = \frac{1}{\beta V_{\text{br}} I_p + \frac{1}{2}\gamma r_s I_p^2} \times \left(\frac{V(t) - V(0)}{V(0)} + \left(\frac{\overline{V} - V(0)}{V(0)} + \frac{r_s I_p}{\overline{V}} \right) \times \left(e^{\frac{\overline{V}}{V(0)} \frac{t}{\tau_{\text{av}}}} - 1 \right) \right). \tag{6}$$

Now, we have an explicit analytical expression, allowing for the calculation of the thermal impedance z_{th} from the voltage waveform $V(t)$. The series resistance r_s can be obtained in two ways: either it is extracted with the help of (2) at $t = 0$ via $r_s = (\Delta V(0)/\Delta I_p)$ from experimental UIS waveforms acquired at different I_p values or, alternatively, r_s can be extracted from a single UIS event, if we use additional assumptions about z_{th}, as we shall see next.

z_{th} is modeled by a thermal equivalent network (Cauer network) of several thermal resistances $r_{\text{th},i}$ and capacitances $c_{\text{th},i}$ in a low-pass filter series. Solving the network for z_{th} yields

$$z_{\text{th}}(t) = \sum r_{\text{th},i} \left(1 - e^{-\frac{t}{r_{\text{th},i} c_{\text{th},i}}} \right). \tag{7}$$

We want to apply this formula to UIS waveforms. Typically, τ_{av} is less than a few 100 μs. In this range (7) can be approximated by

$$z_{\text{th}}(t) = \frac{t^q}{\tilde{c}}. \tag{8}$$

For a given thermal equivalent network, q and $\tilde{c}$ can be extracted from $r_{\text{th},i}$ and $c_{\text{th},i}$ by means of linear regression of $\ln(z_{\text{th}}(t))$ versus $\ln(t)$. The intensive, dimensionless parameter q is typically assumed to be $(1/2)$ [2], but we extracted q of $\approx$0.4 to $\approx$0.9 from our z_{th} measurements. The extensive, modified heat capacitance $\tilde{c}$ is typically $\tilde{c} < 0.1\ Ws^q/K$. This knowledge about the nature of z_{th} can now be utilized to determine r_s in (6). This can be achieved by fitting (6) to a t^q power law and varying r_s until the regression coefficient R^2 is optimized.

Furthermore, substituting $z_{\text{th}}(t)$ by (8) into (3) and (1) yields explicit expressions for ΔT and $V(t)$

$$\Delta T(t) = \frac{\overline{V} I_p}{\tilde{c}} t^q \left(1 - \frac{t}{(1+q)\tau_{\text{av}}} \right). \tag{9}$$

This expression allows us to calculate the maximum temperature rise

$$\Delta T_{\max} = \frac{\overline{V} I_p}{\tilde{c}} \frac{q^q}{(1+q)} \tau_{\text{av}}^q. \tag{10}$$

Now, we can use $E = (1/2)\overline{V} I_p \tau_{\text{av}}$ and solve for τ_{av} and then substitute it in (10) to express the avalanche energy (E) dissipated during a UIS event in terms of $\Delta T_{\max}$

$$E = \frac{(1+q)^{\frac{1}{q}}}{2q} \Delta T_{\max}^{\frac{1}{q}} \tilde{c}^{\frac{1}{q}} \overline{V}^{1-\frac{1}{q}} I_p^{1-\frac{1}{q}}. \tag{11}$$

This expression provides insight into the failure mechanism of power MOSFETs due to UIS stress. If failure is due to the MOSFET reaching a critical temperature, the failure energy must show a dependency of E on I_p like in (11). We shall use (11) in Section IV to show this. Moreover, (11) provides a possible UIS figure of merit, which allows for the comparison of MOSFET architectures with differently rated operating voltages and currents.

III. Comparison to Measured UIS Waveforms

Now, we shall compare the model described in Section II to measured UIS data. We measured two of our commercially released Gen3 (see [10]) MOSFET products C3M0017120 (17 mΩ) and C3M0075120 (75 mΩ) with an ITC-UIS station and recorded $V(t)$ with an oscilloscope. Measurement noise was removed with a kernel smoother function, and then, $t = 0$ and $t = \tau_{\text{av}}$ were determined by filtering dV/dt between the 1st and the 99th percentile. Thus, obtained $V(t)$ allows for the calculation of $V(0)$. Repeating this procedure at different peak currents I_p allows to extrapolate to $V(0)$ at $I_p = 0$. This value $V(t = 0, I_p = 0)$ is the equivalent of the normal avalanche breakdown voltage BVDSS obtained through an I–V sweep. The slope of this linear fit represents r_s as introduced in (1). Measuring UIS waveforms at different temperatures T and repeating this procedure for each T allow for the extraction of β and γ from (2).

Fig. 1 shows on the top the values for $V_{\text{br}} = V(t = 0, I_p = 0)$ and BVDSS measured at different temperatures for 14 samples from the two different devices. Solid lines represent UIS extracted values and dashed lines represent BVDSS from I–V sweeps. The slopes of these lines allow for the extraction of β. Both methods show very similar values: 120 ppm/K for the UIS-extracted avalanche temperature coefficient and about 160 ppm/K for the I–V-sweep-extracted coefficient with no significant difference between the two transistor types. This is as expected since both describe the same vertical avalanche process.

On the bottom of Fig. 1, we plot measured $r_s = dV/dI$ as a function of temperature. Here, there is a significant difference between the transistor types. C3M0017120 has r_s of $\approx$0.4 Ω and γ around -300 ppm/K, whereas C3M0075120 has an r_s of $\approx$1.1 Ω and γ around -800 ppm/K. We observe a good qualitative scaling of r_s with *RDSon* as one would expect. We speculate that the different values of γ for the two transistor types might be due to different field enhancements due to different corner roundings and curvatures of the diffused *P-WELL*.

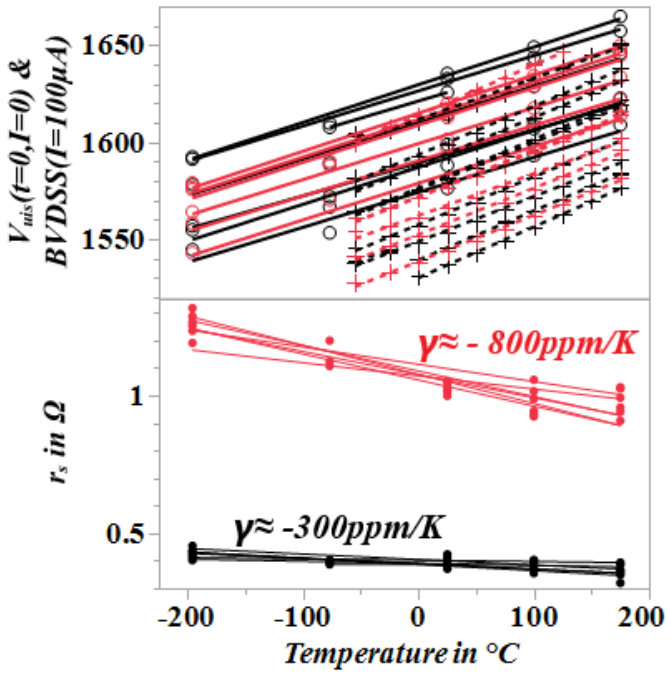

Fig. 1. Top: $V_{\text{br}} = V(t = 0, I_p = 0)$ (solid) and BVDSS (dashed) versus T with a slope of β for 14 samples from two different transistor types C3M0017120 (black) and C3M0075120 (red). Bottom: r_s versus T with slopes of γ.

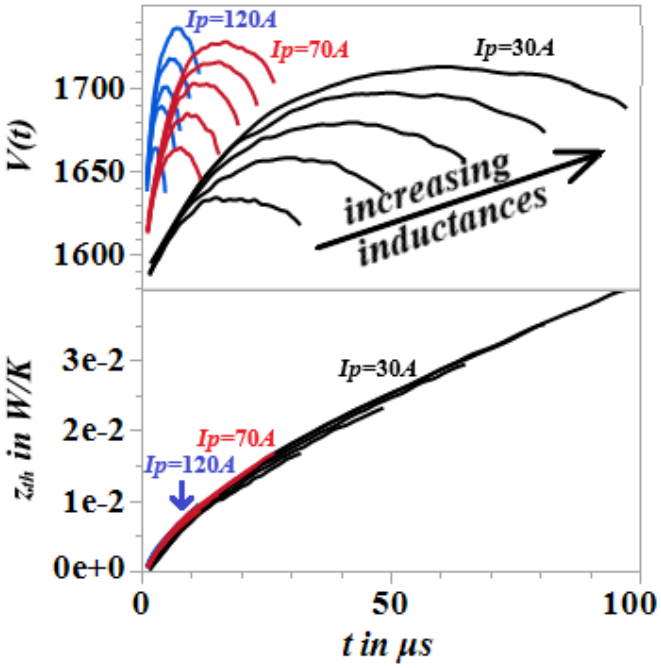

Fig. 2. Top row: $V(t)$ from UIS pulses from a C3M0017120 MOSFET with $I_p = 30$ A (black), $I_p = 70$ A (red), $I_p = 120$ A (blue), and each of the five different inductance values. Bottom row: z_{th} in K/W calculated from curves above with the help of (6); blue curve buried behind red curve.

Now, equipped with $V(t)$, $V(0)$, and $\overline{V}$ [from $V(t)$] and r_s, β, and γ, we can proceed to calculate z_{th} according to (6). Fig. 2 shows $V(t)$ from UIS pulses from a C3M0017120 MOSFET with $I_p = 30$ A (black), $I_p = 70$ A (red), and $I_p = 120$ A (blue), each with five different inductance values: 1.8–5.4 mH in steps of 0.9, 0.3–0.7 mH in steps of 0.1, and 0.06–0.18 mH in steps of 0.03 mH, respectively. Fig. 2 also shows z_{th}, calculated from the curves in the upper half of Fig. 2 with the help of (6). In this plot, r_s was extracted as described previously by variation until R^2 was optimized. Since all waveforms under vastly different conditions reproduce the same thermal impedance, this plot illustrates the validity of (6).

Next, we compare z_{th} from (6) to the standard z_{th} measurement method (transient dual interface (TDI), JESD 51-14 [13]), based on body diode V_f as a thermometer. Fig. 3 shows z_{th} calculated from (6) for the transistors from Fig. 1. Our new measurement method shows qualitative agreement between the two different methods. However, the UIS-extracted z_{th} curves are slightly steeper. The TDI method reproduces an exponent q of exactly $(1/2)$, which was entered into the model to begin with. From [13], "due to the electrical disturbances at the beginning of the measurement *(with the TDI method)*, the signal has to be discarded for all points of time t smaller than a cutoff time t_{cut}…$(t)^{1/2}$ can be used to extrapolate to …$t = 0$." In our method, based on (6), the exponent q is independently measured and comes out higher ($q \sim 0.7$).

This new method for extracting z_{th} is not only very fast but also allows for the measurement of z_{th} in nonstandard environments, like at wafer level or open cavity packages.

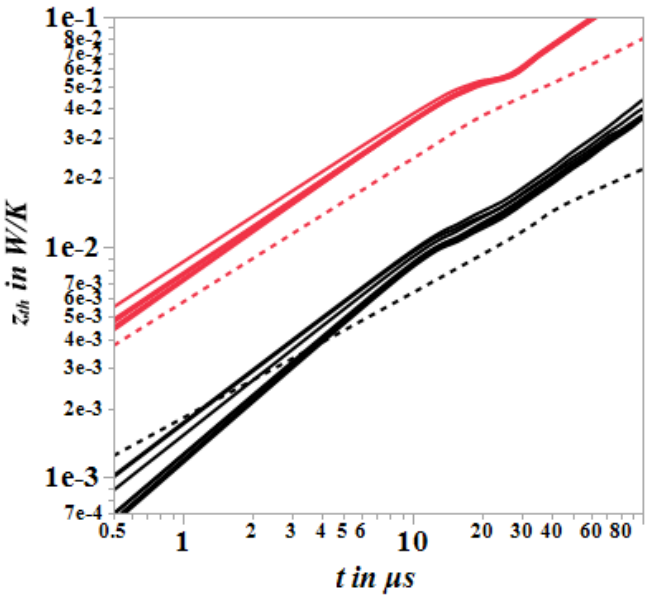

Fig. 3. z_{th} extracted from UIS waveform with (6) for the transistors from Fig. 1, again C3M0017120 (black, $I_p = 70$ A) and C3M0075120 (red, $I_p = 20$ A). Dashed Lines show data sheet reference for the two products based on TDI measurements.

Fig. 4 shows a comparison of z_{th} readouts calculated with (6) from UIS-waveforms at $t = 10$ μs for three different cases for the same 17 mΩ product: on wafer level, standard overmold, and open cavity package. For all three cases, β and γ were assumed to be the same as extracted according to Fig. 1 from packaged parts. It can be seen that in a wafer-level setup,

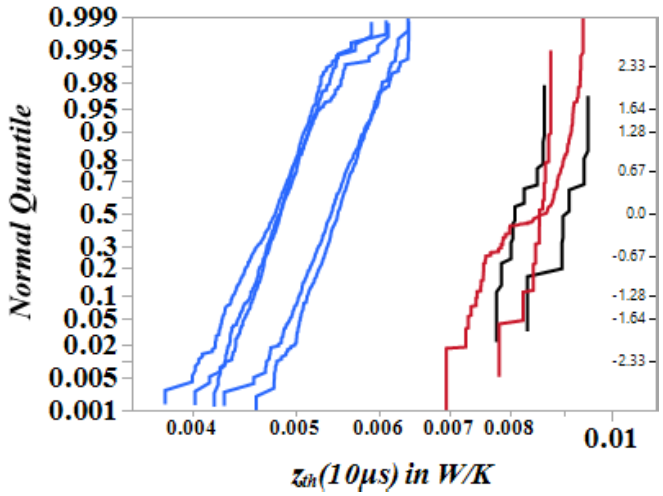

Fig. 4. Cumulative $z_{\text{th}}(t = 10\ \mu s)$ for C3M0017120 transistors in three different setups: wafer level (blue, five wafers, ~500 sites, and two different frontside platings), overmolded package (red, from two different wafers 500 and 189 parts), and open cavity package (black, from two different wafers, 32 and 27 parts).

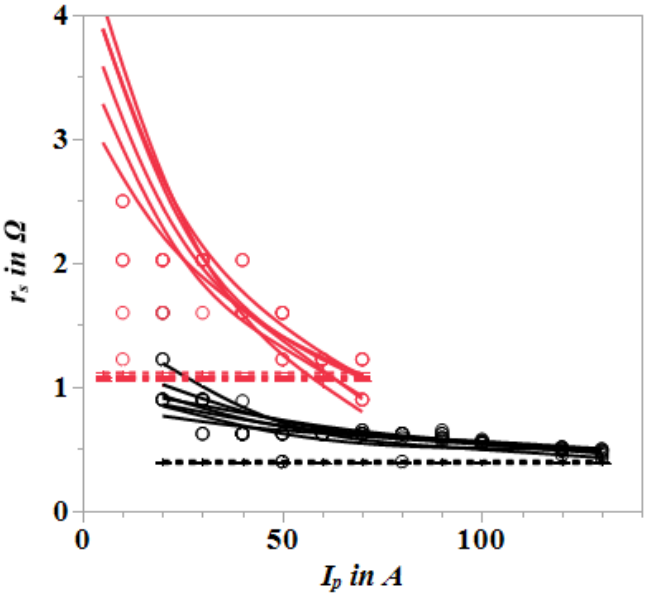

Fig. 5. r_s from varying r_s in (6) and optimizing R^2 (solid lines) and r_s from Fig. 1 being the slope dV/dI (dashed lines) for the transistors from Fig. 1, again C3M0017120 (black) and C3M0075120 (red).

z_{th} is a factor of 1.5 lower than packaged parts and there is little difference between open cavity and fully overmolded packages.

Finally, we want to compare the two different methods for extracting the series resistance r_s from the slope dV/dI and r_s from optimizing R^2. Each circle in Fig. 5 represents an r_s value extracted from a UIS curve at a given I_p with (6) and optimized with respect to R^2, the solid lines show a spline through those values. The dashed lines show r_s from Fig. 1. The agreement at higher peak currents is very good. This is yet another confirmation of the consistency of the model. The nonlinear nature of the series resistance becomes apparent with the method of (6), which shows the higher values for r_s for lower peak currents I_p.

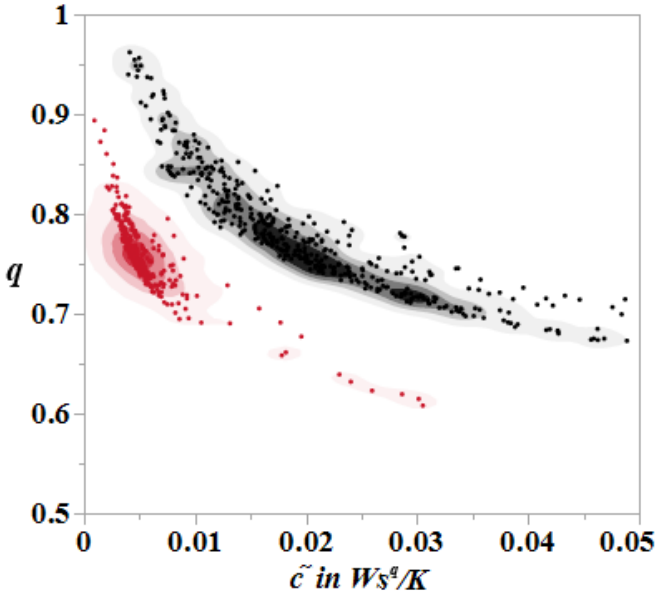

Fig. 6. q versus $\tilde{c}$ 30 packaged MOSFETs of each of the devices C3M0017120 (black) and C3M0075120 (red) by measuring z_{th} and fitting q and $\tilde{c}$ according to (8).

IV. Approximation for z_{TH}

In Section II, we discussed an approximation for z_{th}, which we want to apply to experimentally measured z_{th} curves. We measured 30 packaged MOSFETs of each of the devices C3M0017120 and C3M0075120, extracted first z_{th} (6) and then q and $\tilde{c}$ according to (8) by fitting slope and intercept of the log–log of z_{th} against t. In Fig. 6, the results are plotted together with their bivariate densities. The densities peak for q around 0.75 for both devices, whereas $\tilde{c}$ differs between the two devices. For C3M0017120, we get approximately 0.02 $Ws^{0.75}/K$ and for C3M0075120 approximately 0.005 $Ws^{0.75}/K$. Thus, we see that q is indeed an intrinsic parameter, whereas $\tilde{c}$ scales with the MOSFET area.

Next, we can apply these measurements to gain some insight into the failure mechanism for UIS. UIS pulses dissipate energy in the MOSFET and ruggedness, with regard to this energy, described by an upper limit, is an important design parameter for power circuits. This upper limit can be explored by repeating pulses and ramping inductances at a constant peak current I_p and thereby establishing a function of the UIS ruggedness energy $E_{\max}$ as a function of I_p. Wang and Jiang [11], and Gao *et al.* [12] reported an inverse proportional dependency $E_{\max} \propto I_p^{-\kappa}$, with $\kappa \approx 0.5$.

In Fig. 7, we report UIS ruggedness data of several MOSFETs, including the designs discussed above from ramping inductances L at constant current peaks I_p. We plot the median of the areal density $e_{\max}$ of $E_{\max}$ as a function of the areal density j_p of I_p. The fit lines show an approximate relationship of the type $e_{\max} = 0.22\ \text{JA}^{0.5}/\text{mm}^3 \times j_p^{-0.5}$. This relationship is essentially the same for all MOSFET types, independent of their area. It can now be compared to (11).

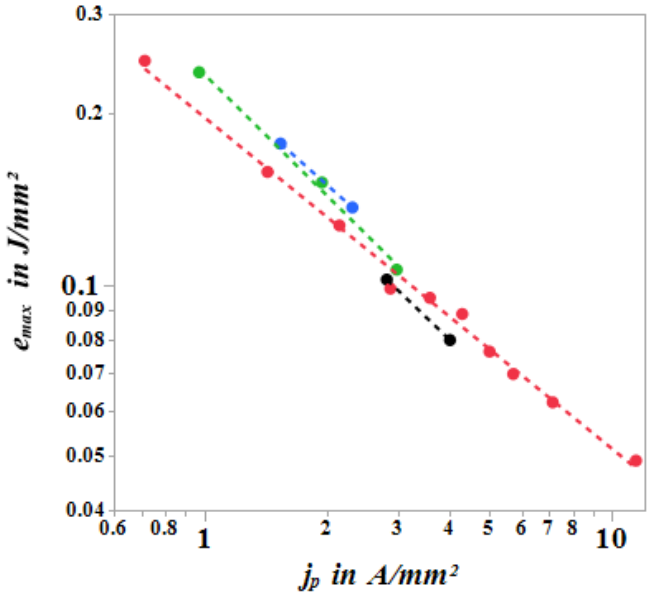

Fig. 7. Median of the areal density of $e_{\max}$ in J/mm^2 of four different MOSFET layouts as a function of the areal density of j_p in A/mm^2, C3M0016120 (blue), C3M0017120 (black), C3M0021120 (green), and C3M0075120 (red).

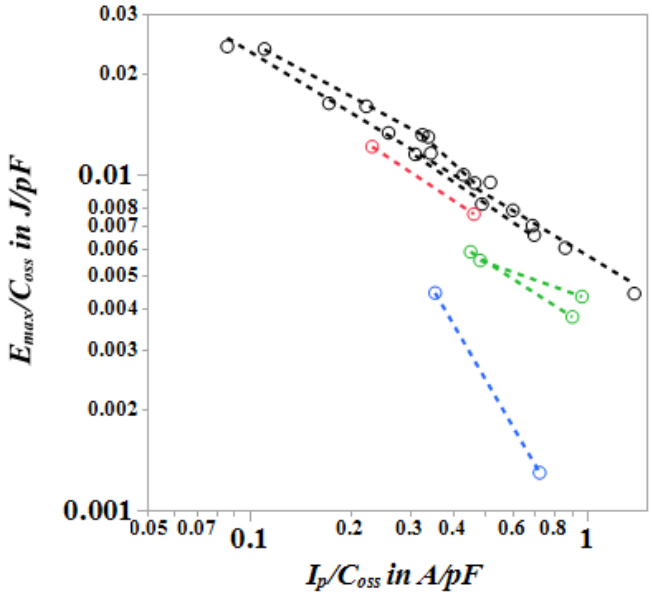

Fig. 8. $E_{\max}/C_{\text{oss}}$ in J/pF of several different MOSFET layouts from different vendors as a function of I_p/C_{oss} in A/pF. Wolfspeed (black, same parts as in Fig. 7), Vendor 1 (red, planar, $Rds_{on} = 80$ mΩ, $C_{\text{oss}} = 80$ pF), Vendor 2 (green, trench, $Rds_{on} = 30, 45$ mΩ, $C_{\text{oss}} = 116$, and 115 pF), and Vendor 3 (blue, trench, $Rds_{on} = 40$ mΩ, $C_{\text{oss}} = 76$ pF).

Since $\kappa \approx 0.5$ and $q = (1/1+\kappa)$, we get $q \approx 0.67$, which is close to the measured q from Fig. 6.

Now, we are in a position where we can use (11) to draw conclusions. Indeed, in Fig. 7, $E_{\max}$ shows a dependency on I_p as predicted by (11). Furthermore, we can extract the critical maximum temperature $\Delta T_{\max,\text{crit}}$ at which failure occurs, e.g., melting of the metal lines. First, (11) can be rewritten in areal density form

$$e_{\max} = \frac{(1+q)^{\frac{1}{q}}}{2q} \Delta T_{\max,\text{crit}}^{\frac{1}{q}} \bar{\tilde{c}}^{\frac{1}{q}} \overline{V}^{1-\frac{1}{q}} j_p^{1-\frac{1}{q}}. \tag{12}$$

Here, $\bar{\tilde{c}} = \tilde{c}/A$ is the modified heat capacity density (A is die area). Resolving for $\Delta T_{\max,\text{crit}}$ yields

$$\Delta T_{\max,\text{crit}} = \frac{2^q q^q}{1+q} \frac{1}{\bar{\tilde{c}}} e_{\max}^q \overline{V}^{1-q} j_p^{1-q}. \tag{13}$$

Extracting $\bar{\tilde{c}}$ from Fig. 6 and $\overline{V}$ from Fig. 2, we calculate $\Delta T_{\max,\text{crit}} \approx 800$ K. This is in line with recent reports from [14].

A fair comparison of UIS ruggedness of MOSFETs with different architectures, ratings, or from different vendors is difficult since the measurement conditions vary. Given the results from above, we propose to use the fit of $\log(e_{\max})$ versus $\log(j_p)$ as a figure of merit to evaluate UIS ruggedness. We acquired parts from three different vendors and measured their ramp to breakdown energies for 30 MOSFETs each, on the same station as for the Wolfspeed parts. Since the die areas of the parts from the vendors are unknown, we decided to use C_{oss} from the products' data sheet instead, which we found scales best with the actual die area. Fig. 8 shows a comparison of the median ramp to UIS breakdown energy densities from the different products similar to Fig. 7, whereby $E_{\max}$ and I_p were divided by C_{oss} instead of die area. It can be seen that the Wolfspeed parts allow for a higher energy density at a given current density before failure occurs.

V. Conclusion

We have derived a simple analytical model for UIS pulses, which improves substantially over older models. We have derived a new, accurate and fast method to extract the transient thermal impedance z_{th}, series resistance r_s, and temperature coefficients β for avalanche voltage and γ for series resistance from the UIS waveform. We showed the consistency of this method and applied it to show differences in thermal impedance between wafer-level and packaged parts. The new model provides insight into the physical nature of the failure mechanism during UIS pulses. We use this method to propose a new figure of merit to compare MOSFETs with respect to ruggedness.

Appendix A
Justification for $I_{\text{EFF}} = I_p/2$ in (2)

We can use (9) to calculate I_{eff} in (2)

$$\begin{aligned}
&\frac{\int_0^{\tau_{\text{av}}} \Delta T \left(1 - \frac{t}{\tau_{\text{av}}}\right) dt}{\int_0^{\tau_{\text{av}}} \Delta T\, dt} \\
&= \frac{\frac{\overline{V} I_p}{\tilde{c}} \int_0^{\tau_{\text{av}}} t^q \left(1 - \frac{t}{(1+q)\tau_{\text{av}}}\right)\left(1 - \frac{t}{\tau_{\text{av}}}\right) dt}{\frac{\overline{V} I_p}{\tilde{c}} \int_0^{\tau_{\text{av}}} t^q \left(1 - \frac{t}{(1+q)\tau_{\text{av}}}\right) dt} \\
&= \frac{q+2}{q^2+4q+3} \approx \frac{1}{2}
\end{aligned} \tag{14}$$

for typical values of $0.4 < q < 0.9$.

REFERENCES

[1] J. W. Palmour, "Silicon carbide power device development for industrial markets," in *IEDM Tech. Dig.*, Dec. 2014, pp. 8193–8205, doi: 10.1109/IEDM.2014.7046960.

[2] D. L. Blackburn, "Power MOSFET failure revisited," in *Proc. 19th Annu. IEEE Power Electron. Spec. Conf.*, vol. 2, Apr. 1988, pp. 681–688, doi: 10.1109/PESC.1988.18196.

[3] J. McGloin and D. Sdrulla, "Estimating the temperature rise of power MOSFETs during the UIS test," in *Proc. 7th Annu. Appl. Power Electron. Conf. Expo.*, Feb. 1992, pp. 448–453, doi: 10.1109/APEC.1992.228375.

[4] A. Agnone, F. Chimento, S. Musumeci, A. Raciti, and G. Privitera, "A new thermal model for power MOSFET devices accounting for the behavior in unclamped inductive switching," in *Proc. IEEE Power Electron. Specialists Conf.*, Jun. 2007, pp. 1006–1012, doi: 10.1109/PESC.2007.4342128.

[5] N. Ren *et al.*, "Investigation on single pulse avalanche failure of SiC MOSFET and Si IGBT," *Solid-State Electron.*, vol. 152, pp. 33–40, Feb. 2019, doi: 10.1016/j.sse.2018.11.010.

[6] R. R. Stoltenburg, "Boundary of power-MOSFET, unclamped inductive-switching (UIS), avalanche-current capability," in *Proc. 4th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 1989, pp. 359–364, doi: 10.1109/APEC.1989.36987.

[7] D. Urciuoli, S. Ryu, D. C. Capell, D. Ibitayo, G. Koebke, and C. W. Tipton, "Performance of a 1-kV, silicon carbide avalanche breakdown diode," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4643–4645, Sep. 2015, doi: 10.1109/TPEL.2015.2403199.

[8] Y. Okuto, "Junction temperatures under breakdown condition," *Jpn. J. Appl. Phys.*, vol. 8, no. 7, pp. 917–922, Jul. 1969, doi: 10.1143/JJAP.8.917.

[9] A. Castellazzi, M. Ciappa, W. Fichtner, G. Lourdel, and M. Mermet-Guyennet, "Comprehensive electro-thermal compact model of a 3.3 kV-1200 A IGBT-module," in *Proc. Int. Conf. Power Eng., Energy Electr. Drives*, Apr. 2007, pp. 405–410, doi: 10.1109/POWERENG.2007.4380225.

[10] J. W. Palmour *et al.*, "Silicon carbide power MOSFETs: Breakthrough performance from 900 V up to 15 kV," in *Proc. IEEE 26th Int. Symp. Power Semiconductor Devices IC's (ISPSD)*, Jun. 2014, pp. 79–82, doi: 10.1109/ISPSD.2014.6855980.

[11] J. Wang and X. Jiang, "Review and analysis of SiC MOSFETs ruggedness and reliability," *IET Power Electron.*, vol. 13, no. 3, pp. 445–455, Aug. 2019, doi: 10.1049/iet-pel.2019.0587.

[12] Z. Gao, Q. Guo, N. Ren, and K. Sheng, "Experimental investigation on failure mechanism of SiC power MOSFETs under single pulse avalanche stress," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl. Asia (WiPDA Asia)*, Sep. 2020, pp. 1–5, doi: 10.1109/WiPDAAsia49671.2020.9360260.

[13] *Transient Dual Interface Test Method for the Measurement of the Thermal Resistance Junction-to-Case of Semiconductor Devices With Heat Flow Through a Single Path*, JEDEC Solid State Technology Association, Standard JESD51-14, 2010.

[14] K. Yao, H. Yano, and N. Iwamuro, "Impact of negative gate bias and inductive load on the single-pulse avalanche capability of 1200-V SiC trench MOSFETs," *IEEE Trans. Electron Devices*, vol. 69, no. 2, pp. 637–643, Feb. 2022, doi: 10.1109/TED.2021.3133201.