High-Speed Steep-Slope GaInAs Impact Ionization MOSFETs (I-MOS) With $SS = 1.25$ mV/dec—Part II: Dynamic Switching and RF Performance

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***Abstract*— Part I of this work described narrow bandgap GaInAs-based I-MOS devices with a minimum steep slope $SS_{min} = 1.25$ mV/dec maintained over 4 orders of magnitude in drain current, I_{ON}/I_{OFF} ratios $>10^6$ at 300 K ($>10^9$ at 15 K), and low operating voltages for a gate length of $L_G = 100$ nm. Part II focuses on the device time-domain switching capabilities and RF performance. Digital switching tests using a hybrid connected inverter reveal excellent capabilities for high clock rate operation. Simple circuit estimates indicate that the present 100 nm GaInAs I-MOS can operate with clock frequencies >10 GHz. The impact-ionization-induced hysteresis in the I_D–V_{GS} I-MOS characteristics does not play any role in dynamic switching of a digital inverter: the *n*-channel pull-down transistor turns on with a steep slope, but turns off classically with a higher threshold voltage which reduces the dynamic power dissipation per switching cycle. Factors impacting GaInAs I-MOS reliability are considered, and a physically motivated approach to enhance the reliability of III–V MOSFETs is proposed. We show that GaInAs-based I-MOS devices offer high analog cutoff frequencies and low-noise characteristics, suggesting applicability for digital and RF applications on a single technological platform. When benchmarked against other steep-slope technologies, GaInAs I-MOS shows the strongest steep slope, competitive I_{ON}/I_{OFF} ratios, and lowest operating voltage of any I-MOS transistor to date, without any back-gate/substrate bias.**

***Index Terms*— Atomic layer deposition (ALD), GaInAs, I-MOS, impact ionization, inverse subthreshold slope (*SS*), MOSFET, RF performance, steep slope.**

I. Introduction

IN PART I of this work, device characterization and TCAD simulations were performed to demonstrate and clarify the steep-slope behavior of GaInAs impact ionization MOSFETs (I-MOS). GaInAs I-MOS devices exhibit an interesting (drain-controlled) dynamic threshold voltage previously shown favorable for low-power logic operation at low drain voltages [1]. The dynamic threshold behavior is examined in more detail using a simple logic inverter. Impact ionization does induce hysteresis in the transfer characteristics when the gate voltage is cycled under a *fixed* high drain voltage V_{DS}: this hysteresis, however, *plays no role* when I-MOS transistors are used in a logic gate because inverter operation involves a varying drain voltage: the *n*-channel pull-down transistor turns on with a steep slope, but turns off classically with a higher threshold voltage which reduces the dynamic power dissipation per switching cycle. The resulting $i_D(t)$ versus $v_G(t)$ trajectory is beneficial for the realization of low-power digital electronics. Preliminary time-domain switching experiments using a hybrid-connected resistive load and ON-wafer devices confirm that GaInAs I-MOS can operate with high clock rates. Factors impacting GaInAs I-MOS reliability are considered, and a physically motivated approach to enhance the reliability of III–V MOSFETs with high-κ gate dielectrics is proposed. For analog applications, GaInAs I-MOS transistors with $L_G = 100$ nm also demonstrate wide bandwidths and low-noise properties with current gain cutoff frequencies f_T of 250 (313) GHz and maximum oscillation frequencies f_{MAX} of 310 (354) GHz at 300 K (15 K), with a room temperature minimum noise figure NF_{MIN} ranging from 0.25 to 1.2 dB over the 8–40 GHz frequency range. The combination of favorable switching and RF performance metrics in GaInAs I-MOS transistors indicates their potential for the realization of mixed-mode analog/digital circuits in a single process platform that is comparatively simpler than those associated with other steep-slope technologies.

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II. Results

A. GaInAs I-MOS Dynamic Switching

In this section, we examine the switching behavior of GaInAs I-MOS devices in more detail, with particular attention to impact-ionization-induced hysteresis in

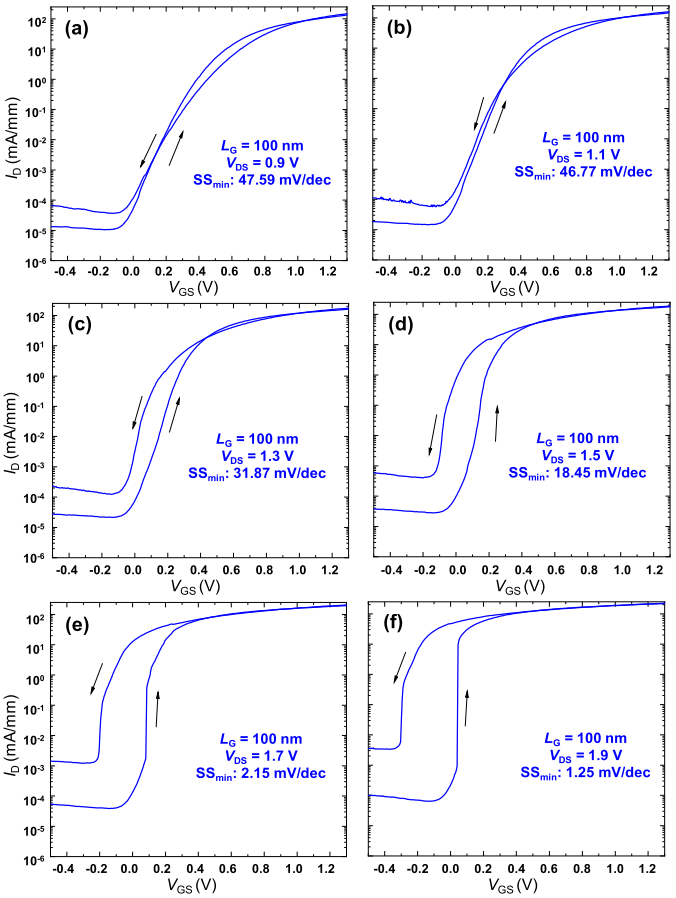

Fig. 1. (a)–(f) 300 K ON/OFF switching characteristics of a GaInAs I-MOS device with $L_G = 100$ nm gate length for various V_{DS} biases (logarithmic scale). A steep slope is observed in both sweep directions. Down-sweep hysteresis is induced when the device is turned off under high-impact ionization conditions. For $V_{DS} < 0.6$ V, I-MOS behaves classically with $SS_{min} = 60$–70 mV/dec (not shown).

the context of dynamic switching of a logic inverter gate.

Let us first consider features of GaInAs I-MOS turn-on behavior. The gate turn-on characteristics shown in Fig. 1(a)–(f) show that the effective threshold voltage (defined at $I_D = 1$ mA/mm) is reduced from $V_T = 0.48$ V when the device operates near classically with $V_{DS} = 0.9$ V, to $V_T = 0.07$ V at $V_{DS} = 1.9$ V when the steep slope is fully developed. The subthreshold characteristics *improve* with increasing V_{DS}: the drain-induced barrier lowering (DIBL) increase in inverse subthreshold slope observed in conventional FETs at higher V_{DS} is suppressed by the steep-slope behavior (also clearly seen in Part I, Fig. 3). This behavior is similar to that of dynamic threshold MOSFETs (DTMOS) engineered (via a body contact) to manifest a reduced threshold voltage for rising gate voltages and a high threshold voltage for a falling gate bias [1]. DTMOS technology is useful in low-power low-voltage VLSI applications by providing a higher current drive than conventional CMOS for rising gate voltages and maintaining low OFF-state currents when the gate voltage drops [2]. Whereas DTMOS uses a body contact (which increases gate capacitance and contributes a static base leakage current) to control the lateral substrate bipolar transistor, GaInAs I-MOS devices display a *natural dynamic threshold effect via* the bipolar action associated with impact ionization generated holes, without the body contact required in DTMOS technology. In contrast to Si or Ge-based I-MOS transistors incorporating lateral gated p-n or p-i-n structures to reduce breakdown voltages [3], GaInAs I-MOS transistors conduct all the way down to $V_{DS} = 0$ V: they are thus compatible with the rail-to-rail operation of conventional CMOS.

When operated under a constant high V_{DS}, the switching characteristics of GaInAs I-MOS devices display a notable hysteresis between the turn-on and turn-off gate sweeps: the hysteresis broadens with V_{DS} (and with shorter gates and lower temperatures associated with higher impact ionization levels). The evolution of hysteresis is detailed in Fig. 1(a)–(f) for $L_G = 100$ nm gates under various drain voltages. Clearly, hysteresis expands in close association with the development of steep-slope behavior. While hysteresis is hardly present at $V_{DS} = 0.9$ V with a minimum observed $SS = 48$ mV/dec [Fig. 1(a)], it becomes pronounced at $V_{DS} = 1.9$ V with a minimum $SS = 1.25$ mV/dec [Fig. 1(f)]. Steep-slope switching behavior is clearly observed in both switching directions. At high V_{DS} in the turn-on gate sweep, devices turn on with a steep slope for a certain gate bias $V_{GS} = V_{T,ON}$. The more negative threshold voltage on V_{GS} down sweep is due to the accumulation of impact-ionization-generated holes under the gate region (as shown in Part I, Fig. 5) when the device is switched from ON to OFF with a high drain-to-source voltage V_{DS}.

The impact-ionization-related hysteresis shown in Fig. 1 *does not* affect the operation of an I-MOS digital steep-slope inverter. This is understood by considering the switching behavior of the resistively loaded I-NMOS pull-down transistor shown in Fig. 2(a). As the gate voltage rises with the pull-down transistor in the OFF-state, the transistor initially experiences a high drain voltage (i.e., logic high output state), and thus turns on according to its steep-slope characteristic for $V_{GS} = V_{T,ON}$. Its drain voltage V_{DS} consequently drops to a low value (logic low output state). For ON-to-OFF switching, the pull-down transistor therefore turns off classically from a low V_{DS} state characterized by a higher threshold voltage $V_{T,OFF} > V_{T,ON}$ (Fig. 2(d), thus replicating DTMOS behavior [2]). The high V_{DS} turn-off trajectory and the steep-slope hysteresis displayed in Fig. 1 *play no role in the operation of an I-MOS transistor inverter*. Stated differently, when used in inverters, I-MOS transistors follow a steep slope to turn on, but turn off according to a low V_{DS} characteristic (i.e., without impact ionization, regardless of material system). The classical turn-off trajectory is advantageous in terms of dynamic power dissipation when compared with devices switching ON/OFF along the same steep slope, because it brings about an earlier drop in drain current and reduces $\int v_D(t) i_D(t) dt$ per switching cycle: we see no advantage in switching off along the steep slope. The dual behavior of I-MOS transistors in inverter applications is an advantage that has apparently not been appreciated before in the pursuit of low power dissipation digital electronics. Because of the symmetry of CMOS inverters,

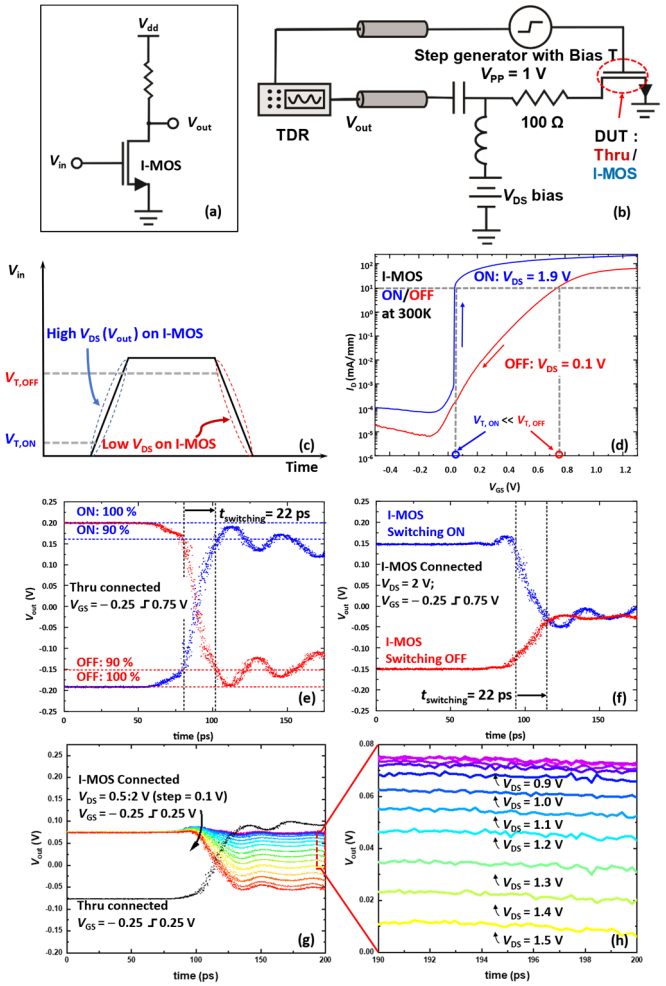

Fig. 2. Dynamic switching characteristics of GaInAs I-MOS devices for L_G = 100 nm. (a) Circuit diagram of a steep-slope resistively loaded inverter with GaInAs I-MOS (I-NMOS) pull-down transistor. (b) Test setup diagram for dynamic switching characterization. (c) Qualitative representation of high/low V_{DS} conditions during inverter switching cycle. (d) Switching trajectories of a GaInAs I-MOS pull-down transistor with dynamic threshold behavior represented for V_{DS} = 1.9 V (turn-on) and V_{DS} = 0.1 V (turn-off). (e) Measured time-domain output voltage V_{out} with a metal thru connection. (f) GaInAs I-MOS inverter fall time (blue) and rise time (red) responses. (g) Time-domain inverter turn-on response with applied V_{GS} step from −0.25 to 0.25 V and V_{DS} = 0.5–2.0 V (0.1 V steps). (h) Magnified view of the dash-box region in (g) showing clear steep-slope ON-switching of I-MOS from V_{DS} = 0.9 V.

similar considerations will apply to eventual I-MOS p-channel pull-up transistors.

Steep-slope transistors must be capable of fast time-domain switching to find use in digital electronics. We now verify that the steep-slope characteristics of GaInAs I-MOS transistors can be used in fast switching by measuring the dynamic response of a resistively loaded inverter built around an ON-wafer GaInAs I-MOS transistor with L_G = 100 nm and a gate width of 150 μm. The hybrid inverter circuit was connected using coplanar probes and an external load resistor connected via a precision coaxial cable as shown in Fig. 2(b). The measurement procedure is akin to time-domain reflectometry (TDR) and involves reflections induced by impedance mismatches, connectors, and bias tees. Both the inverter fall time (I-MOS switching on) and rise time (I-MOS switching off) were characterized.

Device biases were applied via wideband bias tees. The time-domain switching performance was recorded with the transistor inserted as the device under test (DUT) in Fig. 2(b) for various drain biases. A gate input voltage with a 7 ps rise time and a 240 ns period was applied, and the output voltage V_{out} was recorded on a high-speed sampling oscilloscope connected through a coaxial cable. Because of the cable and connector losses, the system response degrades to 22 ps when the input voltage step is fed directly to the oscilloscope via a thru connection [Fig. 2(e)]: this determines the minimum achievable transition time of the hybrid test setup. Based on the drain switching characteristic at V_{DS} = 1.9 V in Fig. 1(f), the ON-resistance R_{ON} of the I-MOS transistor is ∼10 Ω, and R_{OFF} is ∼127 kΩ considering the drain leakage current of ∼15 nA when I-MOS is switched on. With a metal thru connected in place of DUT in the hybrid inverter setup, the observed output voltage swing is 0.4 V (rather than by voltage pulse of 1 V) due to the mismatch reflections between the 100 Ω resistor and the capacitor. With GaInAs I-MOS transistor as DUT, the resistance associated with I-MOS results in an additional reflection of the propagated wave and a reduced 0.3 V output voltage swing amplitude. Because of multiple reflections in the hybrid test setup, the output voltage sweep does not reach the full amplitude in either ON-switching [blue trace in Fig. 2(f)] or OFF-switching [red trace in Fig. 2(f)] due to multiple reflections between the I-MOS and the series resistor.

With the transistor inserted in the circuit, the measured 10%–90% fall time for a positive gate voltage step in Fig. 2(f) remains unchanged with an inverter fall time of 22 ps (blue trace). The inverter rise time (red trace) is also seen to be equal to 22 ps in Fig. 2(f). The data show that GaInAs I-MOS switching delay is significantly shorter than the test setup limited transition time of 22 ps: they confirm the excellent dynamic ON/OFF switching characteristics of the present steep-slope transistors. Impact ionization clearly builds up rapidly in the direct narrow gap semiconductor as the device turns on in steep-slope operation.

Fig. 2(g) and (h) clarifies the role of steep slope in switching from OFF-to-ON for gate voltage swings of −0.25 to 0.25 V as a function of drain voltage V_{DS}: while no inverter response is observed below V_{DS} = 0.9 V, signal inversion develops rapidly for higher drain voltages. V_{DS} = 0.9 V corresponds to the onset bias for steep slope in the present I-MOS transistors (Part I, Section III, Fig. 3), confirming the role of the steep slope in fast device switching reported here.

Conservative estimates of switching capabilities can be drawn from the above observations. Circuit analysis shows that the overall response time τ_r of cascaded networks with rise (fall) times τ_{IMOS} and $\tau_{channel}$ is $\tau_r = (\tau_{IMOS}^2 + \tau_{channel}^2)^{1/2}$. A 4% transition time degradation (i.e., more than practically measured here) with the transistor in-circuit would correspond to an inverter fall time of only 6.28 ps when cascaded with 22 ps channel response time: this sets the upper bound on I-MOS switching time and corresponds to a switching bandwidth of 0.35/6.28 ps ≈ 55.7 GHz. Because digital signals use spectral content up to the clock frequency fifth

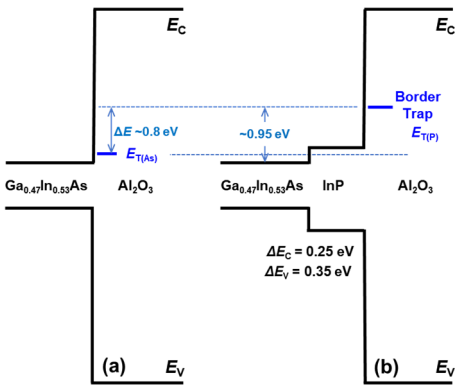

Fig. 3. Band alignments of $Ga_{0.47}In_{0.53}As$, InP, and Al_2O_3 with border trap states $E_{T(As)}$ at (a) Al_2O_3:GaInAs interface and (b) $E_{T(P)}$ at Al_2O_3:InP interface from [10]. The InP interlayer raises E_T by ~0.8 eV with respect to the Al_2O_3:GaInAs case, strongly decoupling channel carriers from trap states. Indium-rich channels further increase carrier–defect decoupling by lowering the GaInAs conduction band with respect to E_T.

harmonic to maintain a good square wave signal, the present GaInAs I-MOS transistors should conservatively operate up to an 11 GHz clock frequency.

B. GaInAs I-MOS Reliability Considerations

The above time-domain switching results provide a good indication of GaInAs I-MOS transistor stability with large gate voltage swings: the stable oscilloscope switching characteristics displayed in Fig. 2 could not be achieved in the presence of short-time parameter drift. With a signal period of 240 ns, every testing hour corresponds to 15 billion large-signal switching cycles without apparent degradation. This is to be contrasted to a strong threshold voltage drift observed in silicon-based I-MOS devices with as few as five switching cycles [4].

As discussed in Part I, silicon-based I-MOS transistors experience rapid threshold voltage shifts due to hot carrier injection (HCI) into the gate oxide because the voltages required to induce impact ionization exceed the oxide injection barriers [4]. HCI cannot take place in GaInAs I-MOS because $\Delta E_C = 2.43$ eV and $\Delta E_V = 2.99$ eV exceed qV_{DS} in device operation.

The next question to consider is the reliability of ALD Al_2O_3 gate oxide on III–V surfaces. Extensive bias temperature instability (BTI) characterization of ALD Al_2O_3 oxides deposited on $Ga_{0.47}In_{0.53}As$ channels revealed a poor device stability due to electron trapping by a band of oxide defect states ("border traps") beginning at an energy $E_T \approx 0.15$ eV above the $Ga_{0.47}In_{0.53}As$ conduction band minimum [5]. Thinner channel layers were shown to further reduce the device stability by increasing the coupling of carriers to oxide defect states [5]. The work of Franco *et al.* [5] raised concerns about the suitability of Al_2O_3 in gate stacks on III–V surfaces and motivated a quest for better high-κ dielectrics [6]. Prior work by the IMEC group [7] showed that increasing the energy separation ΔE between carriers in the channel and oxide traps to reduce the carrier–defect coupling is the most productive approach to improving reliability in a wide variety of material systems [7]. Franco *et al.* [7] introduced a universal metric ξ (i.e., the voltage–time acceleration factor exponent) characterizing the carrier–defect coupling in various dielectric–semiconductor systems. Higher ξ values indicate a weak carrier–defect coupling and predict long device lifetimes in the gate overdrive versus lifetime trade-off [7].

Al_2O_3 defects depend on the underlying III–V surface [8]. This is no great surprise considering ALD consumes part of the underlying semiconductor layer (as seen for InP in Fig. 2, Part I). Theoretical work by Robertson *et al.* [9] on Al_2O_3 defects showed that when deposited on GaAs and InAs, the pertinent oxide defects at E_T are associated with the As–As dimer antibonding state. Interpolation of the As–As defect energy level between GaAs and InAs leads to level $E_{T(As)} \sim 0.15$ eV above the $Ga_{0.47}In_{0.53}As$ conduction band minimum [Fig. 3(a)], in good agreement with the experimental results of Franco *et al.* [5]. In contrast, Al_2O_3 on InP leads to a P–P antibonding state $E_{T(P)} \sim 0.7$ eV above the InP conduction band minimum, i.e., 0.95 eV higher than the $Ga_{0.47}In_{0.53}As$ conduction band minimum [Fig. 3(b)] [10]. The InP interlayer in a Al_2O_3:InP/GaInAs stack thus raises oxide defect states by 0.95–0.15 = 0.8 eV with respect to those of Al_2O_3:GaInAs structures: this strongly decouples channel carriers from the oxide defect states. To put this in perspective, Franco *et al.* [7] established that increasing the energetic separation of channel carriers to defect states by ΔE induces a near quadratic rise in ξ: a $\Delta E = 0.5$ eV already suffices to achieve long-term device reliability in high-κ silicon and germanium pMOS/nMOS [7]. The $\Delta E = 0.8$ eV increase in carrier–defect decoupling should provide Al_2O_3:InP/GaInAs MOSFETs the BTI stability that has so far eluded Al_2O_3:GaInAs devices. The higher channel indium concentrations used here further enhance ΔE.

Higher κ dielectrics may be desirable in certain applications to increase the effective gate capacitance [11], [12]. However, higher dielectric constants are associated with narrower oxide energy gaps, and their use likely will increase carrier–defect coupling by lowering the oxide trap energy E_T with respect to carriers in the GaInAs channel. The experimental data support this idea well: HfO_2:Al_2O_3:GaInAs oxide traps do extend to lower energies than in Al_2O_3:GaInAs [11]. In principle, Al_2O_3:InP layers of sufficient thickness could be combined with higher κ dielectrics to enhance reliability by preserving the high energy of P–P trap states in the wider Al_2O_3 gap (and the beneficial self-cleaning properties of ALD-deposited Al_2O_3). The InP barrier should then be thick enough to decouple Al_2O_3 from the underlying GaInAs: Fig. 2 in Part I suggests that the InP layer should be thicker than ~1.5 nm (i.e., the thickness consumed by oxidation). The Al_2O_3 interlayer should decouple the higher κ dielectric from semiconductor layers and match the quality of a single thick Al_2O_3 layer: according to [11], this criterion is satisfied for Al_2O_3 thicknesses $\geq$0.5 nm. The insertion of Al_2O_3:InP interlayers, however, places constraints on the minimum achievable gate length by increasing the gate-to-channel separation.

Although formal reliability studies on Al_2O_3:InP/GaInAs structures have yet to be performed, prospects appear promising based on the above discussion and in light of reported improvements in $C-V$ and I_D–V_G dispersion compared with

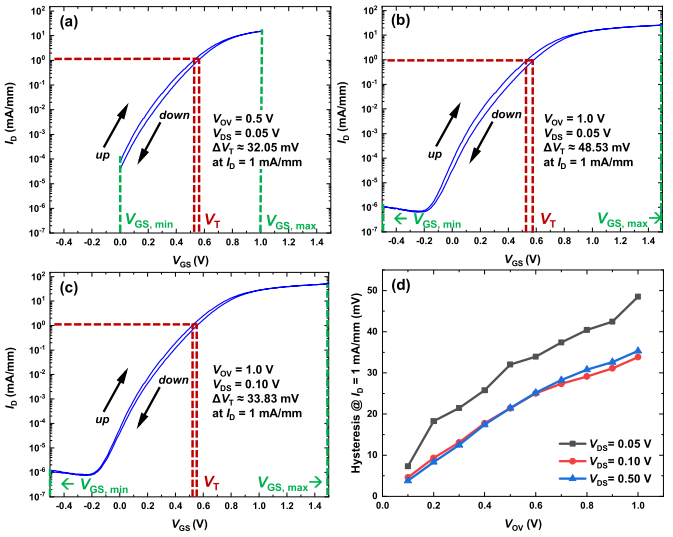

Fig. 4. (a)–(c) 300 K threshold voltage hysteresis in GaInAs I-MOS device with L_G = 100 nm gate length. (a) V_{OV} = 0.5 V, V_{DS} = 0.05 V, with 32 mV hysteresis at V_T. (b) V_{OV} = 1.0 V, V_{DS} = 0.05 V, with 49 mV hysteresis at V_T. (c) V_{OV} = 1.0 V, V_{DS} = 0.10 V, with 34 mV hysteresis at V_T. (d) Hysteresis dependence on V_{OV} for various drain biases V_{DS}.

those of Al_2O_3:GaInAs stacks [13]. In the same vein, very low interface and border trap densities ($D_{it} \approx 1.6 \times 10^{11}$ cm^{-2}·eV^{-1}; $N_{BT} \approx 6.3 \times 10^{12}$ cm^{-2}·eV^{-1}) were recently reported for Al_2O_3:InP/GaInAs FETs [12]. In comparison, $D_{it} \approx 1.7 \times 10^{12}$ cm^{-2}·eV^{-1} and $N_{BT} \approx 2.8 \times 10^{13}$ cm^{-2}·eV^{-1} have been achieved in Al_2O_3:$Ga_{0.47}In_{0.53}As$ [14] and $GdAl_2O_3$:$Ga_{0.47}In_{0.53}As$ [15] structures.

The amount of charge trapping in gate oxides can be assessed from the threshold hysteresis in I_D–V_G dispersion as a function of the applied gate overvoltage with respect to V_T at ON-switching, $V_{OV} = |V_{G,min} - V_T| = |V_{G,max} - V_T|$. Fig. 4(a) shows little I_D–V_G hysteresis for a 100 nm gate I-MOS device measured at V_{DS} = 0.05 V with V_{OV} = 0.5 V; Fig. 4(d) shows the hysteresis magnitude at I_D = 1.0 mA/mm as a function of the gate overvoltage ($\pm V_{OV}$): for a ±0.5 V gate swing, V_T hysteresis is only 32 mV, and for a ±1 V gate swing, V_T hysteresis is 48 mV. This is to be contrasted to the 70 mV hysteresis reported in 1 μm gate Al_2O_3:GaInAs FinFETs tested under similar conditions (with a ±0.75 V gate swing, V_{DS} = 0.05 V; I_D = 0.5 mA/mm) [16].

C. GaInAs I-MOS RF and Noise Performance

Fig. 5 reports the RF and noise performances of the present GaInAs I-MOS transistors. Devices with gate lengths L_G of 100 and 150 nm achieve high short-circuit current gain cutoff frequency f_T and maximum oscillation frequency f_{MAX} analog figures of merit. Specifically, L_G = 100 nm transistors show peak values of f_T/f_{MAX} = 250/310 GHz at 300 K and f_T/f_{MAX} = 313/354 GHz at 15 K, while at L_G = 150 nm the devices show f_T/f_{MAX} = 216/261 GHz at room temperature and f_T/f_{MAX} = 273/326 GHz at 15 K. To the best of our knowledge, this is the first report of high cutoff frequencies in steep-slope devices. As seen in Fig. 5(d)–(e), the transistors provide f_T > 125 GHz over a wide range of bias conditions

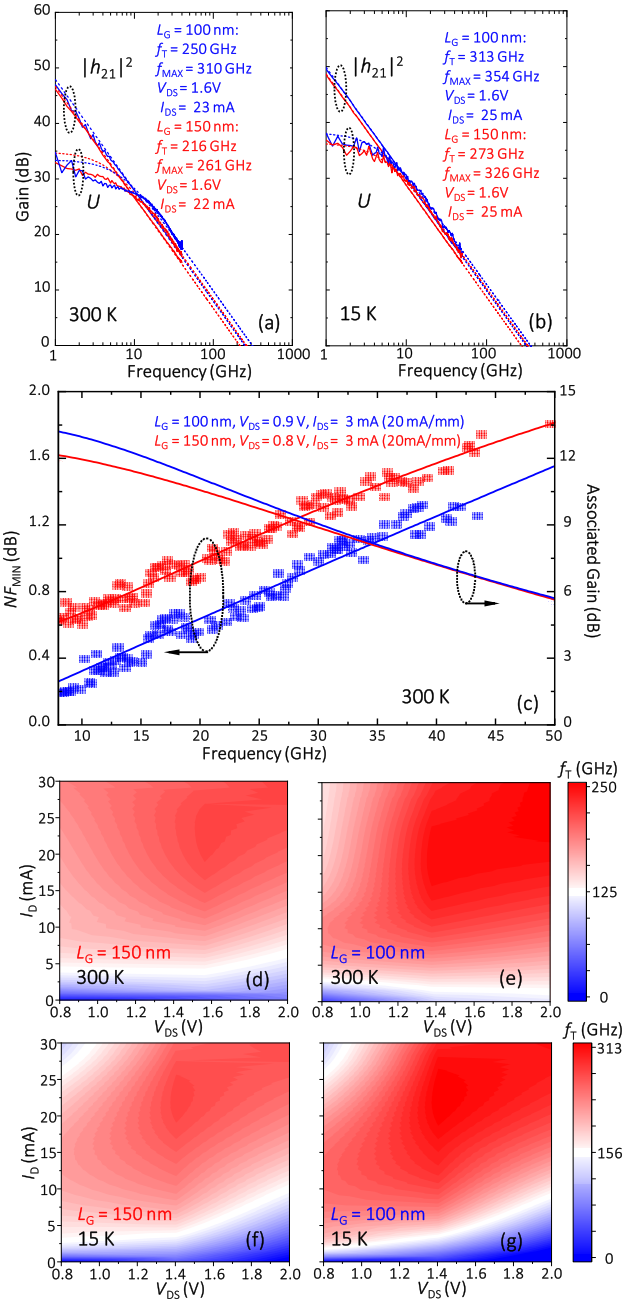

Fig. 5. RF and noise figure characterization of GaInAs I-MOS devices for 2 × 75 μm wide transistors with L_G = 100/150 nm. (a) and (b) Short-circuit current gain $|h_{21}|^2$ and unilateral power gain U with single-pole fit extrapolations at 300 and 15 K used to determine cutoff frequencies f_T of 250 and 313 GHz. (c) Frequency dependence of the minimum noise figure NF_{MIN} and associated gain. (d)–(g) Contour maps of the bias dependence of f_T at 300 and 15 K.

at room temperature. Impact ionization mostly affects the low-frequency small-signal scattering parameters and does not greatly influence the cutoff frequencies determined by extrapolation from higher frequencies [19].

The noise performance of our GaInAs I-MOS transistors was characterized by extracting the minimum noise figure NF_{MIN} and associated gain from noise parameters measured from 8 to 50 GHz. As common in transistor NF_{MIN} measurements, solutions may not be possible for all frequency points

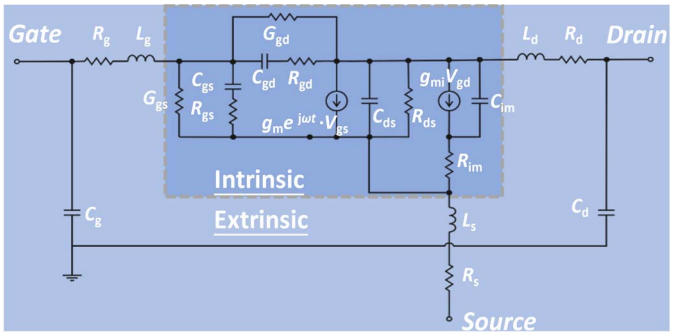

Fig. 6. Augmented small-signal equivalent circuit accounting for impact ionization [17], [18]. The model is used to simulate the noise characteristics of Fig. 5(c) in ADS.

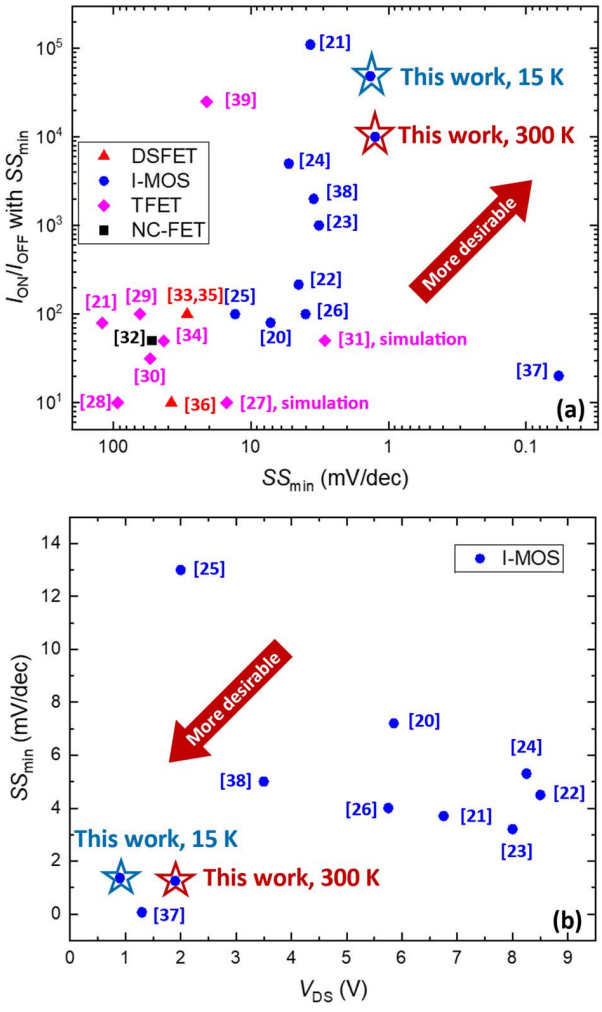

Fig. 7. Benchmarking state-of-the-art steep-slope transistor technologies at 300 K. (a) ON/OFF ratio at point of steepest slope. (b) SS_{min} versus drain bias in I-MOS devices. The arrows indicate more desirable steep-slope performance trends. N.B.: [37] and [38] use back-gate or substrate biases (3–5 V) to reduce the operating steep slope V_{DS}, whereas GaInAs I-MOS devices achieve low-voltage operation naturally.

due to practical setup limitations associated with the use of a passive source tuner. To provide a clearer characterization, NF_{MIN} was also modeled as a function of frequency using Keysight Advanced Design System (ADS) NF_{MIN} function. The small-signal equivalent circuit used for NF_{MIN} modeling is shown in Fig. 6 [17]: it accounts for impact ionization per Reuter *et al.* [18] and Ruiz *et al.* [19]. A good consistency between measured and modeled minimum noise figures and associated gains is shown in Fig. 5(c) for both gate lengths L_G. Devices with $L_G = 100$ nm show a 0.3–0.4 dB lower minimum noise figure (NF_{MIN}) at its optimum bias condition ($V_{DS} = 0.9$ V, $I_D = 20$ mA/mm) compared with transistors with $L_G = 150$ nm because of a lower C_{GS}. Rollet's stability factor k is well above unity, indicating unconditional stability at the best noise bias.

D. GaInAs I-MOS Benchmarking

This work demonstrated $L_G = 100$ nm GaInAs I-MOS transistors with a minimum steep–slope parameter $SS_{min} = 1.25$ mV/dec over 4 orders of magnitude in drain current at a bias of $V_{DS} = 1.9$ V. This performance is contrasted to other steep-slope technologies [20]–[39] in Fig. 7(a) in terms of their minimum steep-slope parameter SS_{min}, operating V_{DS}, and I_{ON}/I_{OFF} ratio *while maintaining* SS_{min} at the switching transition. GaInAs I-MOS achieves the lowest SS_{min} with a high switching current ratio. Fig. 7(b) shows that GaInAs I-MOS provides the lowest operating voltage and steepest slope among all I-MOS devices to date for devices operating without back-gate/substrate voltages.

III. Conclusion

This work establishes that narrow direct gap semiconductor III–V MOSFETs with a simple device architecture achieve excellent steep-slope transistor characteristics and fast logic switching. In terms of dynamic switching, preliminary tests reveal excellent capabilities for high clock rate operation: conservative estimates suggest that an 11 GHz clock operation with a ~1 V swing is possible with $L_G = 100$ nm. The time-domain switching measurements confirm that ionization-induced hysteresis does not affect switching: GaInAs I-MOS devices switch swiftly from OFF-to-ON, as well as from ON-to-OFF, according to the analysis in Fig. 2(f) above. When used in a logic gate inverter, I-MOS transistors turn on according to their steep slope, but turn off classically with a more positive threshold voltage, thus replicating the power-saving advantages associated with DTMOS technology [1]. This I-MOS advantage has apparently not been recognized before. We argued that switching off classically, rather than along the original steep slope, is beneficial from a dynamic power dissipation point of view. Switching performance was shown to be stable with more than 15 billion switching cycles, and analysis of reliability factors suggests that adequate reliability is possible with Al_2O_3:InP/GaInAs gate stacks.

We showed that GaInAs I-MOS transistors provide high cutoff frequencies over a broad range of bias conditions, with peak f_T and f_{MAX} cutoff frequencies in excess of 250 and 310 GHz at room temperature. In addition, the present devices show low-noise characteristics between 8 and 50 GHz which indicate potential for realization of mixed-mode analog/digital circuits in a single technological platform. To our knowledge,

this is the first demonstration of narrow gap III–V compound semiconductor-based I-MOS transistors and the first report of high cutoff frequencies coupled with high-speed switching in steep-slope transistors of any kind.

It is desirable to further reduce the necessary voltage for the onset of strong steep-slope behavior to below 1 V to compete with current CMOS technologies. Prospects for increased impact ionization levels with sub-volt operation are good, as judged from the presented 15 K data, where a fully developed steep slope is observed at $V_{DS} = 1$ V with 100 nm gates [see Fig. 3(c), Part I]. Obvious avenues to achieve sub-volt operation at 300 K involve, but are not limited to, the pursuit of shorter gate lengths L_G and narrower gate recesses (or self-aligned gates) to increase the channel electric field and higher In-content channels to achieve high levels of impact ionization at lower V_{DS}. For instance, InAs-GaInAs composite channel HEMTs already display notable impact ionization effects above $V_{DS} = 0.5$ V [40]. Preliminary work in our group confirms sub-volt steep-slope operation in an InAs channel at 300 K. In addition, steep-slope *p*-channel devices are also needed to achieve a full III–V complementary I-CMOS platform—work was initiated toward realization of *p*-channel steep-slope devices on InP in our laboratory. In our perspective, the main challenge in achieving a full I-CMOS platform likely will be the development of a suitable E-mode *p*-channel transistor in light of the much lower impact ionization rate for holes in most direct gap III–V materials. A few avenues to increase hole impact ionization in *p*-channels can be foreseen: they will be reported on in due course, should they prove effective.

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