Deep Sub-Electron Read Noise in Image Sensors Using a Multigate-Source-Follower

Wei Deng, *Student Member, IEEE*, and Eric R. Fossum, *Fellow, IEEE*

(Invited Paper)

***Abstract*—As the in-pixel source-follower (SF) gate size scales down in CMOS image sensors (CISs) and quanta image sensors (QISs), the pixel conversion gain (CG) increases at the cost of more 1/*f* noise. In this article, a multigate SF (MGSF) is proposed to simultaneously increase pixel CG and reduce 1/*f* noise. The MGSF improves the tradeoff between 1/*f* noise and CG that exists for pixels with conventional SFs, leading to reduced input-referred read noise at deep sub-electron levels.**

***Index Terms*—1/*f* noise, CMOS image sensor (CIS), multigate source-follower (MGSF), quanta image sensor (QIS).**

I. Introduction

THE input-referred read noise of CMOS image sensors (CISs) has steadily improved over the past several decades. In this sensor, photosignal charge is collected and then transferred to a floating-diffusion (FD) sense node, and the change in voltage on the sense node is buffered by a source-follower (SF) transistor. The electron input-referred read noise is determined by the SF voltage noise divided by the output conversion gain (CG), (volts/e$^-$) of the sense node, and SF. The CG is inversely proportional to the total sense node capacitance. The CMOS Quanta Image Sensor (QIS), a special type of photon-counting CIS with deep sub-electron input-referred read noise obtained by using high CG, has achieved read noise as low as 0.12-e$^-$ rms in some pixels at room temperature although the median noise across all pixels was 0.22-e$^-$ rms [1]. This enables good detection of single electrons without the use of avalanche multiplicative gain. The goal is for all pixels to achieve input-referred read noise of less than 0.15-e$^-$ rms so that accurate (low bit-error rate) single-photoelectron counting can be performed since the bit-error rate drops rapidly with read noise [2]. The specialized QIS pixel is referred to as a jot [3].

Manuscript received January 19, 2022; revised March 20, 2022; accepted April 5, 2022. Date of publication April 28, 2022; date of current version May 24, 2022. This work was supported in part by the Jet Propulsion Laboratory under Grant RSA 1658937, in part by the NASA Award Subcontract from Rochester Institute of Technology under Grant 80NSSC20K0310. The review of this article was arranged by Editor D. Van Blerkom. *(Corresponding author: Wei Deng.)*

The authors are with the Thayer School of Engineering, Dartmouth College, Hanover, NH 03755 USA (e-mail: wei.deng.th@dartmouth.edu).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2022.3166723.

Digital Object Identifier 10.1109/TED.2022.3166723

The SF transistor output noise is generally composed of thermal noise, random telegraph noise (RTN), and $1/f$ noise. The well-known models, such as the McWhorter number fluctuation model [4], Hooge mobility fluctuation model [5], or the Berkeley unified $1/f$ noise model [6], have been developed to model the $1/f$ noise, although none of them is universally accepted. Experimental data previously obtained from a QIS prototype chip with small SF show that the mobility fluctuation model matches the best in that case [7].

No matter from where the $1/f$ noise originates, it is widely observed that $1/f$ noise scales inversely with transistor gate area so that an SF with a larger gate area has a lower $1/f$ noise [8]. However, a larger area will lead to a larger SF gate parasitic capacitance, which will cause a larger total FD parasitic capacitance and thus lower the CG. Therefore, to achieve a higher CG, a smaller gate area is desired. Due to this tradeoff between $1/f$ noise and CG, the input-referred read noise can only achieve a theoretically limited minimum level when the SF is sized at its optimum [7].

The tradeoff between $1/f$ noise and CG makes it difficult to further reduce the input-referred read noise at the pixel level. To improve this tradeoff, a new SF structure was conceived [9]. In this article, a multigate SF (MGSF) is designed and fabricated with the aim to simultaneously increase the pixel CG and reduce the $1/f$ noise.

II. Pixel Design

The conventional SF in a CIS/QIS pixel is replaced with an MGSF. The MGSF consists of the SF modulation gate (MG), i.e., the FD-connected input gate, and one or two dc-biased guard gates (GG). Conceptually, the GG is introduced to increase the total effective SF gate area for $1/f$ noise reduction, while the SF modulation gate can be the minimum size allowed to achieve a higher CG.

Three MGSF configurations are explored. The GG of an MGSF can be placed closer to the source end (configuration version V1) or the drain end (V2). The MGSF can also have two GGs, while the modulation gate is placed in-between (V3). Since the modulation gate is separated from the GG, the parasitic capacitance between the SF drain/source and the GG will not contribute much to FD total capacitance. The width of MG/GG is 0.14 μm and the length of MG is 0.27 μm

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

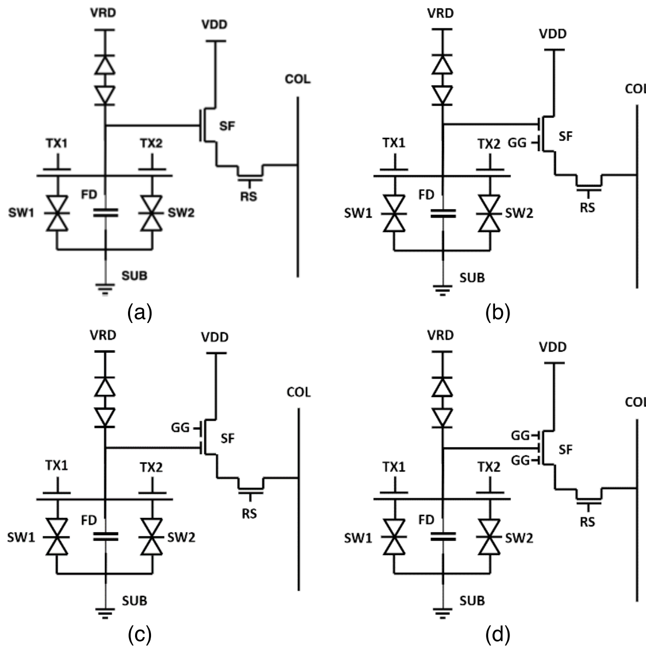


Fig. 1. Schematic: (a) V0 SF, (b) MGSF V1, (c) MGSF V2, and (d) MGSF V3.

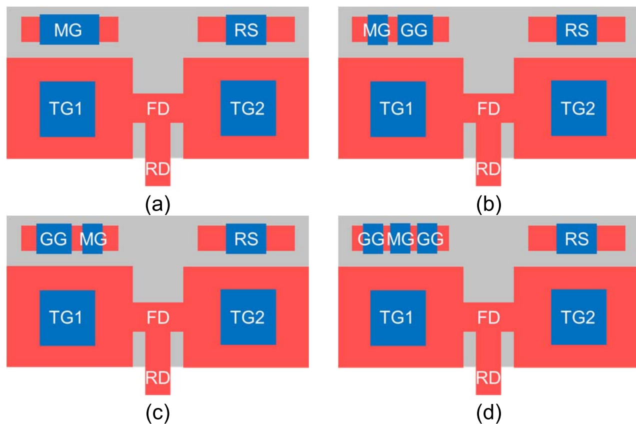


Fig. 2. Layout: (a) V0 SF, (b) MGSF V1, (c) MGSF V2, and (d) MGSF V3.

for all MGSFs. The length of GG is 0.32 μm for V1/V2 and 0.27 μm for V3 due to limited space. The as-drawn gap between gates is 0.13 μm and may be comparable within 2–3$\times$ to the mean free path of an electron in the channel [10]. A conventional MOSFET SF with the same total gate area as V1 and V2 is included for baseline reference (V0 SF configuration). Since the buried-channel SF generally has lower $1/f$ noise [7], all MGSF configurations and the V0 SF are buried-channel devices.

The schematics of V0 SF and three versions of MGSF are shown in Fig. 1(a)–(d), and the corresponding layouts are shown in Fig. 2(a)–(d). A 1 $\times$ 2 shared readout circuitry is used. As illustrated in both the schematic and layout, the pump-gate jot with a distal FD is implemented to eliminate the parasitic overlap capacitance between the transfer gate (TG) and FD [11]. The jot storage well (SW) is located underneath the TG. The punchthrough reset (PTR), which eliminates the reset gate between FD and the reset drain (RD), is implemented to further reduce the parasitic overlap capacitance between the reset gate and the FD [11].

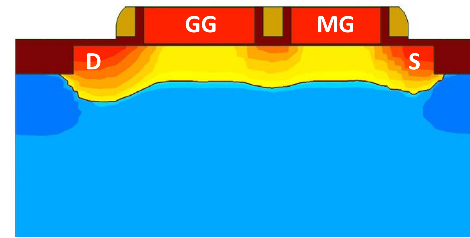


Fig. 3. Cross-sectional view of the simulated doping profile of a buried-channel MGSF V2 in TCAD. Red indicates N-doped and blue indicates P-doped.

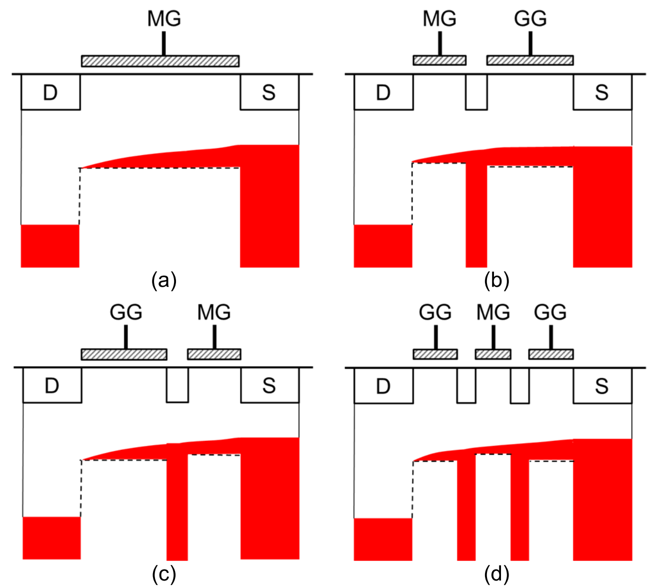


Fig. 4. Operation potential-well diagram of (a) V0 SF, (b) MGSF V1, (c) MGSF V2, and (d) MGSF V3.

The doping profile of a buried-channel MGSF V2 is simulated in TCAD and the cross-sectional view is shown in Fig. 3 as an example. An N-type layer can be seen in the channel region, which forms the buried channel. Self-aligned process is used to dope the source, drain, and the gap region. The gap between the modulation gate and the GG is filled by spacer.

The potential-well diagrams of the MGSFs in operation are shown in Fig. 4. Fig. 4(a) corresponds to V0 SF, which shows the potential-well diagram when the gate is turned on. As shown in Fig. 4(b), the modulation gate is biased at a slightly lower voltage than the GG. The gap between MG and GG forms a deeper potential well and is filled with charge carriers. The potential-well diagrams of MGSF V2 and V3 are shown in Fig. 4(c) and (d), respectively.

Correspondingly, Fig. 5 shows the electrostatic potential along the channel of the MGSFs in operation based on TCAD simulation. Fig. 5(a) shows the electrostatic potential profile of V0 SF when the modulation gate is turned on. For MGSF V1, the modulation gate is biased at a slightly lower voltage than the GG. Its electrostatic potential profile is shown in Fig. 5(b). The undulation is due to doping changes. The electrostatic potential profiles of MGSF V2 and V3 are shown in Fig. 5(c) and (d), respectively.

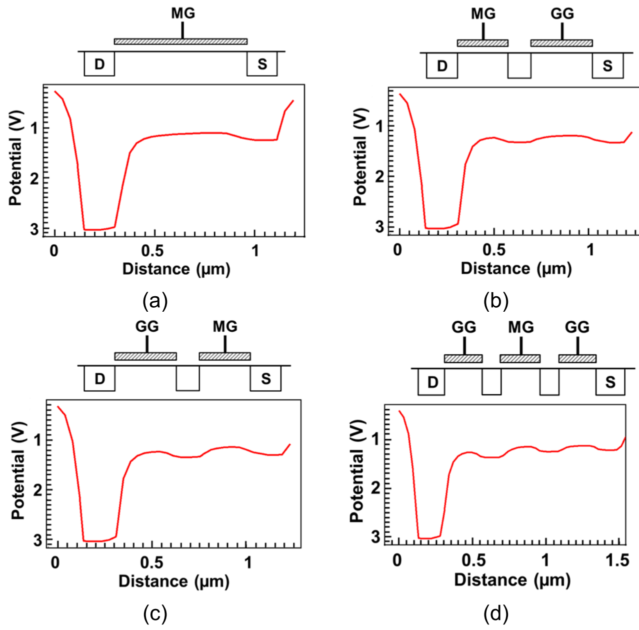


Fig. 5. Electrostatic potential along channel of (a) V0 SF, (b) MGSF V1, (c) MGSF V2, and (d) MGSF V3. Undulations are due to doping changes. MG and GG are biased at 1.4 and 1.5 V, respectively.

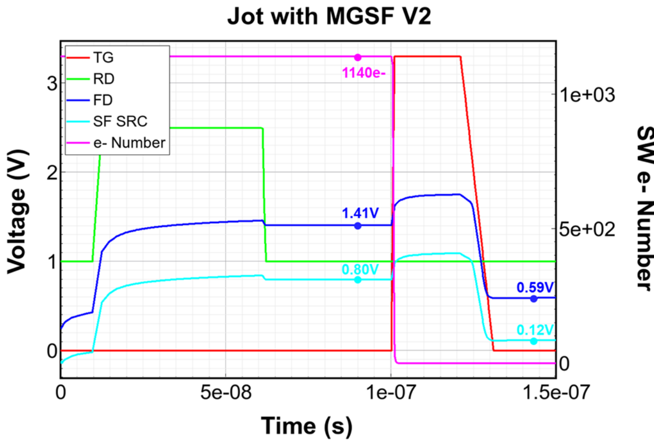


Fig. 6. Transient simulation of a jot with MGSF V2 in TCAD used to estimate CG including parasitics. (SRC: Source.)

Operation of MGSF V2 was simulated using Sentaurus TCAD, as shown in Fig. 6. When the TG is pulsed, 1140 e^- is transferred from the photodiode SW to the FD, causing an FD voltage drop of 0.82 V (i.e., from 1.41 to 0.59 V). Therefore, the input-referred CG is calculated to be 716 μV/e^-. A summary of extraction results from all types of SF devices is shown in Table I. The extracted input-referred CG of MGSFs (e.g., 700 μV/e^- for V1, 716 μV/e^- for V2, and 709 μV/e^- for V3) is about 20% higher than that of the V0 SF (e.g., 579 μV/e^-) since the size of the MGSF modulation gate is smaller compared to the V0 SF gate. According to the previous experimental verification [11], a CG that is ~20% smaller than the simulated CG is expected in fabricated devices due to other factors that are not considered in simulation. The electron input-referred read noise is estimated using the mobility fluctuation model and total MGSF gate area.

TABLE I
SUMMARY OF EXTRACTION RESULTS FROM TCAD SIMULATION AND THE MEASURED SF GAIN

SF Type	V0 SF	MGSF V1	MGSF V2	MGSF V3
Total Gate Area	0.083 μm^2	0.083 μm^2	0.083 μm^2	0.113 μm^2
C_{FD}	0.278 fF	0.229 fF	0.223 fF	0.226 fF
CG@FD	579.1 μV/e-	699.7 μV/e-	716.2 μV/e-	708.7 μV/e-
SF Gain	0.85	0.83	0.84	0.83
CG@SF Source	490.7 μV/e-	578.7 μV/e-	598.1 μV/e-	588.1 μV/e-
CG Improvement	N/A	+18%	+22%	+20%
Measured SF Gain	0.78	0.76	0.77	0.76
Estimated Read Noise (rms)	0.38e-	0.17e-	0.17e-	0.16e-

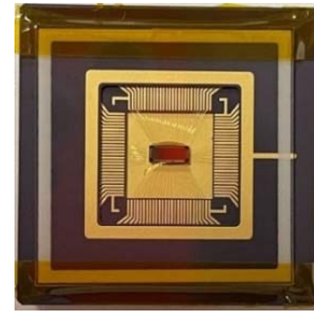


Fig. 7. QIS test chip.

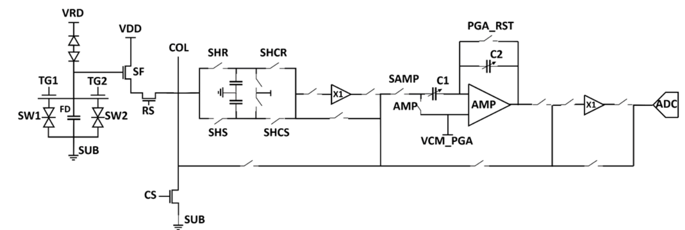


Fig. 8. Schematic of the readout signal chain with the conventional SF configuration.

The QIS test chip within a ceramic pin grid array package is shown in Fig. 7. Fig. 8 shows the schematic of the readout chain. The pixel output is sent to a correlated double sampling (CDS) circuit, followed by a unity-gain buffer. A subsequent programmable gain amplifier (PGA) is utilized to amplify the signal, with a switchable analog gain that ranges from 2 to 40 V/V. The output of the PGA is then sent to another unity-gain amplifier, which drives the output pads so the signal can be read out off-chip. The signal is then digitized by an off-chip analog-to-digital converter (ADC). The gain of the PGA is set to be 10 V/V during the $1/f$ noise testing.

Fig. 9 shows the $1/f$ noise spectrum measurement timing diagram. First, the pixel is reset by turning on both the TG and the reset gate. Then, the PGA continuously samples the pixel output signal for 0.25 s with a sampling period of 0.5 μs; 500 000 samples are collected for each pixel. The data are digitized by an off-chip ADC and a data acquisition card saves the digitized data in a PC memory. The fast Fourier transform (FFT) algorithm was used to convert the data from the time domain to the frequency domain. A noise spectrum can thus

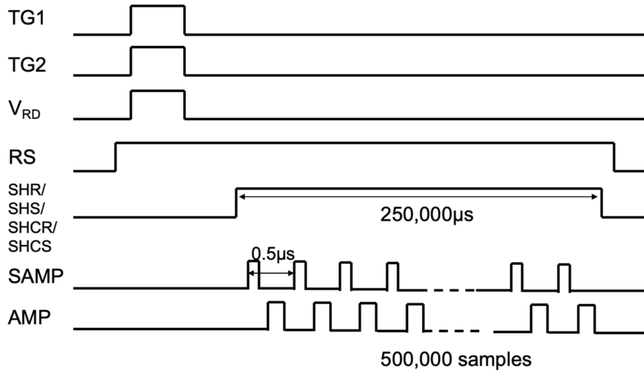


Fig. 9. Timing diagram for noise measurement.

be constructed. The input-referred noise power spectra are obtained by dividing the measured output noise spectra by the gain of the readout circuit.

III. Characterization Results

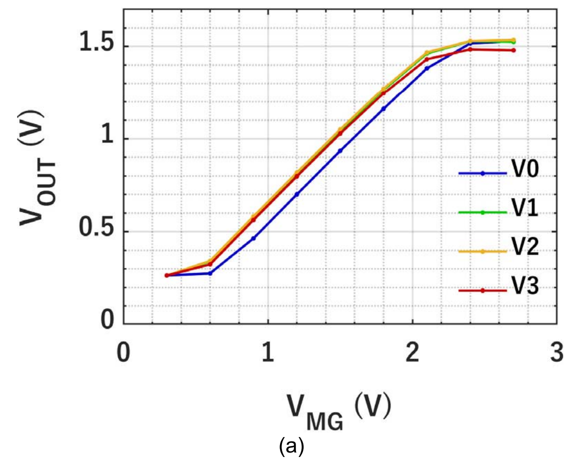
The QIS with MGSFs is implemented in a TSMC 45/65 nm stacked backside-illuminated (BSI) CIS baseline process. The pixel pitch is 2.2 μm × 1.1 μm. PTR operation was expected, but the PTR structure was found to be always "ON" with RD shorted to the SF gate, perhaps due to implant conditions. Measurement of read noise by the photon-counting histogram technique [12] was thus not possible. However, the implementation defect meant we could directly access the SF gate for voltage-domain measurements. The gain and noise for all types of MGSFs were tested. A total of 32 devices of each type were measured.

A. MGSF Gain

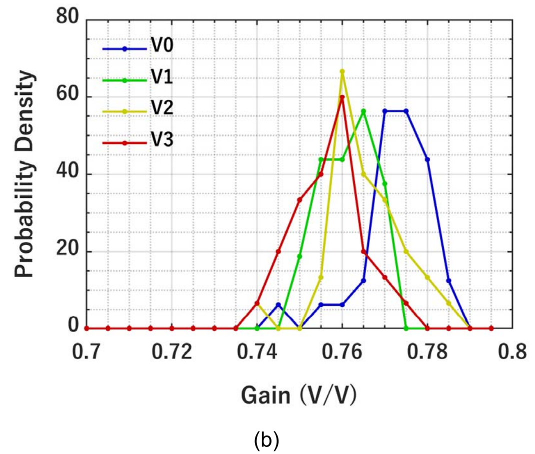
The gain measurement results for four types of SFs are shown in Fig. 10. Fig. 10(a) shows the measured average of transfer curves from 32 SFs of each type. The GG is biased at a dc voltage of 2.5 V for MGSF. The conventional MOSFET SF and the MGSF configurations show similar transfer characteristics. The SF gain can be extracted by measuring the slope of the linear region of the transfer curve. Although the gain of the V0 SF is slightly higher (e.g., 0.78), the gain of the MGSFs is similar (e.g., 0.76 for V1 and V3 and 0.77 for V2). The gain generally matches the TCAD simulation result although it is 9% smaller, possibly due to the discrepancy between the process flow used in simulation and fabrication. The output voltage of MGSFs is higher than that of the V0 SF, due to the GG biased at a slightly higher voltage lowering the threshold voltage of MGSFs. The extracted SF gain and the measured gain are summarized in Table I. Fig. 10(b) shows the histograms of the measured gain for all SFs. The MGSFs have similar gain variations as the conventional V0 SF. Normal SF operation is maintained for MGSFs with the extra GG.

B. 1/f Noise Spectrum

The input-referred noise power spectra for four types of SFs are shown in Fig. 11. Each curve is an average of the results from 32 devices. The $1/f$ trend is also shown using



(a)



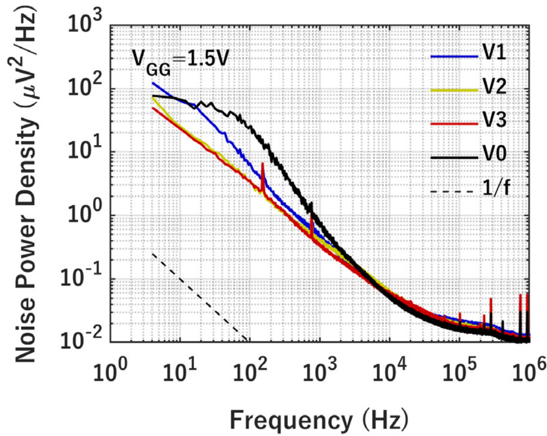
(b)

Fig. 10. Gain measurement for four types of SFs. (a) Transfer curves. (b) SF gain histograms.

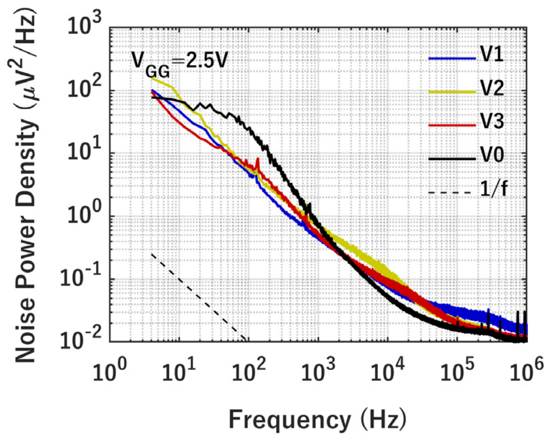
the dashed line as a reference. The bias current for all SFs is 1 μA. Fig. 11(a) shows that the MGSFs have lower noise compared to the V0 SF when the GG is biased at 1.5 V. This indicates that splitting a larger SF gate into a smaller modulation SF gate plus a GG seems to reduce the overall $1/f$ noise—a surprising result since nominally one might expect similar $1/f$ noise power for devices with the same total gate area.

The apparent change in exponent α in the $1/f^{\alpha}$ dependence is also noteworthy where α is close to unity in the V2 and V3 MGSF configurations, but $\alpha \approx 1.5$ for the "normal" V0 SF configuration, possibly indicating a change in underlying physical mechanism for the noise. (The exponent is $\alpha \approx 1.2$ for the V1 configuration.) We might further speculate that since the exponent changes mostly for V2 and V3, the mechanism may be related to the drain (pinchoff) end of the MOSFET.

The results show the same trend when the GG is biased at 2.5 V, as shown in Fig. 11(b). It is observed that the variation of the individual noise spectrum among all 32 SFs from each SF type is relatively large (about an order of magnitude), probably due to the small gate size and thus relatively large variations in geometry, doping, and scattering center distribution during fabrication. In the high-frequency region, the noise spectrum flattens out because of the white noise (e.g., thermal noise). Correlated multiple sampling (CMS) may be utilized to suppress the high-frequency noise.

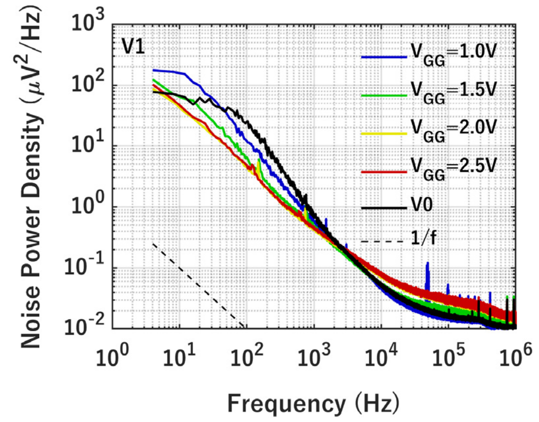


(a)

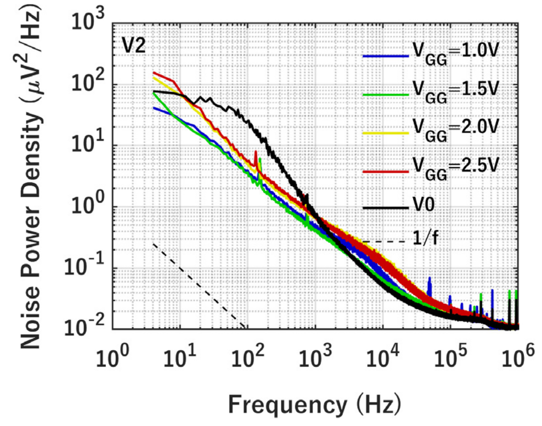


(b)

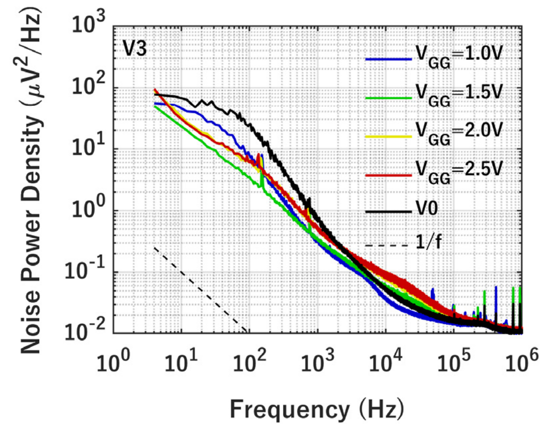
Fig. 11. Input-referred noise spectra for four types of SFs with different GG bias voltages (SF modulation gate bias voltage $V_{MG} = 1.5$ V and bias current $I_b = 1$ μA). (a) $V_{GG} = 1.5$ V and (b) $V_{GG} = 2.5$ V.



(a)



(b)



(c)

Fig. 12. Input-referred noise spectra of four types of SFs at different GG bias voltages (SF modulation gate bias voltage $V_{MG} = 1.5$ V and bias current $I_b = 1$ μA). (a) MGSF V1, (b) MGSF V2, and (c) MGSF V3.

The impact of the GG bias voltage V_{GG} is shown in Fig. 12. For buried-channel SFs, the height of the potential barrier between the channel and the Si–SiO$_2$ interface changes since the surface potential increases monotonically from the source to the drain. Due to the higher bias on the drain end, the potential barrier is higher on the drain end, leading to better shielding of the interface. Therefore, the GG may have different impact on the noise when placed on the drain end or the source end.

Fig. 12(a) shows the input-referred noise spectra of MGSF V1 at different GG bias voltages. The $1/f$ noise decreases when the GG is biased at a higher voltage. It indicates that the $1/f$ noise spectrum can be modulated by the GG bias voltage. When the GG (closer to the source end) is biased at a higher voltage, the potential barrier between the channel and the Si–SiO$_2$ interface will be lowered, and intuitively, the noise will be higher due to weaker shielding. However, the observed noise is lower at higher V_{GG}, which indicates that there might be another mechanism other than shielding. For example, higher V_{GG} may lead to more inversion charge and thus less charge number variation or less noise.

For different versions of MGSF, the influence of the GG bias is different. As shown in Fig. 12(b), for MGSF V2, the $1/f$ noise decreases when the GG is biased at a lower voltage, which is the opposite compared to MGSF V1. This is probably because the lower the GG (closer to the drain end) voltage, the potential barrier seen by the buried channel is higher, and thus, the $1/f$ noise is smaller.

The input-referred noise spectra of MGSF V3 at different GG bias voltages are shown in Fig. 12(c). Similarly, the $1/f$ noise is V_{GG} dependent. However, no clear trend is observed, probably because there are GGs on both the drain end and the source end, which combines the two opposite noise effects observed in Fig. 12(a) and (b).

To achieve the lowest noise, the optimum GG bias voltage should be used. Overall, compared to the MGSFs with different GG bias voltages V_{GG}, the V0 SF has a similar or higher $1/f$ noise.

IV. Discussion and Conclusion

These surprising results generate many questions that need to be explored through additional experiments in the future. For example, how is the $1/f$ noise affected by the intergate gap size? Is it related to the mean free path of the channel electrons? Why does it not matter too much if the GG is on the source end or drain end? How is the MGSF different from two transistors in series connected by merged source–drain such as the normal relationship between the SF and select transistor in typical CIS devices? Or do conventional CIS devices already benefit from the two transistors in series with respect to $1/f$ noise? Can the MGSF be successfully implemented in a less advanced technology node with a larger gap between gates? And, of course, one needs to demonstrate that the MGSF actually improves input-referred read noise in fully functional pixels?

An image sensor pixel with an MGSF is introduced in this article. Compared to the conventional MOSFET SF with the same total gate area, the MGSF shows similar or lower noise. The bias voltage of the MGSF GG can be used to optimize the $1/f$ noise. The MGSF has a higher CG compared to the conventional SF due to the small size of the modulation gate, as shown in the TCAD simulation. It appears that higher CG and lower $1/f$ noise can be obtained simultaneously, making MGSF potentially useful for noise reduction in CIS and QIS devices.

Acknowledgment

The authors are grateful for the comments from Dr. Jiaju Ma with Gigajot Technology, Inc., during the chip design phase. They appreciate Taiwan Semiconductor Manufacturing Corporation for the device fabrication and also grateful for the support from NASA and the collaboration with Rochester Institute of Technology under Dr. Don Figer. Recent conversations with Prof. Jifeng Liu with Dartmouth are also appreciated.

References

[1] J. Ma, D. Zhang, O. A. Elgendy, and S. Masoodian, "A 0.19 e-RMS read noise 16.7 Mpixel stacked quanta image sensor with 1.1 μm-pitch backside illuminated pixels," *IEEE Electron Device Lett.*, vol. 42, no. 6, pp. 891–894, Jun. 2021, doi: 10.1109/LED.2021.3072842.

[2] E. R. Fossum, "Modeling the performance of single-bit and multi-bit quanta image sensors," *IEEE J. Electron Device Soc.*, vol. 1, no. 9, pp. 166–174, Sep. 2013, doi: 10.1109/JEDS.2013.2284054.

[3] J. Ma and E. R. Fossum, "A pump-gate jot device with high conversion gain for a quanta image sensor," *IEEE J. Electron Devices Soc.*, vol. 3, no. 2, pp. 73–77, Mar. 2015, doi: 10.1109/JEDS.2015.2390491.

[4] A. L. McWhorter, "1/f noise and related surface effects in germanium," Ph.D. dissertation, Dept. Elect. Eng., MIT, Cambridge, MA, USA, 1955.

[5] F. N. Hooge, "1/f noise is no surface effect," *Phys. Lett A*, vol. 29, no. 3, pp. 139–140, Aug. 2002, doi: 10.1016/0375-9601(69)90076-0.

[6] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, "A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors," *IEEE Trans. Electron Devices*, vol. 37, no. 3, pp. 654–665, Mar. 1990, doi: 10.1109/16.47770.

[7] W. Deng and E. R. Fossum, "1/f noise modelling and characterization for CMOS quanta image sensors," *Sensors*, vol. 19, no. 24, p. 5459, Dec. 2019, doi: 10.3390/s19245459.

[8] M.-H. Tsai and T.-P. Ma, "The impact of device scaling on the current fluctuations in MOSFET's," *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 2061–2068, Nov. 1994, doi: 10.1109/16.333823.

[9] W. Deng and E. R. Fossum, "Multi-gate source-follower for quanta image sensors (QIS)," in *Proc. Int. Image Sensor Workshop*, Sep. 2021, pp. 20–23.

[10] B. Qiu *et al.*, "First-principles simulation of electron mean-free-path spectra and thermoelectric properties in silicon," *Europhys. Lett.*, vol. 109, no. 5, p. 57006, Mar. 2015, doi: 10.1209/0295-5075/109/57006.

[11] J. Ma, S. Masoodian, D. A. Starkey, and E. Fossum, "Photon-number-resolving megapixel image sensor at room temperature without avalanche gain," *Optica*, vol. 4, no. 12, pp. 1474–1481, Dec. 2017, doi: 10.1364/OPTICA.4.001474.

[12] D. A. Starkey and E. R. Fossum, "Determining conversion gain and read noise using a photon-counting histogram method for deep sub-electron read noise image sensors," *IEEE J. Electron Devices Soc.*, vol. 4, no. 3, pp. 129–135, May 2016, doi: 10.1109/JEDS.2016.2536719.