

HDR CMOS Image Sensors for Automotive Applications

Isao Takayanagi¹, Member, IEEE, and Rihito Kuroda², Member, IEEE

(Invited Paper)

Abstract—Because of various purposes and high dynamic range (HDR) of brightness of objects in automotive applications, HDR image capture is a primary requirement. In this article, HDR CMOS image sensor (CIS) technology and its automotive applications are discussed including application requirements, basic HDR approaches and trends of HDR CMOS image sensor technologies, advantages and disadvantages for automotive application, and future prospect of the HDR technology. LED flicker caused by time aliasing effect and motion artifacts are two major issues in conventional multiple exposure HDR (MEHDR) approach, and several HDR technologies have been introduced for automotive applications. The advancements of image sensor fabrication technology, for instance, backside illumination (BSI) process and pixel level hybrid wafer bonding, have created new trends in the HDR technology.

Index Terms—Automotive applications, CMOS image sensors (CISs), dynamic range (DR), high DR (HDR), image sensors.

I. INTRODUCTION

THE high dynamic range (HDR) image acquisition allows a lot of advantages in the automotive application. If dynamic range (DR) of a camera is not high enough, the autoexposure control must be used to adjust camera sensitivity for the system to perceive objects, which could take a few frames and degrade a response to the system. The delay of the feedback causes significant concerns in the automotive applications. Consider a case where two vehicles are moving in opposite directions each other at 110 km/h. When they are coming closer, the distance between the two cars changes by 2 m during one video frame period at 30 frames-per-second (fps). If a few frames are consumed for the exposure control, the two cars easily come closer for about 10 m until an adoptable image is obtained.

The HDR technology resolves this issue. If the image sensor has a significant capacity of detecting a high luminance range, only postprocessing is needed to optimize contrast for objects of interest without the exposure control, which simplifies the

Manuscript received January 17, 2022; revised March 25, 2022; accepted March 26, 2022. Date of publication April 25, 2022; date of current version May 24, 2022. The review of this article was arranged by Editor R. M. Guidash. (Corresponding author: Isao Takayanagi.)

Isao Takayanagi is with Brillnics Japan Inc., Tokyo 140-0013, Japan (e-mail: takayanagi.isao@brillnics.com).

Rihito Kuroda is with the New Industry Creation Hatchery Center and the Graduate School of Engineering, Tohoku University, Sendai 980-8578, Japan (e-mail: rihito.kuroda.e3@dc.tohoku.ac.jp).

Color versions of one or more figures in this article are available at <https://doi.org/10.1109/TED.2022.3164370>.

Digital Object Identifier 10.1109/TED.2022.3164370

camera operation sequence and makes information acquisition more efficient.

Image sensors have been implemented in automotive applications for various purposes, such as electrical mirrors, driving assistance/safety, the advanced driving assistant system (ADAS), and in-cabin monitors [1]–[3]. Such camera implementations are basically categorized into outside monitors and in-cabin monitors. Information from a front camera is used for many purposes, such as detection of persons, speed measurement, road line detection, traffic sign detection, measuring distance to the vehicles in the front, stop line detection, and so on. The distance measurement range of the front monitor is as wide as 0–200 m. For side cameras and rear cameras, major purposes are perception of surroundings and relatively short distance measurement to the peripheral objects up to about 10 m in the rear direction and about 5 m in the side direction. Several distance-measurement schemes, such as binocular stereo cameras or multiple camera visions, radars, and light detection and ranging (LiDAR), have been utilized. Fusion of sensing technologies has been reported to be useful to optimize reliability and stability for object perception [3]. For example, the low radio-wave reflectance of human body makes it difficult to detect persons in radar system. Pattern matching accuracy in stereo/multiple camera systems is affected by environmental conditions like bad weathers. Less texture-contrast degrades sensitivity in time-of-flight (ToF) systems. In most cases, image information from monocular cameras and/or binocular cameras is the primary input for perception of surroundings and on-road environment, vehicle tracking, obstacle detection, traffic sign recognition, and in-cabin monitoring in the sensor fusion.

Advancement of CMOS image sensor (CIS) technology and device integration, particularly backside illumination (BSI) technology and high-density wafer-to-wafer connection technology [4]–[6], allows implementation of a variety of HDR schemes within a practical pixel size. In this article, basic performance requirements to the automotive application are discussed in Section II, and the introduction of HDR technologies of CMOS image sensors and discussions for the automotive application will be given in Sections III and IV, respectively, and the conclusion will be given in Section V.

II. BASIC PERFORMANCE REQUIREMENT

In this chapter, basic image sensor requirements for the automotive applications are discussed. For safety drive assistance, automatic control, high data quality, and reliability of the acquired image are primarily required as well as HDR.

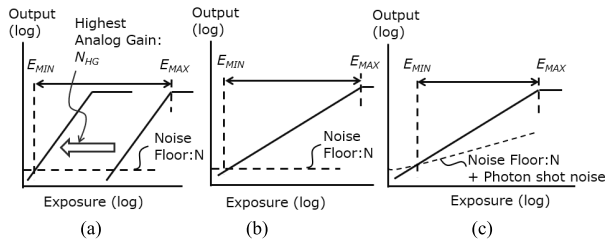


Fig. 1. Definitions of image sensor DR. Horizontal arrows denote DR between minimum exposure level and maximum exposure level, E_{MIN} and E_{MAX} , respectively. (a) Sensor DR. (b) Intrascene DR. (c) Image DR.

A. Dynamic Range

There are several definitions of image sensor DR, as shown in Fig. 1. The “sensor DR” in Fig. 1(a) is defined by the ratio between noise floor equivalent exposure under the highest gain condition E_{MIN} and the saturation exposure E_{MAX} . The “intrascene DR” of Fig. 1(b) is defined by E_{MIN} and E_{MAX} within a single image. Previously, the sensor DR was often used in image sensor specification documents, but recently, the intrascene DR definition has been recognized as a more important index, as the intrinsic DR performance of image sensors can be directly compared by using it. On the other hand, the “image DR” in Fig. 1(c) is defined as the ratio between the exposure level at which $SNR = 1$ is obtained and the saturation exposure. Significant distinction between the intrascene DR and the image DR is the influence from the photon shot noise. When we refer to the image DR, readout noise floor of much less than $1e^-$ no longer increases DR because quantum fluctuation of the incident photons (i.e., the photon shot noise) becomes dominant.

On the other hand, the intrascene DR in Fig. 1(b) increases as the readout noise reduces, even when the noise floor is lower than $1e^-$. For the frame averaging approaches and the 3-D-weighted noise reduction [7], subelectron readout noise is still beneficial. In this article, the intrascene DR in Fig. 1(b) is used for discussions unless otherwise noted. Thus, max DR is defined hereinafter by the ratio of the saturation exposure E_{MAX} and the noise equivalent exposure E_{MIN} within an image as follows:

$$DR = 20\log(E_{MAX}/E_{MIN}). \quad (1)$$

Fig. 2 shows the examples of distribution of luminance in a night scene at a local town. The surface brightness of each object was measured in cd/m^2 from the position where the photograph was taken. In the photograph, the surface luminance of the LED traffic sign (light) shows about $2000 cd/m^2$, while a person’s face at the sidewalk is about $1-10 cd/m^2$, and the ratio of luminance between those two objects is about 2000:1 or 66 dB. To extract the person’s face in the image, a certain amount of margin is required from the background noise level to the signal level of the face in the dark. Consequently, a discussion of minimum SNR is needed to determine the target performance of DR. Although there are several definitions about the minimum SNR requirement, the SNR of 4–5 is commonly considered necessary in terms of input signal quality for human vision [8], [9]. The dark random noise level of recent consumer CMOS image sensors has been reduced

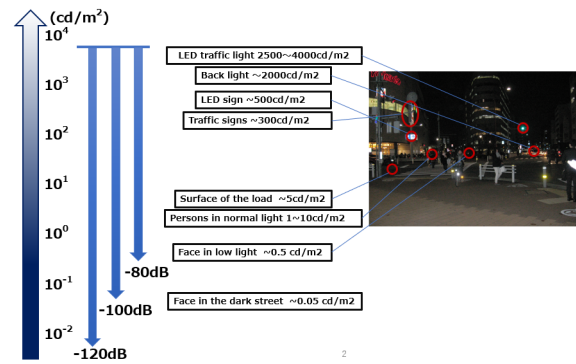


Fig. 2. Surface luminance on a street.

to about $1e^-_{rms}$ or less [10]–[12]. Here, taking into account the photon shot noise and the dark random noise with the assumption of $1e^-_{rms}$, the minimum number of signal electrons per pixel, n_{sig} , corresponding to the minimum SNR of 4–5 is $17-26e^-$, respectively. This means that for the intrascene DR of image sensors, extra DR of 24–28 dB is needed between the dark object in the scene and the dark random noise floor of the image sensor. These criteria may be relaxed with the use of machine-learning-based object recognition. For simplicity, assuming three sigma of background noise or SNR of 3 as a practical criterion for data recognition with 99.3% detection accuracy, the minimum n_{sig} and the extra DR from the dark random noise floor become $10e^-$ and 20 dB, respectively. Consequently, in this article, extra DR of 20 dB is taken into account for the determination of target DR as discussed below.

In the referenced scene in Fig. 2, the minimum DR requirement for simultaneous recognition of both the LED sign and the passerby on a sidewalk is approximately $66 dB + 20 dB = 86 dB$. Furthermore, if the target is to cover the LED traffic light and persons in the dark street simultaneously, the minimum DR requirement is estimated as $100 dB + 20 dB = 120 dB$. DR of greater than 120 dB is suggested in many references as a practical target for the automotive applications [13], [17].

B. Resolution and Pixel Size

High-resolution images allow accurate object recognition. However, resolution and pixel size have tradeoff relationship in the same optical format. Signal electrons per pixel is expressed as (2) with lens F -number F , pixel area A , unit responsivity of pixels K , luminance of an object I , and exposure time t_{EXP}

$$n_{sig} \sim \frac{\pi}{4F^2} AK I t_{EXP}. \quad (2)$$

Fig. 3 shows the pixel size dependence of signal electrons per pixel versus luminance of objects supposing lens F -number of 2.8, exposure time of $1/60 s$, and practical photodiode unit responsivity of $2.4 ke^-/(lx \cdot s \cdot \mu m^2)$ under assumptions of 5100k spectral response, IR-cut filter, and silicon absorption model [14]. While the signal electrons strongly depend on optics and exposure time, the pixel sizes of automotive sensors and surveillance sensors are much larger than those of sensors for mobile applications because of this pixel sensitivity requirement. Substituting $n_{sig} = N_n$ in (2),

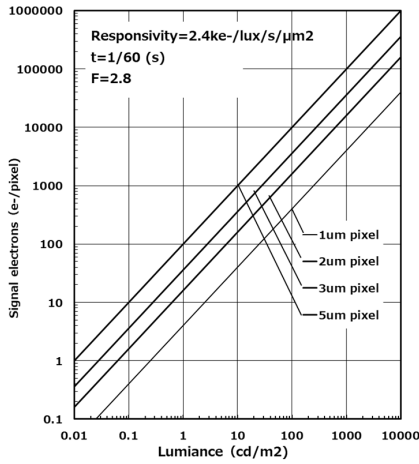


Fig. 3. Photo generated electrons per pixel versus luminance of objects and pixel size.

minimum focal plane exposure E_{MIN} is expressed by

$$E_{\text{MIN}} = \frac{N_n}{AKt_{\text{EXP}}}. \quad (3)$$

Referring to the luminance of 0.5 cd/m^2 at a person's face in a low light condition (see Fig. 2), $3\text{-}\mu\text{m}$ pixel size is required to obtain the necessary signal electrons of $16\text{--}25e^-$.

C. LED Flicker Mitigation

A light source with pulse-controlled LEDs is gradually and widely used in the automotive systems and transportation environment. Light power of these LEDs is usually controlled by pulsewidth and its frequency. Because of asynchronization between the LED lighting pulse of a traffic sign and the image sensor operation, the traffic sign may appear or disappear in video stream that is called as LED flicker [46]. In a simple single pulse model, the probability of missing light signals is roughly expressed by the following equation:

$$P = 1 - \min\left(1, \frac{t_{\text{EXP}} + t_{\text{LED}}}{t_{\text{frame}}}\right) \quad (4)$$

where t_{LED} and t_{frame} are the LED pulsewidth and the video frame period, respectively. The equation suggests that a shortened exposure time decreases the probability to detect the LED pulse; thus, the LED flicker arises more significantly. Simulation of the light detectability was reported in the literature [47], [90].

In the multiple exposure HDR (MEHDR) imaging, a short exposure time frame and a long exposure time frame are combined. Therefore, the short exposure image tends to miss the detection of the LED sign, as shown in Fig. 4. The LED flicker mitigation is mandatory for the automotive application. To mitigate the LED flicker in short exposure, pulsed integration scheme has been introduced [38], [46]. By using sensitivity gate control, integration time is divided into multiple subexposure timings and the pulse-wise subexposure durations are distributed for overall frame period, so that the probability of missing LED pulse is significantly reduced.



Fig. 4. Missing pulse-controlled LED traffic light caused by electrical shutter, which is caused by the same mechanism as the LED flicker.

D. Temperature Requirement

Guaranteeing the sensor operation in a wide temperature range, low interface cost, low communication cost, and low data processing cost are common demands for automotive applications. In AEC-Q100 automotive reliability requirement [15], four grades of temperature ranges are defined, Grade 0 (-40°C to 150°C), Grade 1 (-40°C to 125°C), Grade 2 (-40°C to 105°C), and Grade 3 (-40°C to 85°C). Although AEC-Q100 does not enforce image quality requirement, signal stability and function guarantee are least requirements within the temperature range. In most cases, data processing is performed in the linear domain. Therefore, the stability of photoconversion characteristics against temperature must be compared in the linear domain after signal linearization.

III. HDR IMAGE SENSOR TECHNOLOGY

Many HDR schemes [19]–[22], [51] have been proposed for CMOS image sensors. In this section, the classification of HDR CMOS image sensor technology is discussed for automotive applications based on technological features, and then, the trend of the HDR technology is described. Fig. 5 shows the summary of HDR enhancement schemes. The HDR approaches are basically categorized into three groups: the nonlinear response HDR approach, the linear response HDR approach, and the hybridized HDR approach of linear and nonlinear responses.

A. Nonlinear Response HDR

To reproduce an HDR image within a limited signal range and a resolution of a display in bits, an approach, where the output signal of an image sensor is compressed, has been proposed and developed. In this approach, the sensor response is extended to cover wide range of object luminance levels. This approach inherently results in nonlinear sensor response. Logarithmic compression of photo current into voltage [23], [24], knee photoresponse compression with charge skimming [13], [17], [25]–[28], [36], and time-to-saturation [29], [30] are well known schemes as conventional nonlinear response HDR schemes.

Although HDR can be obtained with a simple pixel circuit configuration, there are issues with the logarithmic response pixel that include large fixed-pattern-noise (FPN) due to variation of IV characteristics of MOS transistors,

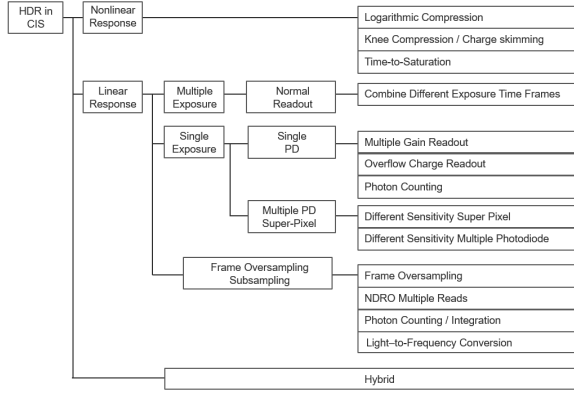


Fig. 5. Classification of HDR CMOS image sensor schemes.

long response time at low-light levels, complicated calibration requirements for FPN suppression, linearization error in image processing, and so on. To improve low light performance, linear-and-logarithmic photoresponse approaches [31], [32] and further calibration method [33]–[35] have been reported to be useful. Because complete FPN correction and accurate linearization are still technical challenges, the nonlinear compression schemes have not been widely adopted for consumer/automotive applications.

On the other hand, the simplification of the pixel structure is suitable for pixel size reduction; 2.7- μm knee performance global shutter pixel with automatic knee point adjustment [48] and 120-dB 2.2- μm linear-and-logarithmic pixel [49] have been reported for instance.

Recent pixel-level stacking technology [6], [37] and increase of integration capacity allow implementation of in-pixel comparator and in-pixel counter within practical pixel size, which suggests feasibility of the digital approach for nonlinear compression [50]. Advantages of photoresponse compression in digital domain are not only high stability toward various environment but also flexible programmability [95].

B. Linear Response HDR With Multiple Exposure

Since a charge-coupled device (CCD) HDR camera using different exposure times was reported in 1998 [18], the MEHDR scheme [39]–[41] has been a popular scheme. Its principle is to combine multiple images with different integration times, as shown in Fig. 6, where a case of two images from two different integration times being captured in a rolling shutter operation is shown. Assuming linear conversion characteristics, the resulting DR, DR_{MEHDR} in decibel, is expressed as follows:

$$\text{DR}_{\text{MEHDR}} = 20\log(n_{\text{sat}}/N_n) + 20\log(t_0/t_1) \quad (5)$$

where n_{sat} is the saturation level, N_n is the noise floor, and t_0 and t_1 are the long integration time and the short integration time, respectively.

Referring to row $\#n$ in Fig. 6, pixels on row $\#n$ are reset by the Shutter Scan 1 and the charge integration starts. After the integration time t_0 , signals from pixels on row $\#n$ are fed to readout signal chain by Read Scan 1. At the same time, signals on row $\#(n - \Delta)$, which was reset by Shutter Scan 2 after Read Scan 1, are fed to the readout signal chain. Note

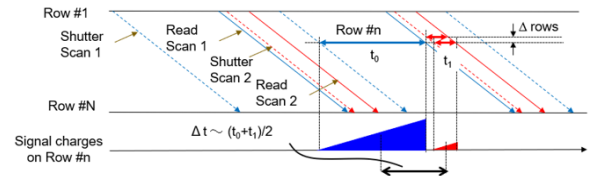


Fig. 6. Typical timing diagram of two exposures HDR in rolling shutter operation.

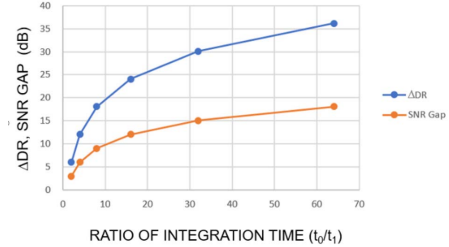


Fig. 7. DR and SNR gap at conjunction point between t_0 image and t_1 image.

that the integration time for row $\#(n - \Delta)$ is t_1 . Delay line memory for Δ rows is needed to combine the two signals, of which integration times are t_0 and t_1 , for HDR image synthesis [45]. Time difference in two images, one with a long integration time t_0 and the other with a short integration time t_1 , is approximately $\Delta t \sim (t_0 + t_1)/2$.

There are several derivative MEHDR scanning schemes, such as a line-interleave scheme, where every two lines (rows) have different integration times [41], and a scheme where more complicated assignment of different integration times to pixels is implemented [43].

The advantage of the MEHDR scheme is that a high ratio between the long integration time and short integration time can be set, thereby yielding a large number of HDR in decibel. In addition, sensitivity ratio between the signals is exactly defined by the ratio of exposure time, giving accuracy in data processing for linearization. However, as the DR enhancement increases, a gap in SNR between the two signals increases. Considering the dominant temporal noise source is the photon shot noise, the SNR gap, $\Delta\text{SNR}_{\text{MEHDR}}$, is given by

$$\Delta\text{SNR}_{\text{MEHDR}} = 20\log\left(\sqrt{t_0/t_1}\right). \quad (6)$$

Since SNR limited by photon shot noise is proportional to $\sqrt{n_{\text{sig}}}$, Fig. 7 shows the relationship between extra DR by MEHDR $\Delta\text{DR}_{\text{MEHDR}}$, $\Delta\text{SNR}_{\text{MEHDR}}$, and the ratio of integration time, t_0/t_1 . For example, DR is extended by 30 dB from (5), but SNR at the signal transition point is degraded by 15 dB from (6) when the ratio of integration time t_0/t_1 is set at 32. Therefore, more than two different integration times may be needed to avoid a significant SNR drop at the signal transition point [40], [44]–[46], assuming 120-dB DR, and 70-dB DR in each subframe. The resulting frame period increases as the number of combined integration times, assuming that the readout speed is constant. In this sense, a high-speed signal processing technology is a key technology to realize a practical image sensor product with MEHDR capability. In addition, its disadvantages are a possible motion artifact and enhanced LED flicker in short exposure frame, simply because each integration timing is not identical, as shown in Fig. 6.

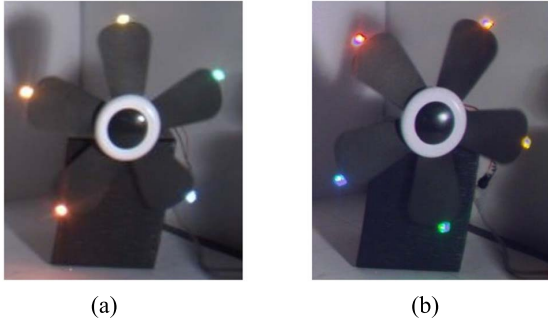


Fig. 8. Comparison between (a) SEHDR and (b) MEHDR.

In order to reduce integration time ratio between the longest exposure and shortest exposure and to mitigate LED flicker, the fusion of MEHDR and single-exposure HDR (SEHDR) approach is currently popular, such that combination with multiple pixel gain [52], [53], dual photodiode [54], [55], lateral overflow integration capacitor (LOFIC) [56], and pulsed integration [46], [47], [56]. By these methods, over 120-dB DR can be achieved.

C. Linear Response HDR With Single Exposure

To address the motion artifact with the MEHDR scheme, an SEHDR scheme has been proposed. The idea is to capture the same image in different gains but identical integration time. Comparing to MEHDR, SEHDR has a fundamental advantage for mitigation of the motion artifacts. Fig. 8 shows the typical comparison of HDR images between MEHDR and SEHDR for a moving object. In Fig. 8(b), LED light is blurred after synthesizing the multiexposure images.

A simple approach to realize the multiple gains in the CMOS image sensor is to have multiple signal paths in the column-parallel gain stage [57], [58]. When signal level of a pixel is larger than a threshold level, low gain signal is used, and high gain signal is used for low pixel signal. The signal voltages [the reset level and the signal level for correlated double sampling (CDS)] are fed to the multiple gain paths, digitized (A/D converted) and synthesized to generate an HDR image, as shown in Fig. 9. With this approach, noise floor of the image is determined by noise in high gain condition N_{n_HG} and max signal is determined by saturation in low gain condition n_{sat_LG} ; thus, DR in SEHDR, DR_{SEHDR} , is expressed as

$$DR_{SEHDR} = 20\log(n_{sat_LG}/N_{n_HG}). \quad (7)$$

To realize large saturation level and a low readout noise of pixel, multiple gain pixel [45], [59], [60] or LOFIC [61], [62], [83], [86]–[89], [98], [99] scheme has been introduced. The multiple pixel gain scheme is suitable for the SEHDR and introduced for consumer sensors with on-chip linearization functions, a 90-dB SEHDR sensor with triple gain pixel [56].

SNR gap at the signal transition point in SEHDR, ΔSNR_{SEHDR} , is expressed as (8) with signal electrons at the signal transition point n_c , signal electron referred to noise floor of the high gain mode and low gain mode, N_{n_HG} and N_{n_LG} , respectively

$$\Delta SNR_{SEHDR} = 20\log\sqrt{\frac{n_c + N_{n_HG}^2}{n_c + N_{n_LG}^2}}. \quad (8)$$

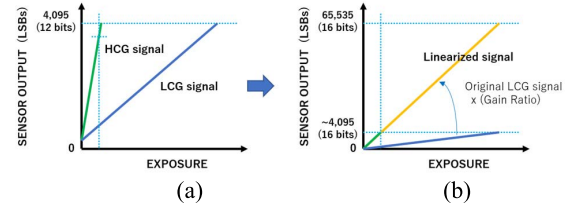


Fig. 9. Simplified linearization scheme in multiple gain SEHDR. (a) Raw photo conversion characteristics. (b) Linearized HDR photo conversion characteristics.

In case when shot noise is dominant in the high gain signal at the signal transition point, ΔSNR_{SEHDR} is simply determined by the following equation:

$$\Delta SNR_{SEHDR} \sim 20\log\sqrt{1/(1 + N_{n_LG}^2/n_c)} \quad (9)$$

which means an increase of n_c at the signal transition point (requires higher full well capacity (FWC) for the high gain signal) and/or a reduction of noise in the low gain readout suppress the SNR gap. Here, for the LOFIC approach, leakage current and its shot noise at the floating diffusion (FD) or other diffusion area along with the overflow path lead to an increase of dark signal nonuniformity and dark temporal noise for the low gain signals utilizing the overflow integration. These are very important at an elevated temperature for automotive applications. Thus, the suppression of the FD leakage current is critically important for this architecture [90], [100]. Introducing multiple gains more than two gains is also beneficial approach to reduce the SNR gap [62].

D. Frame Oversampling and Photon Counting

Frame oversampling, namely, high frame rate readout in much faster than necessary video rate and summing frames, enhances DR [63], [85]. Assume a constant light in time, readout noise equivalent electrons, N_n , and saturation signal n_{sat} in the subframe. If subframe rate is M times faster than a required video frame rate, DR of the frame subsampling DR_{FSS} can be expressed as

$$DR_{FSS} = 20\log(\sqrt{M}n_{sat}/N_n). \quad (10)$$

One of the fundamental solutions to enhance the intrascene DR is to detect photon in very high frame rate with very low noise floor. In this way, DR can be increased by accumulating number of signal photons. This approach requires low noise floor with single-photon avalanche diode (SPAD) imaging [64], [66] or very low noise readout technology [10], [11], [65], which is also represented by quantum jot concept [12], [16], [67]–[70], [80]. Giving high conversion gain, readout noise floor of less than $0.3e_{rms}^-$ [12] has been achieved and photon number can be detected. SNR by photon counting HDR, SNR_{PC} , is approximately expressed by the following equation:

$$SNR_{PC} = 20\log\left(n_{SIG}/\sqrt{n_{SIG} + M \times N_n^2}\right) \quad (11)$$

where M is the number of accumulated subframes, N_n is the noise floor equivalent signal electrons, and n_{SIG} is the total signal electrons of M subframes. Equation (11) suggests that detection noise must be lower than the shot noise to achieve similar SNR level of charge integration-type image sensors.

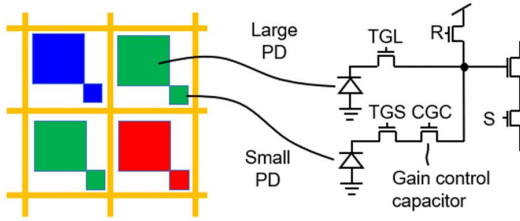


Fig. 10. Typical configuration of split photodiode pixel consists of high-sensitivity photodiode and low-sensitivity photodiode with lower conversion gain.

DR in the photon counting approach is limited by practical maximum number of counter. By combining time-to-counter saturation, 124-dB DR with very high sensitivity is reported [71], [72].

E. Linear Response HDR With Multiple Photodiodes

Output from the large photodiode covers lower light signal and output from the small photodiodes covers higher light signal. Both signals are combined into HDR output as the same manner, as shown in Fig. 10. Many CMOS image sensors with the split diode concept were demonstrated [54], [55], [73]–[76]. Fig. 10 shows an example [73], where a large photodiode covers low-light portion of the scene with high-pixel conversion gain. The small photodiode covers high-light portions of the scene with lower pixel conversion gain and high FWC. From layout constraints in practical pixel size as about $3\ \mu\text{m}$, available ratio of photodiode sensitivity is around ten times or so, thus about 20 dB. DR of this system is determined by noise floor in high-sensitivity photodiode readout, photodiode sensitivity ratio, and FWC in the low-sensitivity photodiode readout. By combining LOFIC operation [61] for low gain readout part and dual gain readout operation [77] for high gain part, 132-dB SEHDR DR is obtained [55].

SNR gap at signal transition point is expressed as (12) introducing readout noise floor in low-sensitivity pixel readout N_{n_LS} and in high-sensitivity photodiode readout N_{n_HS} , respectively. Because of reduced sensitivity with ratio k , equivalent shot noise component is enhanced by k when linearization is done

$$\Delta \text{SNR}_{\text{MPD}} = 20 \log \left(k \sqrt{\frac{n_c/k + N_{n_LS}^2}{n_c + N_{n_HS}^2}} \right). \quad (12)$$

Two fundamental issues of the split photodiode HDR are: 1) less lens flexibility and 2) special mismatch between the high gain photodiode and the low gain photodiode. Since the angular responses of the large and small photodiodes cannot be identical, as is expected from Fig. 10, this type of HDR pixel is not suited for exchangeable-lens system such as digital still cameras. Also, the local discrepancy between the photodiode causes pattern matching error in subpixel resolution for stereo 3-D imaging. The “nested photodiodes” pixel configuration [74] has been proposed to mitigate this issue.

IV. DISCUSSION

Technological features and developments trend of various HDR technologies have been summarized in Section III. Here, in this section, desirable technology directions suitable for

automobile applications are discussed, and future technology trend enabled by hybridized HDR technology with pixel-level stacking is explored.

A. Directions

Considering variety of image applications in the automotive system, prioritization of image sensor performance and appropriate HDR solutions should be discussed. For the outside monitor, high sensitivity, resolution, data stability, and credibility of the image information regardless any sorts of light source are primary required besides HDR. HDR scheme that does not affect spatial accuracy for subpixel superresolution [96], [97] and having capability of seamless exposure to mitigate LED flicker are fundamentally suitable solution for outside monitor. In the classification in Fig. 5, single-exposure and single-photodiode HDR, frame oversampling, and frame subsampling schemes correspond to this category.

To achieve 120-dB DR with a single-exposure and $\sim 1e$ readout noise and 1-V voltage swing at FD, pixel capacitance of 160 fF is required to accumulate $10^6 e^-$, which corresponds to $30\ \text{fF}/\mu\text{m}^2$ for $3\text{-}\mu\text{m}$ pixel if capacitance coverage factor is 60% of the pixel area. Unit capacitance of conventional pixel capacitor composed from MOS capacitors or metal-oxide-metal (MOM)/MIM capacitors is around few $\sim 10\ \text{fF}/\mu\text{m}^2$. Implementation of high-density 3-D MIM capacitors [91] or Si trench capacitors [89] can breakthrough this issue [101]. Pixel-level 3-D stacking has further potential to provide higher integrity for charge accumulation capacitor of LOFIC.

Frame oversampling by photon counting and seamless accumulation for whole frame period is another ultimate solution. To achieve 120 dB by this scheme, photon counting rate of at least 10^6 times faster than that of the superframe rate is required. To mitigate the speed requirement, in pixel function such as multiphoton detection in the subframe or adaptive comparator threshold control, pixel level data compression must be implemented. High logic integrity of application-specified integrated circuit (ASIC) wafers is suitable for these purpose with the pixel-level 3-D stacking technology.

HDR fusion combining the SEHDR and nonlinear compression is another interesting approach. Pixel-level analog-to-digital conversion (ADC) and digital domain compression in high light signal provide drastic stability against temperature degradation or data storage noise in HDR global shutter pixel, which is to integrate these features in pixel within appropriate pixel size, pixel-level stacking is the mandatory technology.

B. Hybridized HDR With Pixel-Level Stacking Technology

The advancement of pixel-level stacking technology with high-density hybrid bonding [5], [6] enables drastic increment of integrity of transistors and/or devices, such as pixel-level ADC, counter or memory, and data compression logic without impact on optical aperture. Fig. 11 summarizes the HDR technology perspective with pixel-level stacking technology. The upper part of the figure illustrates an example of three-layer stack chip [92], with high-density hybrid bonding with pixel-level connections for the first substrate with photodiode (PD) and second substrate and bonding with through silicon via

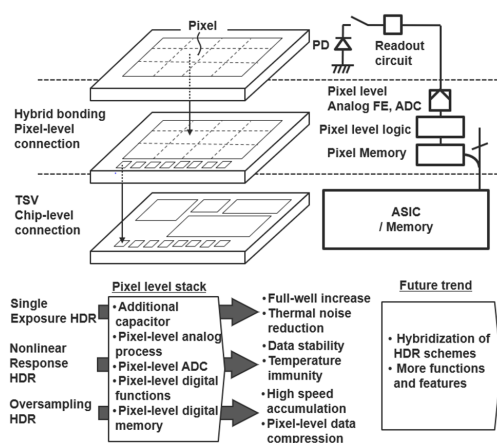


Fig. 11. Perspective of HDR technologies using pixel-level stacking technology.

(TSV) connections on chip peripheral region for the second and third substrates, respectively. The stacking feature is not limited to this example. As TSV density can be greatly improved [93], multsubstrate stacking with pixel-level connections is possible in the future. As summarized in the bottom of Fig. 11, the pixel-level stacking technology enables further performance improvements of the conventional HDR approaches by adding more advanced device components to the pixel such as, data compression in digital domain in nonlinear photoresponse compression HDR, large number of counters or memories for photon counting HDR, large capacitors to increase LOFIC capacitor, and so on. In addition, it will realize hybridization different HDR technologies with more flexible design.

The stack technology with pixel-level bonding brings benefits to photon counting HDR approach, too. By separating SPAD layer and counting layer, the integrity of the storage is drastically increased as well as a high-diode fill-factor is obtained. With combination of SPAD photon counting and time-to-saturation approach, it has been recently reported that 124-dB DR is achieved with $12.24\text{-}\mu\text{m}$ pixel [72].

In addition, image sensors with pixel-level ADC and digital data storage, namely, digital pixel sensors (DPSs), allow smart data quantization for HDR [80]–[82]; $4.6\text{-}\mu\text{m}$, 10-bit DPS with 127-dB single-exposure DR and digital compression [83], and $4.0\text{-}\mu\text{m}$, 118-dB, 9-bit digital pixel [84] have been reported. In the $4.6\text{-}\mu\text{m}$ DPS [83], 127-dB HDR is realized by combination of LOFIC operation and time-to-saturation quantization in a single readout. A high gain linear quantization for low light signals, low gain linear quantization for middle light signals, and time-to-saturation quantization for very high light signals are performed.

A fundamental advantage of the pixel-level photon detection and accumulation without data scanning will be available with pixel-level stacking technology, which is equivalent to high-speed readout and frame integration for DR enhancement. For the multiple layer stack with very fine interconnect pitch and alignment, 3-D sequential integration has been proposed to be useful and explored for CIS, and recently, actual imaging result has been presented [42], [102], [103]. Furthermore, with the

cointegration of advanced memory devices, more sophisticated in-sensor computing is foreseen [94].

Consequently, pixel-level stacking technology is and will be making dramatical evolution in CIS HDR technology for automotive applications.

V. CONCLUSION

Strong demand toward a safer and more automated driving in automotive applications accelerates the research and development of HDR CIS technologies. In this article, various HDR schemes were overviewed along with the application requirements. The single-exposure/single-PD scheme has fundamentally suitable for the imaging system with various optical conditions without image information loss. With the great efforts of the CIS industry for the research and mass production, stacking technology with high-density electrical connections in CIS is now leading the entire semiconductor industry, making it possible to be adopted by the automotive applications. The performance and functionality of the HDR technology are expected to be further improved by using the pixel-level stacking technology. Moreover, it will enable hybridization of HDR schemes to both improve performances and add more functions, such as in pixel data compression, signal processing and recognition for real-time sensing, and control with high efficiency.

ACKNOWLEDGMENT

The authors would like to thank Prof. Nobuyuki Okazi of Nagoya University and Toru Saito of Subaru Corporation for their valuable advice on issues and requirements of imaging systems in automotive system and traffic control system. They would also like to thank Dr. Junichi Nakamura for his kind discussion and feedback on the basis of CMOS image sensor technologies.

REFERENCES

- [1] S. Dabral, S. Kamath, V. Appia, M. Mody, B. Zhang, and U. Batur, "Trends in camera based automotive driver assistance systems (ADAS)," in *Proc. IEEE 57th Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Aug. 2014, pp. 1110–1115.
- [2] H. Kim, J. Lee, S.-M. Hwang, and S. Cha, "Embedded camera module for automotive camera system," in *Proc. Pan Pacific Microelectron. Symp. (Pan Pacific)*, Jan. 2016, pp. 1–7.
- [3] D. J. Yeong, G. Velasco-Hernandez, J. Barry, and J. Walsh, "Sensor and sensor fusion technology in autonomous vehicles: A review," *Sensors*, vol. 21, no. 6, p. 2140, Mar. 2021.
- [4] T. Kondo *et al.*, "A 3D stacked CMOS image sensor with 16 Mpixel global-shutter mode and 2Mpixel 10000 fps mode using 4 million interconnections," in *Proc. Symp. VLSI Circuits (VLSI Circuits)*, Jun. 2015, pp. C90–C91.
- [5] Y. Kagawa *et al.*, "An advanced CuCu hybrid bonding for novel stacked CMOS image sensor," in *Proc. IEEE 2nd Electron Devices Technol. Manuf. Conf. (EDTM)*, Mar. 2018, pp. 65–67.
- [6] J. Jourdon *et al.*, "Hybrid bonding for 3D stacked image sensors: Impact of pitch shrinkage on interconnect robustness," in *IEDM Tech. Dig.*, Dec. 2018, p. 7.
- [7] K. Hwang and T. Hiro Nishimura, "A study on the 3D-weighted filtering for the $1/f$ noise reduction on CMOS image sensor," in *Proc. IEEE Int. Symp. Ind. Electron.*, Jul. 2009, pp. 575–580.
- [8] J. C. Dainty *et al.*, *Image Science*. London, U.K.: Academic, 1974, ch. 5.
- [9] A. Rose, *Vision: Human and Electronic*. New York, NY, USA: Plenum Press, 1973, ch. 1.
- [10] S. Wakashima *et al.*, "A linear response single exposure CMOS image sensor with $0.5e^-$ readout noise and $76ke^-$ full well capacity," in *Proc. Symp. VLSI Circuits (VLSI Circuits)*, Jun. 2015, pp. 88–89.

- [11] M. W. Seo *et al.*, "A 0.27 e-rms read noise 220- μ V/e-conversion gain reset-gate-less CMOS image sensor with 0.11- μ m CIS process," *IEEE Electron Device Lett.*, vol. 36, no. 12, pp. 1344–1347, Dec. 2015.
- [12] J. Ma and E. R. Fossum, "Quanta image sensor jot with sub 0.3e- r.m.s. read noise and photon counting capability," *IEEE Electron Device Lett.*, vol. 36, no. 9, pp. 926–928, Sep. 2015.
- [13] M. Schanz, C. Nitta, A. Bussmann, B. J. Hosticka, and R. K. Wertheimer, "A high-dynamic-range CMOS image sensor for automotive applications," *IEEE J. Solid-State Circuits*, vol. 35, no. 7, pp. 932–938, Jul. 2000.
- [14] J. Nakamura, *Image Sensors and Signal Processing for Digital Still Cameras*. Boca Raton, FL, USA: CRC Press, 2005.
- [15] Automotive Electronics Council, "Failure mechanism based stress test qualification for integrated circuits," AEC Q100 REV-H, 2014.
- [16] E. Fossum, J. Ma, S. Masoodian, L. Anzagira, and R. Zizza, "The quanta image sensor: Every photon counts," *Sensors*, vol. 16, no. 8, p. 1260, Aug. 2016.
- [17] D. Hertel, "Extended use of incremental signal-to-noise ratio as reliability criterion for multiple-slope wide-dynamic-range image capture," *J. Electron. Imag.*, vol. 19, no. 1, 2010, Art. no. 011007.
- [18] K. Yamada, T. Nakano, and S. Yamamoto, "A vision sensor having an expanded dynamic range for autonomous vehicles," *IEEE Trans. Veh. Technol.*, vol. 47, no. 1, pp. 332–341, Feb. 1998.
- [19] O. Yadid-Pecht, "Wide-dynamic-range sensors," *Opt. Eng.*, vol. 38, no. 10, pp. 1650–1660, 1999.
- [20] A. Spivak *et al.*, "Wide-dynamic-range CMOS image sensors—Comparative performance analysis," *IEEE Trans. Electron Devices*, vol. 56, no. 11, pp. 2446–2461, Nov. 2009.
- [21] T.-C. Kim, "Wide dynamic range technologies: For mobile imaging sensor systems," *IEEE Consum. Electron. Mag.*, vol. 4, no. 2, pp. 30–35, Apr. 2014.
- [22] R. Kuroda, "Review on IISW 2019; outline and topics (1); small pixels and optics, noise and high dynamic range," *J. Inst. Image Inf. Telev. Eng.*, vol. 74, no. 2, pp. 263–268, 2020.
- [23] S. G. Chamberlain *et al.*, "Silicon imaging arrays with new photoelements, wide dynamic range and free from blooming," in *Proc. Custom Integr. Circuits Conf.*, Rochester, NY, USA, 1984, pp. 81–85.
- [24] D. Scheffer *et al.*, "Random addressable 2048 \times 2048 active pixel image sensor," *IEEE Trans. Electron Devices*, vol. 44, no. 10, pp. 1716–1720, Oct. 1997.
- [25] S. Decker *et al.*, "A 256 \times 256 CMOS imaging array with wide dynamic range pixels and column-parallel digital output," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2081–2091, Dec. 1998.
- [26] Y. Muramatsu, S. Kurosawa, M. Furumiyama, H. Ohkubo, and Y. Nakashiba, "A signal-processing CMOS image sensor using a simple analog operation," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 101–106, Jan. 2003.
- [27] Y. Egawa *et al.*, "A 1/2.5 inch 5.2Mpixel, 96 dB dynamic range CMOS image sensor with fixed pattern noise free, double exposure time read-out operation," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2006, pp. 135–138.
- [28] Y. Oike *et al.*, "A 121.8 dB dynamic range CMOS image sensor using pixel-variation-free midpoint potential drive and overlapping multiple exposures," in *Proc. Int. Image Sensor Workshop (IISW)*, Jun. 2007, pp. 30–33.
- [29] T. Nishibe *et al.*, "Auto-focus IC," *Fuji Electr. J.*, vol. 61, no. 7, pp. 470–474, 1988.
- [30] A. Guilvard *et al.*, "A digital high-dynamic-range CMOS image sensor with multi-integration and pixel readout request," *Proc. SPIE*, vol. 6501, Feb. 2007, Art. no. 65010L1.
- [31] G. G. Storm *et al.*, "Combined linear-logarithmic CMOS image sensor," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2004, pp. 116–117.
- [32] K. Hara, H. Kubo, M. Kimura, F. Murao, and S. Komori, "A linear-logarithmic CMOS sensor with offset calibration using an injected charge signal," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2005, pp. 345–346.
- [33] C. A. de Moraes Cruz, D. W. de Lima Monteiro, A. K. Pinto Souza, L. L. Furtado da Silva, D. Rocha de Sousa, and E. Gomes de Oliveira, "Voltage mode FPN calibration in the logarithmic CMOS imager," *IEEE Trans. Electron Devices*, vol. 62, no. 8, pp. 2528–2534, Aug. 2015.
- [34] M. Bae, B.-S. Choi, S.-H. Jo, H.-H. Lee, P. Choi, and J.-K. Shin, "A linear-logarithmic CMOS image sensor with adjustable dynamic range," *IEEE Sensors J.*, vol. 16, no. 13, pp. 5222–5226, Jul. 2016.
- [35] S. Cui *et al.*, "Combined linear-logarithmic CMOS image sensor with FPN calibration," in *Proc. IEEE Int. Conf. Integr. Circuits, Technol. Appl. (ICTA)*, Nov. 2018, pp. 128–129.
- [36] D. Arnaud, "Response curve programming of HDR image sensors based on discretized information transfer and scene information," in *Proc. Int. Symp. Electron. Imag. (IS&T)*, 2018, p. 400.
- [37] Y. Kagawa *et al.*, "Novel stacked CMOS image sensor with advanced Cu2Cu hybrid bonding," in *IEDM Tech. Dig.*, Dec. 2016, pp. 208–211.
- [38] T. Lule, "True flicker-free HDR solution for pixel and image sensor," Autosens, Horsham, U.K., Tech. Rep., 2016.
- [39] T. Nakamura *et al.*, "Recent progress of CMD imaging," in *Proc. IEEE Workshop CCDs Adv. Image Sensors*, Jun. 1997.
- [40] O. Yadid-Pecht and E. R. Fossum, "Wide intrascene dynamic range CMOS APS using dual sampling," *IEEE Trans. Electron Devices*, vol. 44, no. 10, pp. 1721–1723, Oct. 1997.
- [41] S. Cho, H. Seok Hong, H. Han, and Y. Choi, "Alternating line high dynamic range imaging," in *Proc. 17th Int. Conf. Digit. Signal Process. (DSP)*, Jul. 2011, pp. 1–6.
- [42] K. Nakazawa *et al.*, "3D sequential process integration for CMOS image sensor," in *IEDM Tech. Dig.*, Dec. 2021, pp. 30.4.1–30.4.4.
- [43] Y. Kimura, "Imaging sensor, imaging apparatus, electronic device, and imaging method with photoelectric conversion elements having different exposure times," U.S. Patent 9215387, Dec. 15, 2015.
- [44] M. Mase, S. Kawahito, M. Sasaki, Y. Wakamori, and M. Furuta, "A wide dynamic range CMOS image sensor with multiple exposure-time signal outputs and 12-bit column-parallel cyclic A/D converters," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2787–2795, Dec. 2005.
- [45] J. Solhusvik *et al.*, "A 1280 \times 960 3.75 μ m pixel CMOS imager with triple exposure HDR," in *Proc. Int. Image Sensor Workshop*, Jun. 2009, pp. 344–347.
- [46] C. Silsby *et al.*, "A 1.2 MP 1/3" CMOS image sensor with light flicker mitigation," in *Proc. Program Int. Image Sensor Workshop (IISW)*, 2015, pp. 8–11.
- [47] M. Oh *et al.*, "Automotive 3.0 μ m pixel high dynamic range sensor with led flicker mitigation," *Sensors*, vol. 20, no. 5, p. 1390, Mar. 2020.
- [48] C. Xu *et al.*, "A stacked global-shutter CMOS imager with SC-type hybrid-GS pixel and self-knee point calibration single frame HDR and on-chip binarization algorithm for smart vision applications," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2019, pp. 94–96.
- [49] J. Lee, "Offset and gain FPN calibrated linear-logarithmic image sensor with shared pixel architecture," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 12, pp. 3518–3521, Dec. 2021.
- [50] J. Bae, D. Kim, I. Hwang, and M. Song, "A high dynamic range CMOS image sensor with a digital configurable logarithmic counter," in *Proc. Eur. Conf. Circuit Theory Design (ECCTD)*, Sep. 2013, pp. 1–4.
- [51] J. Solhusvik *et al.*, "A comparison of high dynamic range CIS technologies for automotive applications," in *Proc. Int. Image Sensor Workshop (IISW)*, Jun. 2013, pp. 421–424.
- [52] T. Lule *et al.*, "High performance 1.3 MPix HDR automotive image sensor," in *Proc. Int. Image Sensor Workshop (IISW)*, Jun. 2015, pp. 381–384.
- [53] S. Velichko *et al.*, "140 dB dynamic range sub-electron noise floor image sensor," in *Proc. Int. Image Sensor Workshop (IISW)*, 2017, pp. 294–297.
- [54] S. Iida *et al.*, "A 0.68e-rms random-noise 121 dB dynamic-range sub-pixel architecture CMOS image sensor with LED flicker mitigation," in *IEDM Tech. Dig.*, Dec. 2018, p. 10.
- [55] Y. Sakano *et al.*, "A 132 dB single-exposure-dynamic-range CMOS image sensor with high temperature tolerance," in *IEEE ISSCC Dig. Tech. Papers*, vol. 7, Feb. 2020, pp. 106–108.
- [56] S. Velichko *et al.*, "Automotive 3 μ m HDR image sensor with LFM and distance functionality," in *Proc. Int. Image Sensor Workshop*, Sep. 2021, pp. 312–315.
- [57] B. Fowler *et al.*, "Wide dynamic range low light level CMOS image sensor," in *Proc. Int. Image Sensor Workshop (IISW)*, Jun. 2009, pp. 344–347.
- [58] H. Totsuka *et al.*, "An APS-H-size 250 Mpixel CMOS image sensor using column single-slope ADCs with dual-gain amplifiers," in *IEEE ISSCC Dig. Tech. Papers*, Jan./Feb. 2016, pp. 116–117.
- [59] A. Huggett, C. Silsby, S. Cami, and J. Beck, "A dual-conversion-gain video sensor with dewarping and overlay on a single chip," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 52–53.
- [60] D. Pates *et al.*, "An APS-C format 14 b digital CMOS image sensor with a dynamic response pixel," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 418–419.

- [61] N. Akahane, S. Sugawa, S. Adachi, K. Mori, T. Ishiuchi, and K. Mizobuchi, "A sensitivity and linearity improvement of a 100-dB dynamic range CMOS image sensor using a lateral overflow integration capacitor," *IEEE J. Solid-State Circuits*, vol. 41, no. 4, pp. 851–858, Apr. 2006.
- [62] T. Oikawa *et al.*, "A 1000 fps high SNR voltage-domain global shutter CMOS image sensor with two-stage LOFIC for *in-situ* fluid concentration distribution measurements," in *Proc. Int. Image Sensor Workshop*, Sep. 2021, pp. 258–261.
- [63] D. J. Griffiths and A. Wicks, "High speed high dynamic range video," *IEEE Sensors J.*, vol. 17, no. 8, pp. 2472–2480, Apr. 2017.
- [64] N. A. W. Dutton *et al.*, "A SPAD-based QVGA image sensor for single-photon counting and quanta imaging," *IEEE Trans. Electron Devices*, vol. 63, no. 1, pp. 189–196, Jan. 2016.
- [65] A. Boukhayma, A. Peizerat, and C. Enz, "A sub-0.5 electron read noise VGA image sensor in a standard CMOS process," *IEEE J. Solid State Circuits*, vol. 51, no. 9, pp. 2180–2191, Sep. 2016.
- [66] A. Matwyschuk *et al.*, "A real time 3D video CMOS sensor with time gated photon counting," in *Proc. 15th IEEE Int. New Circuits Syst. Conf. (NEWCAS)*, Jun. 2017, pp. 57–60.
- [67] E. R. Fossum, "Modeling the performance of single-bit and multi-bit quanta image sensors," in *IEEE ISSCC Dig. Tech. Papers*, vol. 7, Feb. 2019, pp. 166–167.
- [68] A. Gnanasambandam *et al.*, "High dynamic range imaging using quanta image sensors," in *Proc. Int. Image Sensor Workshop (IISW)*, vol. 23, 2019, pp. 218–221.
- [69] R. K. Henderson *et al.*, "A 256×256 40 nm/90 nm CMOS 3D-stacked 120 dB dynamic-range reconfigurable time-resolved SPAD imager," in *IEEE ISSCC Dig. Tech. Papers*, vol. 7, Feb. 2019, pp. 166–167.
- [70] A. Gnanasambandam *et al.*, "HDR imaging with quanta image sensors: Theoretical limits and optimal reconstruction," *IEEE Trans. Comput. Imag.*, vol. 6, pp. 1571–1585, 2020.
- [71] J. Ogi *et al.*, "A 124-dB dynamic-range SPAD photon-counting image sensor using subframe sampling and extrapolating photon count," *IEEE J. Solid-State Circuits*, vol. 56, no. 11, pp. 3220–3227, Nov. 2021.
- [72] J. Ogi *et al.*, "A 250 fps 124 dB dynamic-range SPAD image sensor stacked with pixel-parallel photon counter employing sub-frame extrapolating architecture for motion artifact suppression," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2021, pp. 113–115.
- [73] T. Willassen *et al.*, "A 1280×1080 4.2 μm split-diode pixel HDR sensor in 110 nm BSI CMOS process," in *Proc. Program Int. Image Sensor Workshop (IISW)*, 2015, pp. 377–380.
- [74] M. Innocent *et al.*, "Pixel with nested photo diodes and 120 dB single exposure dynamic range," in *Proc. Int. Image Sensor Workshop (IISW)*, vol. 13, 2019, pp. 95–98.
- [75] T. Asatsuma *et al.*, "Sub-pixel architecture of CMOS image sensor achieving over 120 db dynamic range with less motion artifact characteristics," in *Proc. Int. Image Sensor Workshop (IISW)*, vol. 31, 2019, pp. 250–253.
- [76] J. Solhusvik *et al.*, "A 1280×960 2.8 μm HDR CIS with DCG and split-pixel combined," in *Proc. Int. Image Sensor Workshop (IISW)*, vol. 32, 2019, pp. 254–257.
- [77] I. Takayanagi *et al.*, "An over 90 dB intra-scene single-exposure dynamic range CMOS image sensor using a 3.0 μm triple-gain pixel fabricated in a standard BSI process," *Sensors*, vol. 18, no. 1, p. 203, 2018.
- [78] T. Hirata *et al.*, "A 1-inch 17 Mpixel 1000 fps block-controlled coded-exposure back-illuminated stacked CMOS image sensor for computational imaging and adaptive dynamic range control," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2021, pp. 120–122.
- [79] J. Ma, D. Zhang, O. Elgendy, and S. Masoodian, "A photon-counting 4Mpixel stacked BSI quanta image sensor with 0.3e⁻ read noise and 100 dB single-exposure dynamic range," in *Proc. Symp. VLSI Circuits*, Jun. 2021, pp. 1–2.
- [80] M. Goto *et al.*, "In-pixel A/D converters with 120-dB dynamic range using event-driven correlated double sampling for stacked SOI image sensors," in *Proc. IEEE SOI-3D-Subthreshold Microelectron. Technol. Unified Conf. (S3S)*, Oct. 2016, pp. 1–3.
- [81] M. Kobayashi *et al.*, "A 1.8e^{-rms} temporal noise over 110-dB-dynamic range 3.4 μm pixel pitch global-shutter CMOS image sensor with dual-gain amplifiers SS-ADC, light guide structure, and multiple-accumulation shutter," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 74–75.
- [82] M. Goto *et al.*, "Quarter video graphics array digital pixel image sensing with a linear and wide-dynamic-range response by using pixel-wise 3-D integration," *IEEE Trans. Electron Devices*, vol. 66, no. 2, pp. 969–975, Feb. 2019.
- [83] C. Liu *et al.*, "A 4.6 μm , 512×512, ultra-low power stacked digital pixel sensor with triple quantization and 127 dB dynamic range," in *IEDM Tech. Dig.*, Dec. 2020, pp. 327–330.
- [84] K. Mori *et al.*, "A 4.0 μm stacked digital pixel sensor operating in a dual quantization mode for over 120 dB dynamic range," in *Proc. Int. Image Sensor Workshop*, Sep. 2021, pp. 308–311.
- [85] T. Vogelsang *et al.*, "Overcoming the full well capacity limit: High dynamic range imaging using multi-bit temporal oversampling and conditional reset," in *Proc. Int. Image Sensor Workshop (IISW)*, Jun. 2013, pp. 417–420.
- [86] Y. Sakano *et al.*, "224-ke saturation signal global shutter CMOS image sensor with in-pixel pinned storage and lateral overflow integration capacitor," in *Proc. Symp. VLSI Circuits*, Jun. 2017, pp. C250–C251.
- [87] Y. Fujihara *et al.*, "An over 120 dB dynamic range linear response single exposure CMOS image sensor with two-stage lateral overflow integration trench capacitors," in *Proc. Int. Symp. Electron. Imag. (IS&T)*, 2020, pp. 1–5.
- [88] I. Takayanagi *et al.*, "A 120-ke⁻ full-well capacity 160- $\mu\text{V}/\text{e}^-$ conversion gain 2.8- μm backside-illuminated pixel with a lateral overflow integration capacitor," *MDPI Sensors*, vol. 19, no. 24, 5572, 2019.
- [89] H. Shike *et al.*, "A global shutter wide dynamic range soft X-ray CMOS image sensor with backside-illuminated pinned photodiode, two-stage lateral overflow integration capacitor, and voltage domain memory bank," *IEEE Trans. Electron Devices*, vol. 68, no. 4, pp. 2056–2063, Apr. 2021.
- [90] M. Oh *et al.*, "3.0 μm Backside illuminated, lateral overflow, high dynamic range, LED flicker mitigation image sensor," in *Proc. Program Int. Image Sensor Workshop (IISW)*, vol. 34, 2019, pp. 262–265.
- [91] C. Roda Neve *et al.*, "High-density and low-leakage novel embedded 3D MIM capacitor on Si interposer," in *Proc. IEEE Int. 3D Syst. Integr. Conf. (3DIC)*, Nov. 2016, pp. 1–4.
- [92] T. Haruta *et al.*, "A 1/2.3inch 20 Mpixel 3-layer stacked CMOS image sensor with DRAM," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 76–77.
- [93] H. Togashi *et al.*, "Three-layer stacked color image sensor with 2.0- μm pixel size using organic photoconductive film," in *IEDM Tech. Dig.*, Dec. 2019, pp. 386–389.
- [94] M. Oka *et al.*, "3D stacked CIS compatible 40 nm embedded STT-MRAM for buffer memory," in *Proc. Symp. VLSI Technol.*, Jun. 2021, pp. 1–2.
- [95] N. Priyadarshini *et al.*, "A high dynamic range CMOS image sensor using programmable linear-logarithmic counter for low light imaging applications," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Oct. 2020, pp. 1–5.
- [96] S. Farsiu, M. D. Robinson, M. Elad, and P. Milanfar, "Fast and robust multiframe super resolution," *IEEE Trans. Image Process.*, vol. 13, no. 10, pp. 1327–1344, Oct. 2004.
- [97] W. Shi *et al.*, "Real-time single image and video super-resolution using an efficient sub-pixel convolutional neural network," in *Proc. IEEE Conf. Comput. Vis. Pattern Recognit. (CVPR)*, Jun. 2016, pp. 1874–1883.
- [98] T. Geurts *et al.*, "A 98 dB linear dynamic range, high speed CMOS image sensor," in *Proc. Program Int. Image Sensor Workshop (IISW)*, May 2017, pp. 282–285.
- [99] P. Sampath *et al.*, "A 12Mpixel 1.3' optical format CMOS HDR image sensor achieving single-exposure flicker-free 90 dB dynamic range in GS shutter mode and over 110 dB dynamic range in 2-exposure ERS mode," in *Proc. Program Int. Image Sensor Workshop (IISW)*, Sep. 2021, pp. 320–323.
- [100] M. Guidash *et al.*, "Floating diffusion dark current and dark signal non-uniformity reduction for high dynamic range overflow collection pixels in high temperature applications," in *Proc. Program Int. Image Sensor Workshop (IISW)*, Jun. 2019, pp. 68–71.
- [101] M. Innocent *et al.*, "Automotive 8.3 MP CMOS image sensor with 150 dB dynamic range and light flicker mitigation," in *IEDM Tech. Dig.*, Dec. 2021, p. 30.
- [102] P. Coudrain *et al.*, "Setting up 3D sequential integration for back-illuminated CMOS image sensors with highly miniaturized pixels with low temperature fully depleted SOI transistors," in *IEDM Tech. Dig.*, Dec. 2008, pp. 1–4.
- [103] J. Michailos, "Innovative fine pitch architectures dedicated to image sensors: From hybrid bonding to 3D sequential integration," presented at the ESSCIRC/ESSDERC Educ. Event, 2020.