TCAD Modeling of Temperature Activation of the Hysteresis Characteristics of Lateral 4H-SiC MOSFETs

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***Abstract*— We investigate the temperature dependence of the hysteresis in the transfer characteristics of 4H silicon carbide (4H-SiC) lateral MOSFETs. Within temperatures ranging from 150 to 300 K, we experimentally characterize the hysteresis width as the difference of the threshold voltage between up and down sweeps. We observe a considerable increase in the hysteresis width toward lower temperatures. When the gate voltage sweeps up, the threshold voltage shifts toward positive gate voltages. This shift is maintained even during the subsequent down sweep. We attribute this behavior to acceptor-like border traps, which get more negatively charged at higher gate voltages. These traps are presumably located near the SiC/SiO_2 interface with energy levels close to the SiC conduction band edge. Using a two-state non-radiative multi-phonon model, we calculated capture and emission times to show that the hysteresis width corresponds to the charge stored on these traps and, hence, possesses an intrinsic temperature dependence due to the transition barriers.**

***Index Terms*— 4H silicon carbide (4H-SiC), border traps, hysteresis, interface traps, MOSFETs, non-radiative multi-phonon (NMP) model, technology computer-aided design (TCAD) modeling.**

I. Introduction

THE 4H silicon carbide (4H-SiC) polytype is a promising material for high-power, high-frequency, and high-temperature electronics having a lot of unique properties, including a wide bandgap, good thermal conductivity, and high breakdown electric field. However, the SiC/SiO_2 interface exhibits a significant defect density with electrically active border and interface traps, resulting in a severely perturbed channel mobility in comparison with the Si/SiO_2 interface [1]–[3]. In addition, the charge stored on these traps results in deteriorated device electrostatics. Due to the coupling of the defects to the surrounding phonon system, the charge transfer kinetics are strongly temperature-dependent. This effect is believed to be responsible for the strongly temperature-dependent threshold voltage shift (ΔV_{th}) [Fig. 1 (top)] as well as the temperature dependence of the hysteresis width ΔV_{H}. This width is determined as the threshold voltage difference between the up and down sweeps of V_{gs} at a chosen reference current $I_{\mathrm{d}}^{\mathrm{ref}}$ [Fig. 1 (bottom)]. Previous experiments have shown that hysteresis is a recoverable phenomenon that does not increase with operating time [4], [5]. However, during the operation of the circuit, the device can turn-off at a higher V_{gs} than turn-on, due to the hysteresis effect [6]. This is an adverse effect that changes the device characteristics [4]. The theoretical assessments of transfer and output characteristics and especially reliability issues such as bias temperature instabilities (BTIs) of SiC transistors have been the subject of research by various groups [7]–[10], [12]–[22]. Also, BTI and, as a consequence, the hysteresis at a bipolar ac signal in the 4H-SiC transistors were characterized using capture and emission time (CET) maps [23]. Furthermore, a recent modeling approach has linked the observed hysteresis in SiO_2/MoS_2 devices to defects at the channel–oxide interface, which can be described by the non-radiative multi-phonon (NMP) theory [24]. However, the temperature dependence of the hysteresis width of transfer characteristics based on the NMP theory has not been presented yet.

In this article, we present a temperature-dependent technology computer-aided design (TCAD) modeling approach, which combines Shockley–Read–Hall (SRH) theory including mobility degradation for interface defects and NMP transitions for charge transfer reactions associated with defects in the oxide. The utilized two-state defect model in this work is based on the original implementation of a four-state NMP model [25], [26].

II. Devices and Experiment

We used lateral 4H-SiC nMOSFETs with an n^+ poly gate. We assume an oxide thickness of 50 nm and a gate length

Manuscript received February 17, 2022; revised April 1, 2022; accepted April 5, 2022. Date of publication April 19, 2022; date of current version May 24, 2022. This work was supported in part by the Austrian Federal Ministry for Digital and Economic Affairs and the National Foundation for Research, Technology and Development, and Austrian Science Fund (FWF), under Project 31204-N30; and in part by the Open Access Funding Program, TU Wien Bibliothek. The review of this article was arranged by Editor D. Sheridan. *(Corresponding authors: Alexander Vasilev; Michael Waltl.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2022.3166123.

Digital Object Identifier 10.1109/TED.2022.3166123

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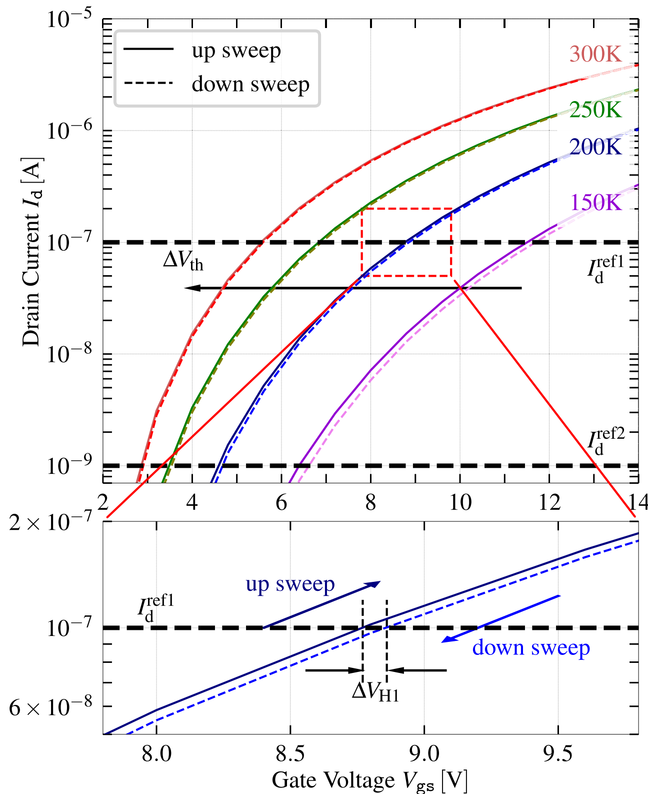

Fig. 1. Measured $I_d - V_{gs}$ curves at $T = 150, 200, 250$, and 300 K using up/down V_{gs} sweeps. Two reference drain currents $I_d^{ref1,2}$ have been used to determine two hysteresis widths ΔV_{H1} and ΔV_{H2} (bottom—for visual clarity, only ΔV_{H1} for $T = 200$ K is presented) as the difference of the corresponding voltages during the up and down V_{gs} sweeps.

of 7.5 μm, see Fig. 2 (left). This oxide layer was formed on the Si-face substrate by chemical vapor deposition. $I_d - V_{gs}$ curves were measured at a fixed drain voltage of $V_{ds} = 0.1$ V while V_{gs} is swept up and down within the range of 0–20 V at a sweep rate of 3.2 V/s, see Fig. 2 (right). A step width of 0.8 V for the gate bias has been used. Two hysteresis widths, ΔV_{H1} and ΔV_{H2}, are defined as the difference between up and down ΔV_{th} values corresponding to two reference drain currents ($I_d^{ref1} = 10^{-7}$ A and $I_d^{ref2} = 10^{-9}$ A, see Fig. 1). The hysteresis width has been extracted for operating temperatures between 150 and 300 K.

III. Modeling Framework

Fig. 1 shows that the $I_d - V_{gs}$ characteristics are shifted by ~5.5 V toward higher V_{gs} at lower temperatures. We attribute this behavior to interface and border traps, which are located within a few nanometers of the SiC/SiO_2 interface [7], [9], [27]. When V_{gs} sweeps up, defects can change their charge state, thereby leading to a threshold voltage shift ΔV_{th}, commonly referred to as BTI [26]. Furthermore, we observe a positive ΔV_{th} shift during the down sweep compared with the up sweep in the $I_d - V_{gs}$ curves, which is more pronounced at low temperatures.

To correctly describe the device electrostatics and, subsequently, the subthreshold swing (SS) and the threshold voltage drift at various temperatures, we employed the Sentaurus TCAD tool in conjunction with the following models [28].

1) Mobility degradation [10], [29], [30].
2) SRH for fast interface traps [13], [31].

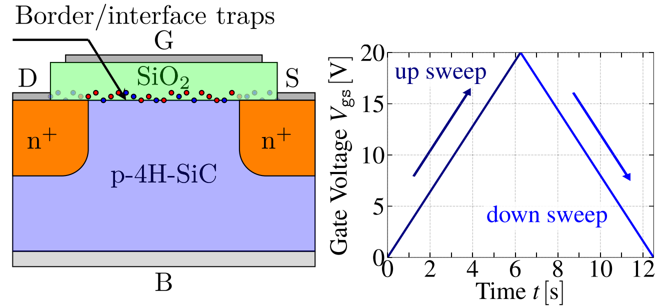

Fig. 2. Left: The commonly used lateral 4H-SiC transistor. The possible defects leading to a drift of the threshold voltage are shown. Right: This shows how the gate voltage is swept. The up-sweep curve (dark blue) starts from 0 V. The down-sweep curve (blue) starts from +20 V.

3) NMP for slow border traps [25], [26].

A. Mobility Degradation

To properly describe the experimental $I_d - V_{gs}$ characteristics within our simulations, mobility models for MOS devices are required. These models include phonon scattering μ_{Ph} and Coulomb scattering μ_C components [10], [29], [30]. Coulomb scattering is dominant, because there is a large number of charge centers at the interface that concentration depends on temperature and deteriorates the channel mobility. At the same time, in long-channel MOSFETs with moderate- to low-channel doping levels, inversion-layer mobility is limited by phonon scattering [30]. In a simplified way, the effective mobility is calculated as $1/\mu_{eff} = 1/\mu_{Ph} + 1/\mu_C$, in which the coulomb component is proportional to $\mu_C \propto \mu_0 (T/300)^\alpha / N_{it}$. In this work, we use $\mu_0 = 10$ cm^{2}V^{-1}s^{-1}, $\alpha = 2.8$, and $N_{it}(T)$ is the temperature-dependent interface charge density in cm^{-2}.

B. Fast Interface Traps

To explain the $I_d - V_{gs}$ curves from Fig. 1, acceptor-like interface traps, which have been previously identified in the SiC/SiO_2 system, were used [10], [11], [13], [15], [34]–[36]. Compared with border traps, interface traps have a narrower distribution of time constants [26] and can only affect the SS of the transfer characteristic. These traps are fast and reach their thermodynamic equilibrium state during our measurement time and, therefore, do not contribute to the hysteresis during the gate voltage sweep [24]. Thus, electrically active interface traps are directly incorporated in the mobility degradation model. The parameters for the SRH model are shown in Table I. By employing these parameters, the measured gate voltage up sweep can be reproduced with high accuracy, as shown in Fig. 3. The defect density of the acceptor-like traps D_{it} is exponentially increasing toward the SiC conduction band edge, see Fig. 4 (red) [13]. However, the high concentration of acceptor-like traps results in a severe positive threshold voltage shift toward higher V_{gs} values, substantially larger than the experimentally observed ones. Hence, we introduced fixed positive traps N_{it}^{fix} to compensate for such a large V_{th} shift [34].

C. Slow Border Traps

We assume that not only interface traps but also border traps affect the threshold voltage shift. This shift stems from acceptor-like traps that can capture electrons from the channel and, hence, become negatively charged. The concentration of

TABLE I
PARAMETERS FOR INTERFACE TRAPS

Parameter	Value
Interface trap concentration D_{it}, $\mathrm{eV}^{-1}\mathrm{cm}^{-2}$	2.6×10^{13}
Acceptor-like defect density D_{ox}, cm^{-2}	2.4×10^{12}
Positive interface trap concentration $N_{\mathrm{it}}^{\mathrm{fix}}$, cm^{-2}	7.0×10^{11}
Exponential energy distribution σ_E, eV	0.1
Capture cross section for electrons σ_e^0, cm^{-2}	10^{-10}
Capture cross section for holes σ_h^0, cm^{-2}	10^{-12}

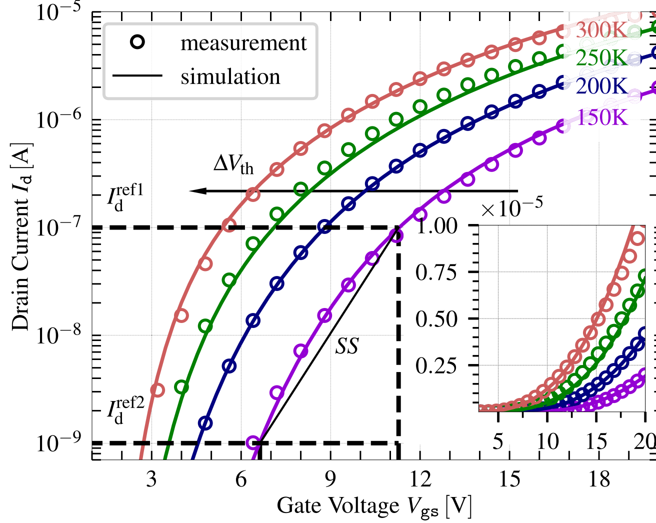

Fig. 3. Simulated versus measured $I_{\mathrm{d}} - V_{\mathrm{gs}}$ up-sweep curves at $T = 150$, 200, 250, and 300 K. Two reference drain currents $I_{\mathrm{d}}^{\mathrm{ref1,\,2}}$ have been used to determine two threshold voltages and SSs.

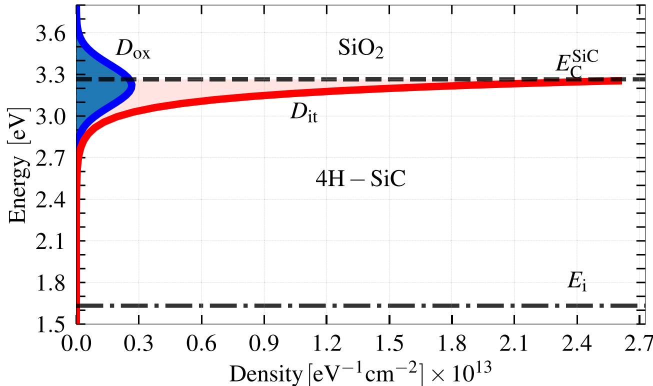

Fig. 4. Densities for the interface traps D_{it} (red—exponential distribution) and for the border acceptor-like traps D_{ox} (blue—Gaussian distribution).

these traps has been obtained by reproducing the experimental data in our simulations considering the ΔV_{th} shift and the hysteresis width $\Delta V_{\mathrm{H1,2}}$ at $T = 200$ K, see Fig. 5. The acceptor-like traps with a $0/{-1}$ charge transition level close to the conduction band edge $E_{\mathrm{t}}^{\mathrm{A}} \sim E_{\mathrm{C}}$ are assumed to be normally distributed with a sigma of $\sigma_{E_{\mathrm{t}}^{\mathrm{A}}} = 0.15$ eV and a defect density of $D_{\mathrm{ox}} \sim 2.4 \times 10^{12}\ \mathrm{cm}^{-2}$, see Fig. 4 (blue) [7]. The parameters used for the interface and border traps are in good agreement with theoretical and experimental data obtained by other groups [37]–[41]. During V_{gs} sweeps, the acceptor-like traps are involved in charging and discharging kinetics with their corresponding CET. As V_{gs} increases, the average capture time of all traps becomes much smaller than the emission time, and the traps become charged [26]. To model CETs,

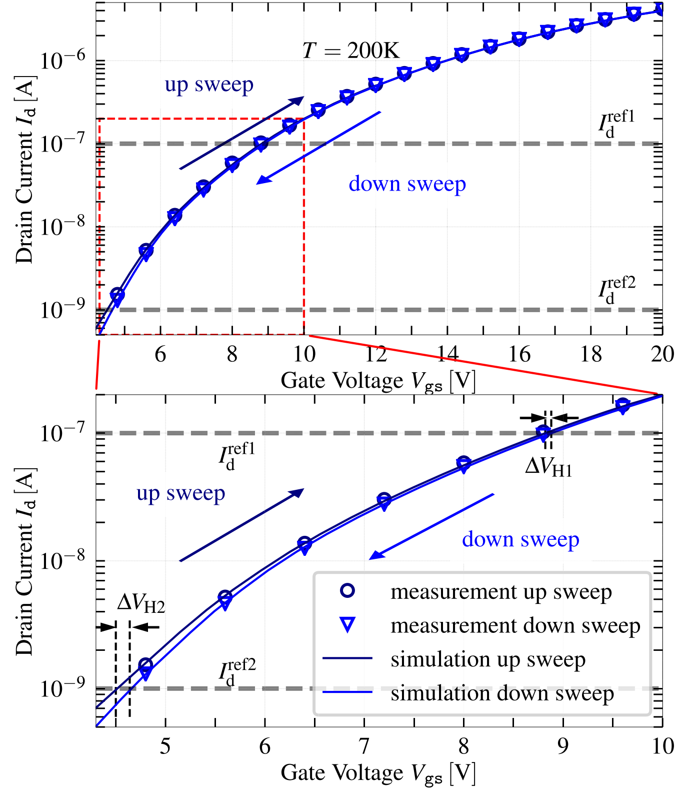

Fig. 5. Simulated versus measured $I_{\mathrm{d}} - V_{\mathrm{gs}}$ curve at $T = 200$ K. The V_{th} shift and $\Delta V_{\mathrm{H1,\,2}}$ width were obtained by the NMP model with the effect of charging acceptor-like traps.

a two-state variant of the NMP model has been utilized [25], [26]. In this model, the intersection point (IP) of two parabolas, which represent the potential energy of the two defect states, determines the energy barriers for the forward and backward processes (i.e., the charge CETs). For the acceptor-like trap, these barriers are determined by the relaxation energy $S = 0.1 \pm 0.01$ eV and the parabolic curvature ratio $R = 1.0 \pm 0.01$. Due to the different forward and backward barriers, an asymmetry in the CET is introduced [25], [26]. It has to be noted that the amorphous SiO_2 leads to a considerable distribution of the structural properties. In our case, due to the fast sweeping rates, only defects that contribute to the hysteresis at the applied gate bias and temperature are considered. As a result, less relaxation energy with narrow distribution was used in the simulation compared with the typically assumed parameters [7], [19]. At the same time, the distribution of the trap energy is wide enough to create a variety of barrier heights for the calculation of the charge transitions. Thus, some of the traps out of the large ensemble used in our simulation are too slow (in other words, emission time is too large) and cannot return back to their initial state during the down sweep of the gate voltage. These charged traps are responsible for the observed hysteresis width. At high temperatures, both of the aforementioned processes have shorter characteristic transition times, and thus, traps can become neutralized faster, and as a consequence, both ΔV_{th} and $\Delta V_{\mathrm{H1,2}}$ decrease.

As one can see, for both up and down sweeps, the combination of acceptor-like interface and border defects finally leads to a good agreement of the simulation with experimental data, as shown in Fig. 5.

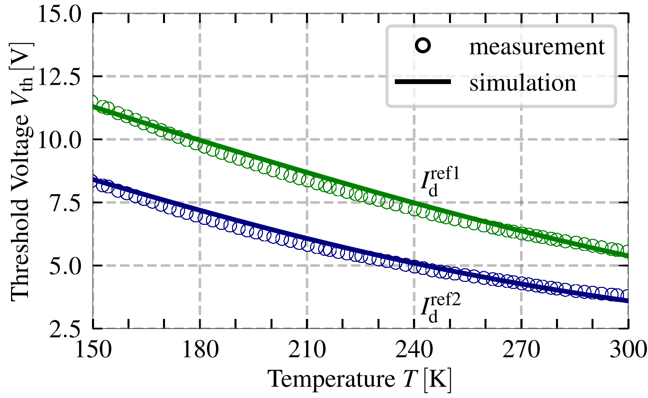

Fig. 6. Simulated versus measured threshold voltage at various temperatures and two references for the drain current. It can be seen that traps can capture a charge, but at the same time, most of these emit faster at the elevated T and decrease the threshold voltage shift. At lower T, traps emit a charge slower, and the threshold voltage shift increases.

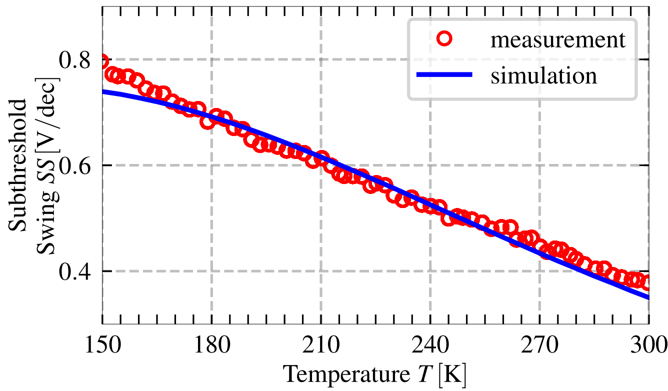

Fig. 7. Simulated versus measured SS at various temperatures. $SS = \partial V_{gs}/\partial I_d$.

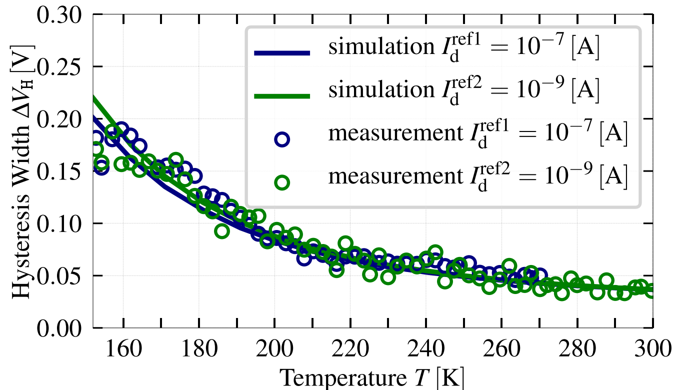

Fig. 8. Measured and simulated widths of the hysteresis $\Delta V_{H1,2}$ in the temperature range from 150 to 300 K using two different reference drain current levels (I_d^{ref1}, I_d^{ref2}).

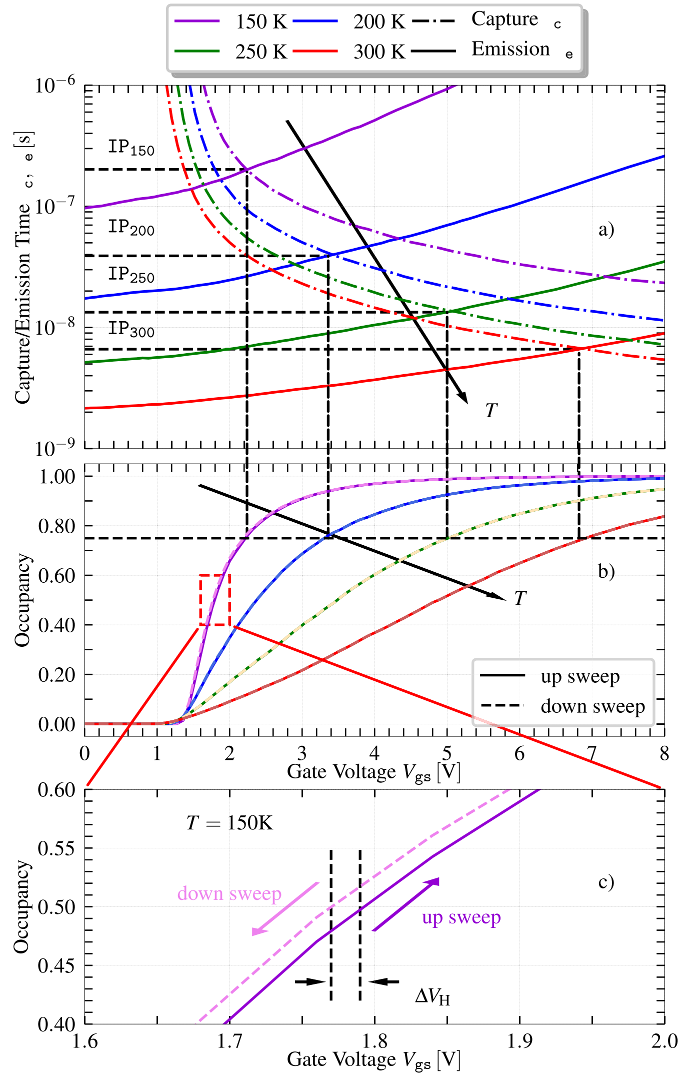

Fig. 9. (a) Modeling charge capture/emission times as a function of V_{gs} (the median data of all trap ensemble). (b) Trap occupancy at $T = 150$, 200, 250, and 300 K. (c) Trap occupancy at $T = 150$ K for up/down V_{gs} sweeps.

IV. Results and Discussion

Fig. 5 shows the $I_d - V_{gs}$ curve simulated for $T = 150$, 200, 250, and 300 K, where one can see that our modeling framework accurately captures the transfer characteristics. In particular, the trend for the temperature dependence of V_{th}, see Fig. 6, and SS, see Fig. 7, are well represented by our approach.

If the gate voltage sweeps up, the acceptor-like interface traps become charged and enhance the effect of Coulomb scattering in the inversion layer and also affect the positive threshold voltage shift. When the temperature increases, the transition rates increase, especially the emission rates, and the number of charged traps decreases. Hence, the threshold voltage shift also decreases, see Fig. 6, similar to the SS as is shown in Fig. 7.

Due to the lower amount of charge stored in the defects close to the interface, Coulomb scattering becomes less pronounced with increasing temperature, which enhances the inversion layer mobility [29]. In addition, the hysteresis during the up and down sweeps is accurately reproduced by the simulation setup. Fig. 5 shows the $I_d - V_{gs}$ curve simulated for $T = 200$ K. Fig. 8 shows the hysteresis width $\Delta V_{H1,2}$ as a function of temperature T. At low temperatures $\Delta V_{H1,2}$ is large, and at high temperatures, it becomes smaller.

To better understand the hysteresis behavior, we have calculated the average CETs of a large ensemble of defects together with their trap occupancy, see Fig. 9. Our simulation shows that during the up sweep, when $V_{gs} < V_{th}$, the emission time τ_e is smaller than the capture time τ_c, $\tau_e \ll \tau_c$ [Fig. 9(a)]; hence, electrons are emitted to

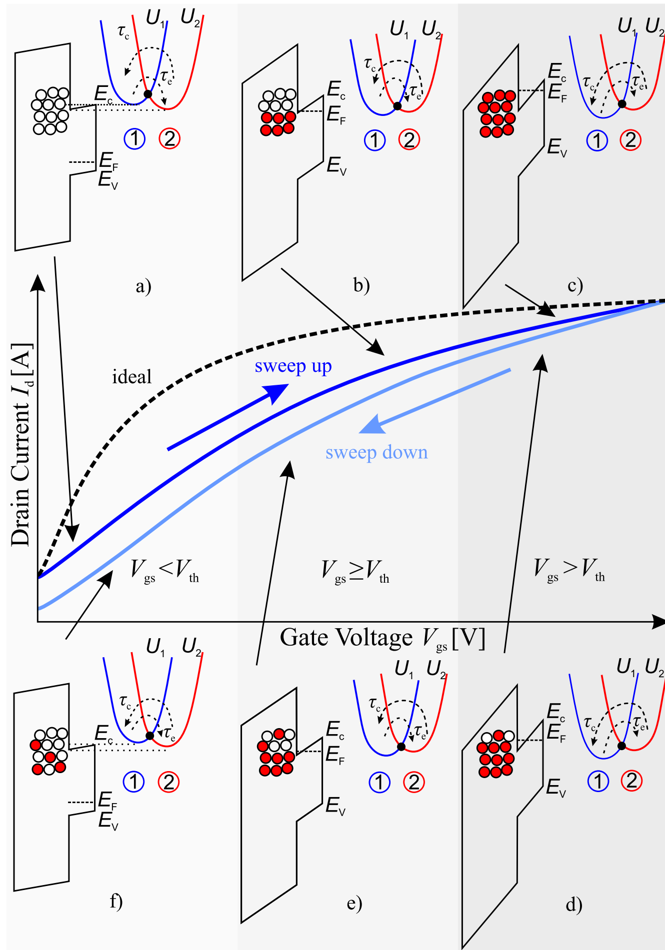

Fig. 10. Hysteresis of transfer characteristics of a 4H-SiC MOSFET is schematically shown (center). (a)–(f) Also, the band diagrams of the SiC/SiO$_2$ interface region with acceptor-like border traps close to $E_{c,\,SiC}$ are schematically shown at different times during the gate bias up and down sweeps. The harmonic approximations of potential energy surfaces for the average defects charged state 1 (blue) and neutral state (red), i.e., $E_{c,\,SiC}$, are displayed, showing the energetic barriers for calculating the CETs, which are determined by the IP (black dot). This barrier changes by shifting the parabolas relative to each other by altering the gate bias. (a) Initially, the capture time is large; i.e., large capture barrier and defects remain in the neutral state. (b) and (c) With increasing the gate bias, the capture barrier is reduced, and more defects become negatively charged, thereby shifting the $I_d - V_{gs}$ curve toward more positive bias. (d)–(f) At the subsequent down sweep, the barrier for electron emission toward the channel is reduced again; however, some of the previously charged defects do not fully discharge during the down sweep, as their emission time constants exceed the sweep duration, even at lower biases. The strong asymmetry between CETs inherent to the NMP model enables us to capture this effect in our simulation.

the channel, and the defect occupancies are mostly zero [Fig. 9(b)]. This effect is schematically shown in Fig. 10(a). When $V_{gs} \geq V_{th}$, the trap levels of the defects cross the Fermi level of the channel and the capture times equal the emission times. It is shown as an IP, see Fig. 9(a). In this regime, the occupancy of the traps is higher than 50% in steady state, while for transient simulations, it depends on the sweep rate, see Fig. 9(b) (horizontal dashed line). Thus, electrons are captured due to the emission time being larger than the capture time $\tau_e \geq \tau_c$, and traps become negatively charged. As a result, V_{th} is shifted toward positive gate voltages, see Fig. 10(b). One can see in Fig. 9(a) that both CETs decrease with T, and their temperature-dependent IP shifts toward higher V_{gs}. Accordingly, the trap occupancies, even at high V_{gs}, drop significantly at elevated T [see Fig. 9(b)]. To reach the same occupancy [horizontal dashed line in Fig. 9(b)] for $T = 150$ K, a lower V_{gs} is needed. This produces a more significant V_{th} shift than the one observed at $T = 300$ K. During the down sweep, at high temperatures, electrons tend to be emitted back to the channel. Thus, most of the traps become neutralized, and the obtained $\Delta V_{H1,2}$ is small, see Fig. 10(e). The $\Delta V_{H1,2}$ widths depend on the ratio between τ_c and τ_e or the IP of the τ_c/τ_e characteristics, which determines the trap occupancy. Also, we need to consider the sweep down time t_{down} (in our case, $t_{down} \sim 6$ s), which can influence the hysteresis width. If $\tau_e \gg \tau_c$ and $\tau_e < t_{down}$, the defect can capture the electron and immediately emit a captured charge during the sweep down. However, if the relationship is reversed $\tau_e > t_{down}$, some of the defects keep their charge state, see Fig. 10(e) and (f). The IP shows the distance between t_{down} and τ_e. Fig. 9(a) shows that IP$_{150}$ is much larger than IP$_{300}$. Hence, when the temperature decreases, not all traps become neutralized, see Fig. 10(f). These traps remain occupied and shift V_{th} [Fig. 9(c)], which results in a large hysteresis, see Fig. 8. The result has a good agreement with other hysteresis measurements [4], [43].

V. Conclusion

We have presented a modeling approach to calculate the temperature activation of the hysteresis width of the transfer characteristics of lateral 4H-SiC MOSFETs. Our investigations show that this behavior is a direct consequence of the charging and discharging kinetics of border traps in the oxide. The hysteresis width and ΔV_{th} shift are caused by an asymmetry of the CETs, which are inherently temperature-dependent. Note that models based on elastic tunneling cannot explain the strong T activation of the hysteresis width, such as the Heiman model [42]. For the calculation of the charge CETs of the defects, we use a two-state NMP model and show that during the down sweep of the gate voltage, traps can remain occupied, an effect that becomes more pronounced at low temperatures and gives rise to an increased hysteresis width. Our modeling approach fully captures the measurement trends in which hysteresis and ΔV_{th} shift decrease with temperature. Finally, it has to be mentioned that the employed trap energy distributions to explain the width of the hysteresis are consistent with trap bands extracted from recent positive BTI investigations, which indicates the high accuracy of our work [7], [19].

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