Sub-Linear Current Voltage Characteristics of Schottky-Barrier Field-Effect Transistors

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***Abstract*—This article studies the sub-linearity of the output characteristics measured in Schottky-barrier metal-oxide-semiconductor field-effect transistors with simulations and experiments. It is shown that the sub-linearity is not due to the forward-biased Schottky diode at the drain contact interface but due to the drain bias impact on the source-side Schottky-barrier, resulting in an increased carrier injection with increasing drain–source voltage. The simulation results are confirmed with the measurements of fabricated dual-gate Schottky-barrier transistors.**

***Index Terms*—MOSFET, non-equilibrium Green's function, program-gate at drain (PGAD), program-gate at source (PGAS), reconfigurable MOSFET, Schottky-barrier MOSFET, silicidation, silicon nanowire, silicon-on-insulator, tetramethylammonium hydroxide (TMAH).**

I. Introduction

IN RECENT years, Schottky-barrier MOSFETs with metallic source and drain contacts have been attracting a great deal of interest since replacing the doped source/drain regions with metals allows avoiding dopant-related issues prevalent in nanoscale conventional MOSFETs. The latter include, for instance, dopant deactivation in nanostructures [1]–[3] as well as device-to-device variability due to random dopant effects [4]–[8]. More recently, the so-called reconfigurable MOSFETs have received an increasing attention [9]–[15]. Reconfigurable transistors employ metallic source/drain contacts to enable carrier injection into the conduction and valence bands and are thus SB-MOSFETs with one or two additional gates. Furthermore, transistor devices based on novel materials such as 2-D materials or carbon nanotubes are usually fabricated in a straightforward way by depositing metals on top of the material. However, in most cases, Fermi-level pinning at the metal–semiconductor interface occurs within the bandgap giving rise to substantial Schottky barriers (SBs) at the contact channel interfaces that strongly impact the electrical characteristics of such SB-MOSFETs, leading to a deteriorated ON-state performance and a degraded switching behavior [16]. One of the most predominant features of SB-MOSFETs is a distinct diode-like exponential current increase (in the following denoted as sub-linear behavior) in the triode operation regime of the I_d–V_{ds} characteristics for small bias voltages [17]–[20] which is highly undesirable with respect to applying such devices in logic circuits. Although SB-MOSFETs have been studied intensively, the sub-linear behavior of the output characteristics has been attributed to the forward-biased Schottky junction at the drain end of the transistor [17], [18], [20]. In the present publication, however, the sub-linearity of SB-MOSFETs is studied with simulations and experiments and it is shown that the sub-linearity is actually due to the source-side SB rather than the drain-side SB. The reason for this is the impact of the drain on the source-side SB provided by the charge within the channel in the ON-state of the device. Note that this is a different mechanism compared to a recent publication where the drain's impact on the source was due to short channel effects (SCEs) [21]. Hence, the sub-linearity is not a consequence of SCEs and also appears in long-channel SB-MOSFETs. Attributing the sub-linearity falsely to the drain-side SB may thus lead to interpreting linear I_d–V_{ds} characteristics of SB-MOSFETs as proof for a low SB at the drain end of the device [19], [20].

II. Device Simulation

In order to study the sub-linear I_d–V_{ds} behavior of SB-FETs, self-consistent Poisson–Schrödinger simulations using the non-equilibrium Green's function formalism (NEGF) have been carried out [22], [23]. To this end, a nanowire (NW) field-effect transistor with metallic contacts exhibiting an SB Φ_{SB}^{s} at the source and Φ_{SB}^{d} at the drain contact is considered as illustrated in Fig. 1. The source and the drain are assumed to be in direct contact with the nanowire that is not only appropriate for, for example, silicide contacts, but also describes contacts deposited onto the nanowire well as long as the metal–nanowire coupling is not weak. A nanowire of diameter d_{nw} is assumed that is thin enough to justify 1-D electronic transport. Such a thin nanowire can be considered to be fully depleted within a broad range of channel doping concentrations. Hence, channel doping will merely shift the built-in potential Φ_{bi}. For simplicity, the nanowire is therefore

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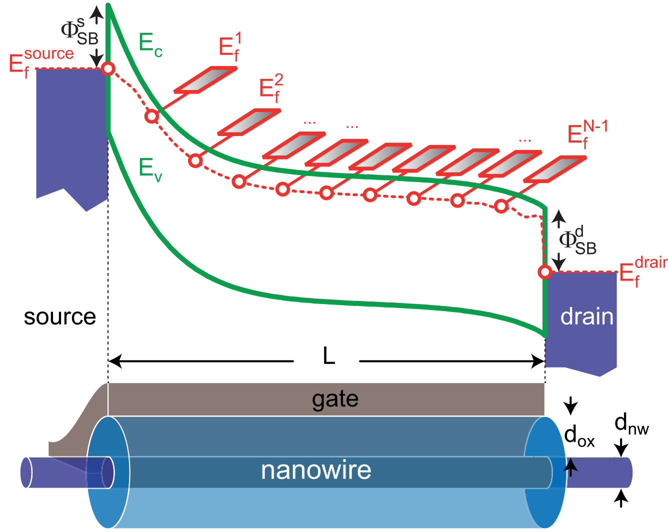

Fig. 1. Conduction and valence bands along the current transport direction of an SB-MOSFET. Metallic source/drain contacts with SB Φ^s_{SB} and Φ^d_{SB} are considered. One-dimensional electronic transport is assumed, and scattering is taken into considerations with Buettiker probes. The lower part shows a schematic of the device.

assumed to be undoped. The electrostatics of such a device can be described well with the following 1-D modified Poisson equation [24]–[26]:

$$\frac{\partial^2 \Phi_f(x)}{\partial x^2} - \frac{\Phi_f(x) - \left(\Phi_g + \Phi_{\text{bi}}\right)}{\lambda^2} = -\frac{e^2 n(x)}{\varepsilon_0 \varepsilon_{\text{nw}}} \tag{1}$$

where λ is a screening length scale for potential variations and reflects the particular device geometry under consideration [16], [27]. Φ_g and Φ_{bi} are the gate- and the built-in potential energies and $\Phi_f(x)$ is the potential energy at the channel–dielectric interface. In addition, $n(x)$ is the mobile charge density, and $\varepsilon_{0,\text{nw}}$ are the vacuum and the relative permittivity of the NW, respectively. In the following, devices are considered that may appear unreasonable in terms of the parameters chosen. However, using (1) together with 1-D electronic transport allows to adjust the charge density and hence its impact on the potential distribution within the channel while keeping the electrostatics due to the device geometry (expressed through the screening length λ) unchanged. For instance, in the case of a single-gate device, $\lambda = ((\varepsilon_{\text{nw}}/\varepsilon_{\text{ox}}) d_{\text{nw}} d_{\text{ox}})^{1/2}$ (even in the case of an NW MOSFET [27]), the same screening can be obtained with either the diameter of the NW $d_{\text{nw}} = 1$ nm and the gate oxide thickness $d_{\text{ox}} = 20$ nm or $d_{\text{nw}} = 5$ nm and $d_{\text{ox}} = 4$ nm. Thus, the screening length λ will be the same for both cases. The charge density and therefore its impact on the potential will, however, be different.

If not stated otherwise, the channel length L of the device is assumed to be significantly larger than λ such that SCEs are completely suppressed. At the same time, L is small enough to justify that the details of the carrier scattering within the channel are irrelevant [23]. We, therefore, use the so-called Buettiker probes to mimic inelastic scattering within the channel and a mean free path of $l_{\text{mfp}} = 50$ nm is assumed [28]. The output characteristics, that is, the drain current versus the drain–source bias, of the following devices

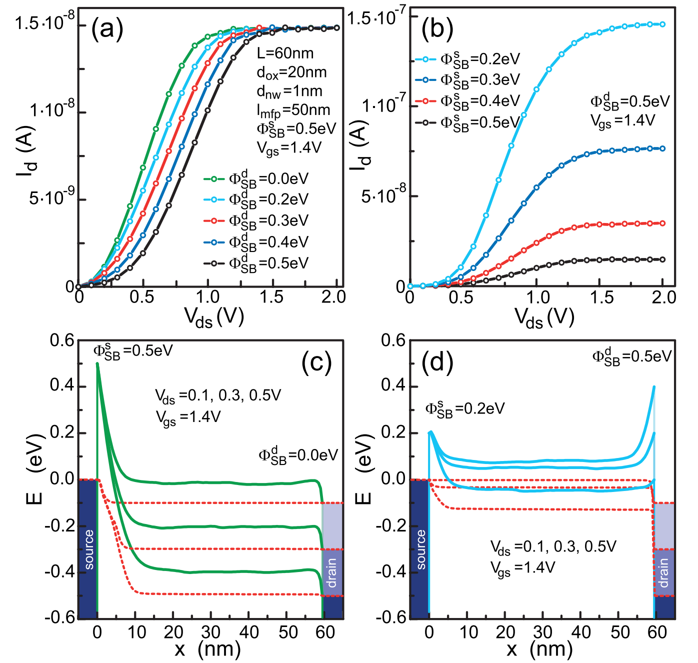

Fig. 2. (a) Output characteristics for a fixed $V_{\text{gs}} = 1.4$ V of an NW SB-MOSFET (see the figure for the simulation parameters) with $\Phi^s_{\text{SB}} = 0.5$ eV and varying Φ^d_{SB}. (b) Output characteristics of the same SB-MOSFET with $\Phi^d_{\text{SB}} = 0.5$ eV and varying Φ^s_{SB}. Band profiles (solid lines) and quasi-Fermi level (dashed line) in the case of (c) $\Phi^s_{\text{SB}} = 0.5$ eV and $\Phi^d_{\text{SB}} = 0$ eV, and (d) $\Phi^s_{\text{SB}} = 0.2$ eV and $\Phi^d_{\text{SB}} = 0.5$ eV for varying V_{ds}.

are simulated and the result for a constant V_{gs} is plotted in Fig. 2: $L = 60$ nm, $l_{\text{mfp}} = 50$ nm, $d_{\text{nw}} = 1$ nm, a bandgap of $E_g = 1$ eV, and an effective mass of $m^\star = 0.2\ m_0$ in a single-gate geometry. Fig. 2(a) shows the I_d–V_{ds} curves at $V_{\text{gs}} = 1.4$ V and $\Phi^s_{\text{SB}} = 0.5$ eV in the case of i) $\Phi^d_{\text{SB}} = 0.5$ eV (black), ii) $\Phi^d_{\text{SB}} = 0.4$ eV (blue), iii) $\Phi^d_{\text{SB}} = 0.3$ eV (red), iv) $\Phi^d_{\text{SB}} = 0.2$ eV (light blue), and v) $\Phi^d_{\text{SB}} = 0.0$ eV (green). Although the sub-linear behavior is slightly reduced with decreasing Φ^d_{SB}, it is clearly observed even though the Schottky barrier at the drain end vanishes in case v). The reason for the sub-linear behavior can be understood when looking at the conduction bands for different bias voltages as depicted in Fig. 2(c)[1]: Even in the case of $\Phi^d_{\text{SB}} = 0$ eV, the strong impact of V_{ds} on the potential distribution within the channel (provided via the channel charge) yields an increase of the tunneling through the source-side SB for increasing bias and hence a distinct sub-linear behavior.

Note that the quasi-Fermi level [the red dashed line in Fig. 2(c)] drops at the source side and hence is (almost) at the same level as the drain Fermi level. Hence, the sub-linear behavior in the present case is purely due to the source-side Schottky barrier. In contrast, the case where the Schottky barrier at the drain is higher than in the source is shown in Fig. 2(b). Here, a substantial portion of the applied bias drops across the drain Schottky barrier [see Fig. 2(d)], leading again to a sub-linear behavior. In this case, the sub-linearity is indeed due to a forward-biased Schottky diode at the drain, since $\Phi^s_{\text{SB}} < \Phi^d_{\text{SB}}$. However, an important observation regarding

[1]Exemplarily, we only consider the n-type branch of the SB-MOSFET. Note that although the simulations include electron and hole contributions, only the conduction band is displayed for clarity of the illustrations.

the role of the source- and drain-side Schottky diodes can be made when comparing Fig. 2(a) and (b): while the saturation current is constant in the case of varying Φ_{SB}^{d} [see Fig. 2(a)], it strongly increases with decreasing Φ_{SB}^{s} [cf. Fig. 2(b)]. This again shows that the source-side Schottky diode is decisive for the electrical behavior of SB-MOSFETs: current saturation of the output characteristics, whose magnitude is determined by Φ_{SB}^{s}, is obtained as soon as V_{ds} is large enough to suppress the drain's impact on the source-side Schottky diode.

While in the case $\Phi_{SB}^{s} < \Phi_{SB}^{d}$, it is clear that a forward-biased Schottky diode at drain leads to a sub-linear behavior, in a (regular) SB-MOSFET with equal Schottky barriers at the source and the drain, it is the impact of the channel charge on the source-side junction that plays the dominant role. This is underlined by simulations carried out for NW SB-MOSFETs with constant $\Phi_{SB}^{s} = \Phi_{SB}^{d} = 0.5$ eV but varying d_{ox} and d_{nw}. In order to keep the transmission probability through the SB unaffected when varying the device parameters,[2] d_{ox} and d_{nw} are changed leaving the screening length λ constant. To be specific, the following four devices are considered: 1) $d_{ox} = 20$ nm, $d_{nw} = 1$ nm; 2) $d_{ox} = 10$ nm, $d_{nw} = 2$ nm; 3) $d_{ox} = 5$ nm, $d_{nw} = 4$ nm; and 4) $d_{ox} = 2$ nm, $d_{nw} = 10$ nm. Since a single-gate device architecture is considered, $\lambda = ((\varepsilon_{nw}/\varepsilon_{ox})d_{ox}d_{nw})^{1/2} = 7.58$ nm in all cases. Furthermore, an increase in d_{nw} yields a reduced carrier density because purely 1-D electronic transport is considered with the charge carriers confined to the NW cross section (i.e., a particle-in-the-box approximation is used). As a result, the wave function spreads across the nanowire cross section, leading to a carrier density reduction (approximately according to $n(x) \propto n^{1D}(x)/d_{nw}^{2}$, where $n^{1D}(x)$ is the carrier density computed with NEGF) for increasing d_{nw} since contributions from higher subbands of the nanowire have deliberately not been taken into account. In addition, to carve out the impact of the channel charge more clearly, the effective mass is lowered from $m^{\star} = 0.2m_0$ to $m^{\star} = 0.05m_0$.[3]

Fig. 3 shows the output characteristics for different d_{nw} and d_{ox} mentioned above. Obviously, an increasing sub-linear behavior develops if d_{nw} decreases (and d_{ox} increases). The reason for this is the increasing charge carrier density with decreasing d_{nw}, leading to a stronger charge-mediated impact of the potential distribution of the source-side SB with larger V_{ds}. In contrast, the carrier density becomes rather small and the oxide capacitance large in case 4) and, therefore, substantially less impact of the charge on the potential distribution is obtained which can also be observed in the conduction band profiles plotted in the inset of Fig. 3.

To further elaborate on this, consider (1): far away from the source-channel and channel-drain interfaces, the second derivative term can be neglected in a long-channel device as assumed here. Hence, $-(\Phi_f - (\Phi_g + \Phi_{bi})) \approx -e^2\lambda^2/(\varepsilon_0\varepsilon_{nw}) \cdot (n^{1D}/d_{nw}^{2}) = -e^2 n^{1D}/(\varepsilon_0\varepsilon_{ox}) \cdot d_{ox}/d_{nw}$. While n^{1D} depends on the device geometry only via λ (which is constant for all four

[2]The transmission probability T through a Schottky barrier, either represented by an effective Schottky barrier [16] or computed with the Wentzel–Kramers–Brillouin (WKB) approximation, depends exponentially on λ.

[3]An increase of the effective bandgap due to carrier confinement is neglected.

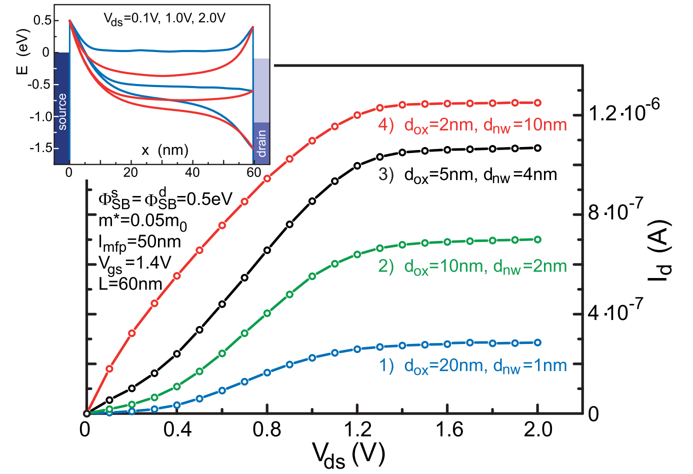

Fig. 3. Output characteristics for a fixed $V_{gs} = 1.4$ V of a nanowire SB-MOSFET (see the figure for the simulation parameters) with $\Phi_{SB}^{s} = \Phi_{SB}^{d} = 0.5$ eV and varying d_{nw} and d_{ox} resulting in the same λ. The inset shows the conduction band profiles in cases 1) and 4).

devices considered), the last factor d_{ox}/d_{nw} ranges between $20, \ldots, 0.2$ for the four SB-MOSFETs displayed in Fig. 3. In fact, in case 4), $d_{ox}/d_{nw} = 0.2$ is so small (or in other words, the carrier density n^{1D}/d_{nw}^{2} and d_{ox} have become so small) that the so-called quantum capacitance limit is reached [29], [30]. In this limit, the charge in the channel is irrelevant, and the potential is determined solely by $\Phi_g + \Phi_{bi}$. Consequently, linear output characteristics are obtained for device 4) due to a strongly suppressed impact of the charge on the source-side Schottky diode although a substantial SB at the drain end exists. Note that reaching the quantum capacitance limit is also the reason for the peculiar observation that device 4) shows substantially more current than 1) although the carrier density is reduced: the improved gate control (due to the reduced carrier density and increased oxide capacitance) results in a larger energetic window for carrier injection and thus more current (cf. inset in Fig. 3).

In the literature, there are examples of SB-MOSFETs that do not exhibit sub-linear output characteristics [11], [31]–[34]. From the discussion above, it is now clear that sub-linearity can be observed if substantial Schottky barriers (larger than $\sim 4 \times k_B T$) exist and if the device is not in the quantum capacitance limit. Furthermore, there is a third prerequisite: if the transmission probability through the source and the drain Schottky diodes is denoted with T_{SB}^{s+d} and if this is combined appropriately with the transmission probability through the channel $T_{ch} = l_{mfp}/(L + l_{mfp})$ (where l_{mfp} is the scattering mean free path), the overall transmission probability is given by $T_{tot} = (L/l_{mfp} + 1/T_{SB}^{s+d})^{-1}$ [35]. This means that in SB-MOSFETs with very long L and/or extremely small carrier mobility (i.e., l_{mfp}) such as pseudo-MOSFETs with L in the mm-range or some thin-film transistors, the Schottky barriers may become irrelevant and a sub-linear behavior is not observed. However, apart from these extreme cases (quantum capacitance limit, extremely long L and/or very low mobility), SB-MOSFETs exhibit sub-linear output characteristics due to the bias-modulated impact of the channel charge on the source Schottky diode.

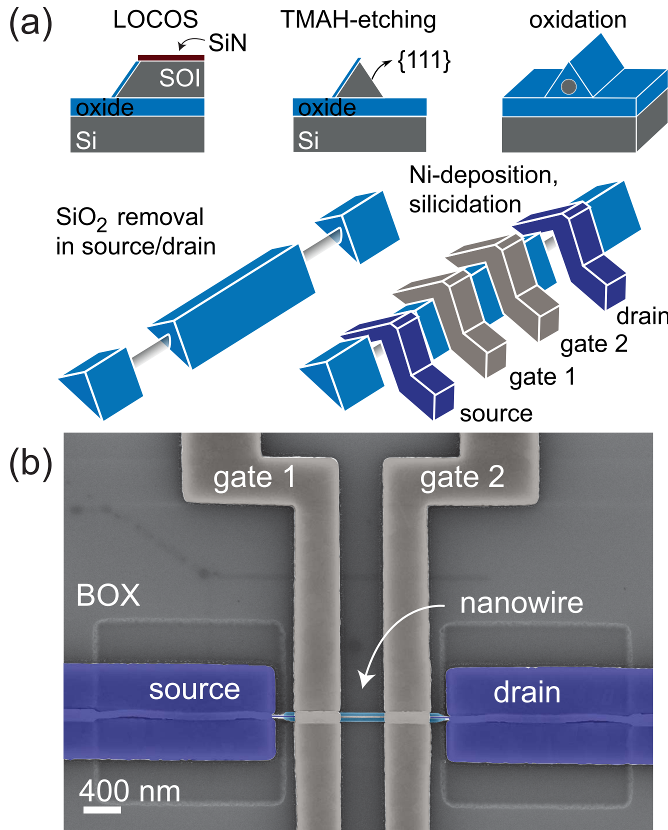

Fig. 4. (a) Schematic illustration of the fabrication process of dual-gate reconfigurable Si nanowire FETs. (b) Scanning electron micrograph of the fabricated device (d_{nw} = ~25 nm and d_{ox} > 15 nm) [15].

III. Dual-Gate Schottky-Barrier Transistors

The findings from the simulations clearly show that the sub-linear behavior of SB-MOSFETs is due to the charge-mediated impact on the source Schottky diode and not because of a forward-biased Schottky diode at the drain. In order to support these simulation results with experimental data, we fabricated dual-gate silicon nanowire transistors with nickel silicide source and drain contacts. The fabrication is schematically shown in Fig. 4(a): First, a silicon nitride mask is grown by thermal nitridation in an ammonia atmosphere. After patterning the nitride into a line-shaped structure, anisotropic silicon etching with tetramethylammonium hydroxide (TMAH) is carried out followed by local oxidation of silicon. Next, the nitride is removed selectively in hot phosphoric acid after a short SF_6/O_2 plasma treatment. Subsequently, a second TMAH etching step is carried out to obtain triangular-shaped silicon nanowires [36]. Afterward, the gate oxide is grown thermally in oxygen ambient at 1100 °C for 180 s, leading to a nanowire with reduced cross-sectional size and minimized degradation of the Si-SiO_2 interface due to roughness induced by the oxidation process [37]. Finally, the oxide is removed in the source/drain areas, four nickel leads are deposited, and a silicidation in a rapid thermal annealer in forming gas atmosphere at 450 °C for 300 s is carried out. During the silicidation, the nickel silicide encroaches into the NW, ensuring that there is no gate underlap between the

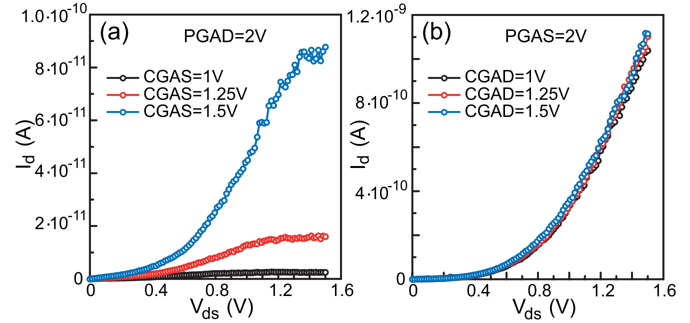

Fig. 5. Output characteristics in (a) program-gate at the drain (PGAD) operation mode and (b) PGAS operation mode for three different control-gate voltages.

source/drain contacts. The remaining two nickel leads serve as gate 1 and 2 (see Fig. 4) [15].

The dual-gate NW MOSFET can be operated in two different modes and thus allows creating the two different device configurations studied above: At first, gate 1 is used to control the current flow through the device and simultaneously a constant voltage larger than the maximum V_{gs} at gate 1 is applied at gate 2 (at the drain end of the device). Since the control gate (i.e., gate 1) is at the source and the so-called program gate (i.e., gate 2) is at the drain, this mode is denoted as "program-gate at drain" (PGAD) or alternatively "control-gate at source" (CGAS). In the second operation mode, the program gate is at the source and the control gate is at the drain (i.e., PGAS or CGAD). Note that the fringing fields of both gate electrodes modulate charge carrier concentration of the uncovered silicon channel (p-type, 10^{15} cm^{-3}) between the two gate electrodes and hence allow proper operation of the device.

In the PGAD mode, the voltage at gate 2 ensures that the drain SB is made rather thin, thereby increasing the tunneling probability through it (as if the original SB was lowered). Since the program voltage is larger than the control gate voltage, the portion of the channel underneath the program gate is (almost) in equilibrium with the drain contact. Therefore, this way of operating the device is equivalent to the case with a lower SB at the drain interface discussed above [cf. Fig. 2(a) and (c)]. On the other hand, if a large and constant voltage is applied to gate 1 (PGAS/CGAD), while gate 2 is used as the control gate, the SB is made transparent at the source. In this case, the first portion of the channel underneath the program gate is (almost) in equilibrium with the source electrode which is similar to Fig. 2(b) and (d) with $\Phi^s_{SB} < \Phi^d_{SB}$.

Fig. 5 shows the output characteristics in the PGAD (a) and PGAS (b) operation modes for three different control gate voltages. The characteristics in (b) exhibit a strong sub-linear behavior with increasing V_{ds} which is due to the forward-biased Schottky diode at the drain [cf. Fig. 2(d)]. In contrast, (a) resembles the I_d–V_{ds} curves of an SB-MOSFET with a distinct sub-linear behavior for small bias in spite of the substantially more transparent SB at the drain (because of applying a program gate voltage larger than the maximum control voltage). This reflects the discussion above [see Fig. 2(c)] and shows that the sub-linear behavior of SB-MOSFETs is

due to an increased tunneling through the source-side SB with increasing V_{ds}.

IV. Conclusion

In conclusion, it was shown that the sub-linear increase in the drain current as a function of V_{ds} is due to the impact of the charge in the channel on the carrier injection through the source-side SB: When V_{ds} is increased, the charge in the channel is strongly reduced from the equilibrium value to a value proportional to the transmission probability through the source Schottky barrier. In turn, the reduced charge yields an increased gate impact and hence larger carrier injection from the source. This results in the typical sub-linear output characteristics of SB-MOSFETs even if the drain Schottky barrier is very small. Our findings are confirmed with the measurements of dual-gate silicon NW SB-MOSFETs.

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