Foreword
Special Issue on Spintronics-Devices and Circuits

IT IS our great pleasure to introduce this Special Issue on Spintronics-Devices and Circuits to the IEEE TRANSACTIONS ON ELECTRON DEVICES readership. This issue features research that addresses the important and timely topics related to spintronic devices, circuits, and new architectures for low power applications. Spintronics is one of the emerging fields for the next-generation nano-electronic devices that offer solutions for memory and energy-efficient circuits and systems for data-intensive processing applications. Recent advances have expanded this technology to the entire microelectronics community in the domains of sensors, memories, oscillators, quantum information, processors, and computer architecture. These advancements in spintronics have shown great promise for stochastic and neuromorphic computing, in-memory computing, and data security applications. However, these applications are constrained by the challenges related to low spin efficiency, device reliability, high power consumption, low processing speed, and large area overhead. This Special Issue has been organized to bring together researchers and experts to address these technological challenges.

The call for papers of this Special Issue on Spintronics-Devices and Circuits was published in February 2021. Reviews for this Special Issue were organized by Guest Editors from the United States, India, France, China, and Singapore. A total of 54 submissions were received, out of which 17 articles were accepted after a rigorous reviewing process. Each of these accepted articles addresses one or more challenges with innovative solutions.

The first part of this Special Issue, containing five papers, is focused on spintronic devices optimized for improved electronic and magnetic properties. In the first article [A1], Frost *et al*. demonstrated that a bcc tungsten seed layer along with non-magnetic overlayers such as Ag and Ta can be used to promote the (110) surface to crystallize a Co-based Heusler-alloy film in a layer-by-layer mode at low energy and to induce perpendicular magnetic anisotropy. The corresponding devices are fabricated and characterized at room temperature. In the second article [A2], Mishra *et al.* used Mn-doped $MoSe_2$ monolayer with and without gas adsorption to tailor the electronic and magnetic properties of the $MoSe_2$ monolayer. Furthermore, Curie temperature and magnetic exchange coupling are calculated to indicate the robust ferromagnetism in both doped and adsorbed Mn-$MoSe_2$ monolayer. In the next article [A3], Fu *et al*. explored the influence of out-of-plane spin polarization for the realization of efficient spin-orbit-torque-based memory and oscillators. In the fourth article [A4], Wang *et al*. used a method based on the magnetoelectric effect present in multiferroic heterostructures to design a reconfigurable waveguide channel for spin-wave transmission. A phase shifter is designed to build an interferometer to fulfill the destruct and construct logic functions based on strain-controlled spin waves. In the last article [A5], Misba *et al*. proposed energy-efficient voltage-induced strain control of a domain wall in a perpendicularly magnetized nanoscale racetrack on a piezoelectric substrate. It can implement a stochastic multistate synapse to be utilized in neuromorphic computing platforms. Such a strain-controlled synapse has an energy consumption of $\sim$1 fJ and could thus be very attractive to implement energy-efficient quantized neural networks.

The second part of this Special Issue, containing six articles, is focused on energy-efficient, high-speed, and reliable spintronic-based circuits. In the first article [A6], Cho *et al.* designed a nonvolatile flip-flop utilizing valley–spin Hall effect in monolayer tungsten. It achieves 74%–75% lower backup energy and 55%–59% lower restore energy than the existing flip flops based on the giant spin Hall effect. In the second article [A7], Liu *et al.* proposed a novel nonvolatile look-up-table design based on a voltage-controlled spin-orbit torque device, which utilizes the symmetrical structure of a spintronic memory cell and a separated CMOS select tree to enhance the operating speed and read reliability and to reduce power consumption. In the third article [A8], Barla *et al.* proposed an auto-write-stopping circuit to achieve energy-efficient implementation of hybrid MTJ/CMOS arithmetic logic circuits based on logic-in-memory architecture. The proposed full adder and arithmetic logic unit are better than the conventional designs in terms of power dissipation, output response, and the number of devices. In [A9], Ghanatian *et al.* presented a 3-bit flash spin-orbit torque analog-to-digital converter (ADC), which is based on switching of a perpendicular-anisotropy magnetic tunnel junction by the spin Hall effect assisted by spin-transfer torque. The design eliminates the need for current mirror circuits that are used in current-mode flash CMOS ADCs. The power consumption and the maximum

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sampling rate are estimated as 416 μW and 102 MS/s, respectively. In the next article [A10], Yang *et al.* proposed a novel in-memory computing platform based on hybrid spintronic/CMOS memory to perform efficient logic and arithmetic operations. One-bit full adder and ripple carry adder are implemented by utilizing the enhanced peripheral circuitry embedded in the memory without adding any processing unit. The performance of write operations is significantly improved by exploiting the toggle spin-torque mechanism. The resistance margin of the proposed design is two times greater than the previous schemes. In the last article [A11] of this part, Tang *et al.* designed a skyrmion-magnetic domain interconversion logic gate and studied the effects of elevated temperatures and structural defects on speed and stability using various geometrical and magnetic parameters. Although the elevated temperatures significantly disrupt the skyrmion stability, it helps with the depinning of magnetic domains in the presence of structural defects to improve the propagation process.

The third and final part of this Special Issue, containing six articles, is focused on the implementation of efficient architectures using spintronic devices for system-level applications. In the first article [A12], Sahu *et al.* proposed a ferrimagnetic domain-wall synapse device as an alternative to its ferromagnetic counterpart for faster and more energy-efficient on-chip learning on a crossbar-array-based analog-hardware fully connected neural network. The ferrimagnetic-domain-wall velocity is about 2–2.5 times higher than the ferromagnetic-domain wall velocity in a CoFe/Pt device at room temperature. As a consequence, the total energy consumption and the time required for on-chip learning are significantly improved. In the next article [A13], Cai *et al*. proposed a device and circuit interaction approach for spintronic-based binary neural network (BNN) realization for MNIST handwritten digit recognition. A 4T-2M bit-cell is developed from commodity spintronic bit-cell to achieve one-step convolution, as well as XNOR and accumulation (XAC) operations. The recognition latency of one-step convolution is improved by 21% than that of XAC convolution, whereas the energy consumption of XAC is 30% lower than the one-step operations. In [A14], Liu *et al*. evaluated a neural spin-orbit torque-based lookup table (NSOT-LUT) approach for artificial neural networks within an island-style reconfigurable fabric and then optimized for energy-sparing operation, throughput, and routability. The NSOT-LUT fabric achieves approximately six-fold area savings, two-fold speedup, and two-fold power savings for a set of 12 benchmark circuits when compared to an island-style baseline FPGA using spintronic configuration memory. In [A15], Nisar *et al*. proposed an advanced encryption standard (AES) system within in-memory computing architecture using a voltage-controlled spin-orbit-torque (SOT) device. The entire encryption process is performed within the high-density spintronic-based memory array to achieve low power and high processing speed. In [A16], Nikam *et al.* presented an approach for resource-intensive core computations of the long short-term memory (LSTM) network *in-situ* on a passive resistive random-access memory (RRAM) crossbar array for realizing compact and ultralow-power recurrent neural network engines for mobile Internet-of-Things (IoT) devices. The passive LSTM-based array implementation outperforms the prior digital and active 1T-1R RRAM designs by several orders of magnitude in terms of area and energy consumption during the training. In [A17], Fu *et al*. proposed level scaling and pulse regulating methods that are simple, feasible, and universal to effectively mitigate the impact of cycle-to-cycle variations for TiO_2/TiO_{2-x} memristor-based edge AI systems.

The Special Issue was attractive and competitive enough since it received a large number of submissions with an acceptance of around 31%. The objectives of the Special Issue were fulfilled in terms of advancing novel and emerging techniques for addressing challenging problems in spintronic devices, circuits and systems. We sincerely thank the reviewers and appreciate their efforts for timely reviews. We also thank all the authors for submitting their research in this Special Issue. We hope that you will enjoy reading these novel contributions.

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APPENDIX: RELATED ARTICLES

[A1] W. Frost, M. Samiepour, and A. Hirohata, "Perpendicular anisotropy controlled by seed and capping layers of Heusler-alloy films," *IEEE Trans. Electron Devices*, early access, Sep. 6, 2021, doi: 10.1109/TED.2021.3105490.

[A2] N. Mishra, B. P. Pandey, B. Kumar, and S. Kumar, "Enhanced electronic and magnetic properties of N_2O gas adsorbed Mn-doped $MoSe_2$ monolayer," *IEEE Trans. Electron Devices*, early access, Oct. 18, 2021, doi: 10.1109/TED.2021.3116929.

[A3] Z. Fu *et al.*, "Optimal spin polarization for spin-orbit-torque memory and oscillator," *IEEE Trans. Electron Devices*, early access, Jan. 10, 2022, doi: 10.1109/TED.2021.3137764.

[A4] F. Wang *et al.*, "Design of reconfigurable spin-wave nanochannels based on strain-mediated multiferroic heterostructures and logic device applications," *IEEE Trans. Electron Devices*, early access, Dec. 23, 2021, doi: 10.1109/TED.2021.3135486.

[A5] W. Al Misba, T. Kaisar, D. Bhattacharya, and J. Atulasimha, "Voltage-controlled energy-efficient domain wall synapses with stochastic distribution of quantized weights in the presence of thermal noise and edge roughness," *IEEE Trans. Electron Devices*, early access, Sep. 23, 2021, doi: 10.1109/TED.2021.3111846.

[A6] K. Cho, S. K. Thirumala, X. Liu, N. Thakuria, Z. Chen, and S. K. Gupta, "Utilizing valley-spin Hall effect in WSe_2 for low power non-volatile flip-flop design," *IEEE Trans. Electron Devices*, early access, Dec. 29, 2021, doi: 10.1109/TED.2022.3135475.

[A7] X. Liu, E. Deng, H. Zhang, Y. Zhang, B. Pan, and W. Kang, "Novel nonvolatile lookup table design based on voltage-controlled spin orbit torque memory," *IEEE Trans. Electron Devices*, early access, Jan. 28, 2022, doi: 10.1109/TED.2022.3143071.

[A8] P. Barla, V. K. Joshi, and S. Bhat, "A novel auto-write-stopping circuit for SHE + STT-MTJ/CMOS hybrid ALU," *IEEE Trans. Electron Devices*, early access, Feb. 4, 2022, doi: 10.1109/TED.2022.3145331.

[A9] H. Ghanatian, H. Farkhani, Y. Rezaeiyan, T. Böhnert, R. Ferreira, and F. Moradi, "A 3-bit flash spin-orbit torque (SOT)-analog-to-digital converter (ADC)," *IEEE Trans. Electron Devices*, early access, Jan. 26, 2022, doi: 10.1109/TED.2022.3142649.

[A10] Z. Yang *et al.*, "A novel computing-in-memory platform based on hybrid spintronic/CMOS memory," *IEEE Trans. Electron Devices*, early access, Jan. 4, 2022, doi: 10.1109/TED.2021.3137761.

[A11] C. Tang *et al.*, "Effects of temperature and structural geometries on a skyrmion logic gate," *IEEE Trans. Electron Devices*, early access, Dec. 10, 2021, doi: 10.1109/TED.2021.3130217.

[A12] U. Sahu, N. Sisodia, P. K. Muduli, and D. Bhowmik, "Ferrimagnetic synapse devices for fast and energy-efficient on-chip learning on crossbar-array-based neural networks (a device-circuit-system costudy)," *IEEE Trans. Electron Devices*, early access, Feb. 9, 2022, doi: 10.1109/TED.2022.3142119.

[A13] H. Cai, Z. Bian, Z. Fan, B. Liu, and L. Naviner, "Commodity bit-cell sponsored MRAM interaction design for binary neural network," *IEEE Trans. Electron Devices*, early access, Dec. 27, 2021, doi: 10.1109/TED.2021.3134588.

[A14] M. Liu, P. Borulkar, M. Hossain, R. F. DeMara, and Y. Bai, "Spin-orbit torque neuromorphic fabrics for low-leakage reconfigurable in-memory computation," *IEEE Trans. Electron Devices*, early access, Jan. 20, 2022, doi: 10.1109/TED.2021.3140040.

[A15] A. Nisar, S. Dhull, S. Shreya, and B. K. Kaushik, "Energy-efficient advanced data encryption system using spin-based computing-in-memory architecture," *IEEE Trans. Electron Devices*, early access, Mar. 3, 2022, doi: 10.1109/TED.2022.3150623.

[A16] H. Nikam, S. Satyam, and S. Sahay, "Long short-term memory implementation exploiting passive RRAM crossbar array," *IEEE Trans. Electron Devices*, early access, Dec. 15, 2021, doi: 10.1109/TED.2021.3133197.

[A17] J. Fu, Z. Liao, and J. Wang, "Level scaling and pulse regulating to mitigate the impact of the cycle-to-cycle variation in memristor-based edge AI system," *IEEE Trans. Electron Devices*, early access, Feb. 10, 2022, doi: 10.1109/TED.2022.3146801.

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Prof. Bandyopadhyay won many awards including Virginia's Outstanding Scientist (2016), the State Council of Higher Education for Virginia Outstanding Faculty Award (2018), the University Award of Excellence (2017), his department's Lifetime Achievement Award (2015), and his university's Distinguished Scholarship Award (2012). His prior employer, the University of Nebraska–Lincoln, gave him the College of Engineering Research Award (1998), Service Award (2001), and Interdisciplinary Research Award (2001). In 2020, he received the "Pioneer in Nanotechnology" Award from the IEEE. He is the Founding Chair of the IEEE Nanotechnology Council Technical Committee on Spintronics. He served as a Jefferson Science Fellow of the U.S. National Academies of Science, Engineering, and Medicine during the 2020–2021 term and was an adviser to the USAID Bureau for Europe and Eurasia, Division of Energy and Infrastructure. He is a fellow of the American Physical Society (APS), the Institute of Physics (IoP), the Electrochemical Society (ECS), and the American Association for the Advancement of Science (AAAS).

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Bernard Dieny played a key role in the pioneering work on giant magnetoresistance spin-valves which were introduced in hard disk drives in 1998. In 2001, he launched SPINTEC Laboratory (Spintronics and Technology of Components) in Grenoble, France. He co-founded two startup companies: Crocus Technology on MRAM and magnetic sensors in 2006 and EVADERIS on circuits design in 2014. His field of expertise covers a broad spectrum from basic research in nanomagnetism and spin-electronics to functional spintronic devices. He has been conducting research on magnetism and spin electronics for 35 years.

He received two Advanced Research Grants from the European Research Council in 2009 and 2014 related to hybrid CMOS/magnetic integrated electronics. He was nominated IEEE Fellow in 2010, received the De Magny Prize from the French Academy of Sciences in 2015, and the IEEE Magnetics Society Achievement Award in 2019.

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Dr. Piramanayagam serves as a Managing Editor for *Nano*, an Editor for IEEE TRANSACTIONS ON MAGNETICS, an Editorial Board Member for *Scientific Reports* (Nature Publishing Group) and *Physica Status Solidi-RRL*. He has served as the Chair for IEEE Magnetics Society Technical Committee, and he is an elected member of the AdCom of IEEE Magnetics Society.

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