

Optimization of 1700-V 4H-SiC Semi-Superjunction Schottky Rectifiers With Implanted P-Pillars for Practical Realization

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Abstract—A class of vertical 1700 V 4H-silicon carbide (SiC) semi-superjunction (SJ) Schottky diodes have been simulated and optimized to ensure practical and costeffective realization. The proposed structures could be realized using an n-type drift region of 9- μ m and etching trenches partway through this region to form the required mesa regions. P-pillars are then created through implantation into both the trench sidewalls and trench bottom. This semi-SJ topology overcomes problems with conventional SJs that span the full drift region (full-SJs), namely a narrow charge-balance window required to achieve the maximum $V_{\rm BD}$, and hard, snappy, switching characteristics. The optimized SiC semi-SJ comprises a 7- μ m SJ region above 2- μ m of conventional drift region. An angled trench sidewall (α), 10° off vertical, introduces a graded charge profile throughout the n-pillar, which widens the implantation window by 34%, while maintaining a $V_{\rm BD}$ of ~2.1 kV and a $R_{\rm ON,SP}$ comparable to a vertical full-SJ. Further advantages of the proposed semi-SJ, over a full-SJ, include a reduced trench aspect ratio and two orders of magnitude lower leakage current. Furthermore, the graded charge profile in the n-pillar gradually depletes the drift region, suppressing ringing and reducing the peak reverse recovery current by 50%.

Index Terms—Device simulation, Schottky diode, semisuperjunction (SJ), silicon carbide (SiC), SJ.

I. Introduction

SILICON carbide (SiC) has demonstrated its potential to reduce the specific ON-resistance ($R_{\rm ON,SP}$) of power devices [1]. With a critical field ten times greater than silicon (Si), fast switching, high voltage, unipolar SiC devices

Manuscript received December 22, 2021; revised January 28, 2022; accepted February 14, 2022. Date of publication March 7, 2022; date of current version March 28, 2022. This work was supported by the Engineering and Physical Science Research Council (EPSRC) under Grant EP/R00448X/1. The review of this article was arranged by Editor F. Udrea. (Corresponding author: G. W. C. Baker.)

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2022.3152460.

Digital Object Identifier 10.1109/TED.2022.3152460

threaten to replace Si p-i-n diodes and insulated gate bipolar transistors (IGBTs) within the 600–1700 V class. However, as the desired blocking voltage is scaled up, the $R_{\rm ON,SP}$ follows the relationship, $R_{\rm ON,SP} \propto V_{\rm BD}^{2.5}$ [2], and thus use of SiC unipolar devices at higher voltages is not feasible. It is therefore necessary to employ techniques to further reduce this relationship and the associated on-state losses in unipolar devices at higher voltages.

In Si, superjunction (SJ) devices have demonstrated a partial linearization of the relationship between the $R_{\rm ON,SP}$ and blocking voltage ($R_{\rm ON,SP} \propto V_{\rm BD}^{1.32}$ [3]). This reduces the $R_{\rm ON,SP}$ of structures to below the unipolar limit of the material, whilst also maintaining the fast switching speed of a unipolar devices [4]. However, SJ structures have two major drawbacks: first, the complexity of fabrication, and second, the "hardness" of the switching characteristics [5]. These drawbacks are magnified when employing SJ technology in SiC devices, as many of the traditional SJ fabrication techniques used in Si processes are not yet fully established in SiC [6], and more investigations regarding the dynamic performance of SiC SJs are required.

There have been several experimental reports demonstrating SiC SJ Schottky barrier diodes (SBDs) [7], [8] fabricated via a trench-etch and sidewall implantation. This fabrication approach has been further utilized to demonstrate a SiC SJ JFET [9]. There have also been several experimental demonstrations of SiC SJ MOSFETs [10]–[12] fabricated via multiepitaxial growth and p-type implantation, and also one demonstration of trench-etching and epitaxial regrowth [13]. The experimental demonstrations of the aforementioned SiC SJ structures have shown promising results with recent works [12], [13] pushing the $R_{\rm ON,SP}$ below the SiC unipolar limit. However, these fabrication techniques require both complex and expensive process flows.

Previously, we proposed a SiC full-SJ structure [14], [15], which was optimized via TCAD simulation to block 2 kV, with an $R_{\rm ON,SP}$ below the unipolar limit. Realizable via a trench-etch and sidewall implantation, its relatively simple fabrication removes the need for epitaxial regrowth. The structure was designed with a tapered sidewall (10° off vertical), which introduces a graded charge profile throughout the n-pillar—improving the device's switching characteristics, and its tolerance of charge imbalance, making fabrication easier.

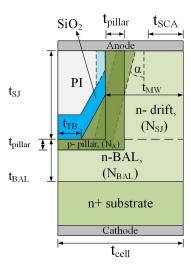


Fig. 1. Schematic cross section (half-cell) of the SiC semi-SJ SBD with key dimensions and parameters.

TABLE I
KEY DIMENSIONS AND PARAMETERS OF
PROPOSED SEMI-SJ STRUCTURE

Symbol	Definition	Value	Units
t _{MW}	Mesa width	2.1	μm
$t_{ m BAL}$	Thickness of bottom assist layer	1.0-8.0	
t_{cell}	Cell pitch	4.2	
$\mathbf{t}_{\mathrm{drift}}$	Thickness of drift region	9.0	
$\mathbf{t}_{\mathrm{pillar}}$	Thickness of p-pillar	0.2	
t_{SCA}	Min. width of Schottky contact	1.0	
$t_{\rm SJ}$	Thickness of superjunction region	1.0-8.0	
t_{TB}	Min. width of trench bottom	0.5	
N_A	P-pillar doping	$3.0 - 4.5 \times 10^{17}$	cm ⁻³
N_{BAL}	Bottom assist layer doping	$0.35 - 2.5 \times 10^{16}$	
N_{SJ}	Doping of SJ drift region	3.5×10^{16}	
α	Sidewall angle	0, 10	0

In this article, a semi-SJ is proposed to further suppress some of the drawbacks of SJ structures [5]. The proposed structure maintains a $V_{\rm BD} > 2$ kV, but with a reduced aspect ratio ($A_{\rm SJ}$, the ratio of pillar depth to width) and a greater tolerance to charge imbalance. Additionally, the proposed semi–SJ realizes a similar $R_{\rm ON,SP}$ to the vertical full-SJ and soft reverse recovery characteristics. The design and optimization of this structure will be discussed in detail throughout this study.

II. DEVICE DESIGN AND SIMULATION

The semi-SJ test-cell can be seen in Fig. 1 with key dimensions in Table I. It is proposed that the semi-SJ would be fabricated via trench etching and sidewall implantation.

The test cell is built on a 4H-SiC substrate, which has a doping concentration of $1.0 \times 10^{19}~\rm cm^{-3}$ and a thickness of $100~\mu m$ —as if it had been thinned postprocessing. The drift region has a total thickness ($t_{\rm drift}$) of $9.0~\mu m$ and is designed to support a blocking voltage $>2~\rm kV$. The semi-SJ

drift region is comprised of both a SJ-region and a conventional non-SJ region situated beneath the SJ-region, which is known as a bottom assist layer (BAL). The SJ-region has a variable depth (t_{SJ}) and a fixed doping concentration (N_{SJ}) of $3.5 \times 10^{16} \text{ cm}^{-3}$. The n-BAL has thickness (t_{BAL}) and doping concentration (N_{BAL}), both of which are varied throughout this study. The half-cell mesa width (t_{MW}) is 2.1 μ m. The trench sidewall angle (α) is initially pivoted about the center of the SJ-region to keep the dose of each pillar balanced. Later, the pivot-point of α is pushed deeper into the structure to further optimize the design. The trench sidewall angle is fixed at either 0° or 10° , with p-pillar doping concentrations ($N_{\rm A}$) optimized to between 3.25 and 4.50×10^{17} cm⁻³. The p-pillar is formed via a tilted implantation into the trench sidewall and a vertical implantation into the bottom of the trench, with a depth (t_{pillar}) of 200 nm. The implantation would use aluminum (Al) ions and is assumed to have a box profile. The trenches are formed via inductively coupled plasma reactive ion etching (ICP-RIE). The trench sidewalls are passivated with SiO_2 , then the trench is filled with polyimide (PI). Metal contacts would then be formed on the top and bottom of the device. The work function of the top-side (Schottky) contact is 5.2 eV, similar to that of Ni. The half-cell pitch (t_{cell}) is fixed at 4.2 μ m for all devices to ensure comparable current densities.

The semi-SJ is simulated at room temperature using the "Sentaurus" module from the TCAD package Synopsys. The models used have been benchmarked to both the experimental and simulation work performed by Zhong *et al.* [7]. Further details are described in our previous work [15]. The effects of both nonlocal tunneling current and barrier-lowering due to image force have been considered for the Schottky contact [16], in both the forward and reverse state. Furthermore, it should be noted that more realistic Al-implanted properties have been used in this simulation [17].

III. RESULTS AND DISCUSSION

A. Determination of t_{BAL}-Ratio in Semi-SJs

Semi-SJ structures offer device designers the opportunity to increase the $V_{\rm BD}$ while reducing the processing complexity compared to full-SJs [5]. However, the $V_{\rm BD}$ of the semi-SJs can only be improved by appropriate design of the n-BAL, as the blocking voltage is the sum of the voltage sustained by the SJ region and by that of the n-BAL. Thus, the BAL is a critical design point for all semi-SJ structures as it influences both the electric field and carrier distributions within the device. A series of simulations were performed, varying both $N_{\rm BAL}$ and t_{BAL} , in order to identity n-BAL designs that achieve a $V_{\rm BD} = 2.1$ kV. The results of this study can be seen in Fig. 2 which reveals the impact on the $R_{ON,SP}$ of both the t_{BAL} -ratio $[(t_{\rm BAL}/t_{\rm drift})^*100)]$ and $N_{\rm BAL}$, with each iteration maintaining a $V_{\rm BD} = 2.1$ kV. In this figure a $t_{\rm BAL}$ -ratio = 0% translates to a full-SJ and a $t_{\rm BAL}$ -ratio = 100% would be a planar SBD without any trench. Hereafter, the N_A was swept for varying t_{BAL} -ratios and N_{BAL} concentrations to find structures that minimized the $R_{ON,SP}$ whilst maintaining the desired V_{BD} . As can be seen in Fig. 2 it is necessary for the t_{BAL} -ratio to be less than 40% to achieve a $R_{ON,SP}$ below the unipolar

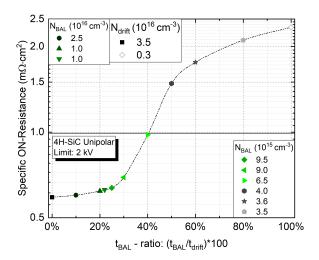


Fig. 2. Relationship between t_{BAL} -ratio and $R_{ON,SP}$.

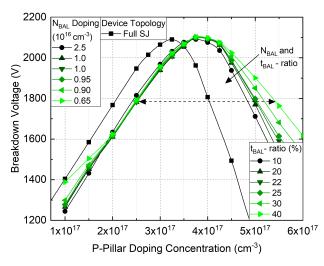


Fig. 3. Effect of $t_{\rm BAL}$ -ratio on the charge balance against $V_{\rm BD}$ in semi-SJ structures.

limit of the material. Additionally, the reduction of the $R_{\rm on,SP}$ for structures with a $t_{\rm BAL}$ -ratio < 25% becomes marginal. In turn, the implantation window was analyzed for structures with a $t_{\rm BAL}$ -ratio < 40%, as shown in Fig. 3. As one would expect, the implantation window (defined as the full width at 85% of the peak $V_{\rm BD}$) increases with as $t_{\rm BAL}$ increases, a result of the electric field modulation principle [18]. As the $t_{\rm BAL}$ -ratio is increased from 10% to 40% the implantation window increases from 22% to 45%, respectively, relative to the full-SJ. The structure with a $t_{\rm BAL}$ -ratio = 22% was selected to be studied hereafter, as the structure achieves a good balance between $R_{\rm ON,SP}$ and relative implantation window improvements measured at 25%.

B. Impact of $\alpha = 10^{\circ}$ on Semi-SJs

The effects of the tilted sidewall angle (α) on the implantation window were then investigated in regard to the semi-SJ structure with a $t_{\rm BAL}$ -ratio = 22%, the results of which can be seen in Fig. 4, benchmarked to the full-SJ. Fig. 4 demonstrates that the introduction of a 10° sidewall angle,

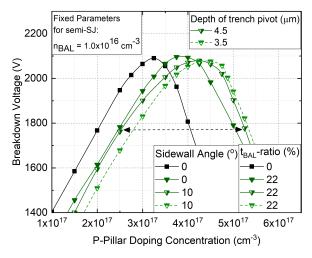


Fig. 4. Effect of α on the charge balance against $V_{\rm BD}$ in semi-SJ structures.

pivoted about the midpoint of the SJ-region at a depth of 3.5 μ m, means that the peak $V_{\rm BD}$ occurs at a greater p-pillar doping density (increased p-type charge Q_P). Unlike in the full-SJ [15], the introduction of the angled sidewall pivoted about the mesa midpoint (3.5 μ m; so conserving charge balance) does not improve the implantation window. This is because the mechanism that results in the increased tolerance to charge imbalance is dominated by the semi-SJ geometry and not the graded charge profile. It was, therefore, decided to implement a more aggressive graded charge profile in the structure by pushing the pivot-point of α deeper into the device to a depth of 4.5 μ m. As the pivot-point of α is pushed deeper into the structure, a greater proportion of the Schottky contact is consumed. By selecting a pivot-point depth of 4.5 μ m, a 1.0-μm Schottky contact width could be maintained. As can be seen in Fig. 4. pivoting α at a depth of 4.5 μ m increased the implantation window by 9% relative to the vertical semi-SJ with an equivalent t_{BAL} -ratio and by 34% relative to the 0° full-SJ, all without compromising the $V_{\rm BD}$. It was decided to take this structure forward throughout the rest of the study.

The widening of the implantation window is the combined results of both the tilted sidewall angle, which introduces a graded charge profile throughout the n-pillar of the device and also the n-BAL. This can be better understood by analyzing the distribution of charge throughout the SJ region and also the electric field throughout the structure.

Charge balance is achieved in a SJ when the charge located within the n- and p-pillars are perfectly compensated $(Q_n = Q_p)$, where the respective Q_n and Q_p values are defined as (pillar width \times pillar doping). As the pillars of a vertical full-SJ mutually deplete, a flat electric field distribution maximizes V_{BD} , as seen in Fig. 5 for the $\alpha = 0^{\circ}$ full-SJ (as previously studied [15]). The introduction of a sidewall angle $\alpha > 0^{\circ}$ into a full-SJ tapers the amount of n-type charge in the mesa, effectively introducing a graded charge profile throughout the drift region. Fully compensated charge balance only then occurs at the pivot point. Above the pivot point a $Q_n < Q_p$ condition is seen and the n-drift is, effectively, under-doped. Conversely, below the pivot point

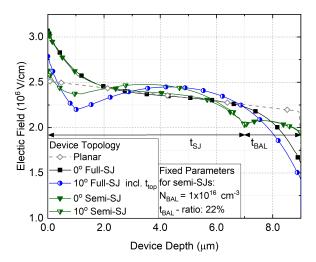


Fig. 5. Electric field distribution at the onset of $V_{\rm BD}$ through the center of the *n*-drift region in the proposed semi- and full-SJs when charge balance is achieved, compared to a planar SBD optimized to 2.1 kV.

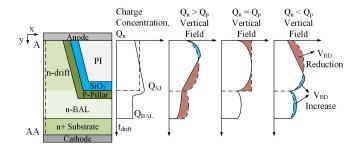


Fig. 6. Electric field distribution along A–AA of a semi-SJ in the presence of charge imbalance in a structure with a graded charge profile.

a $Q_{\rm n}>Q_{\rm p}$ condition is seen meaning that the n-drift is effectively over-doped. The introduction of $\alpha>0^{\circ}$ about the mesa midpoint, therefore, causes a symmetrical deviation from the rectangular electric field distribution causing a reduction of $V_{\rm BD}$. To rebalance the full-SJ [15], a high-doped surface region, named $t_{\rm top}$, helps to rebalance the top of the mesa structure and recover the $V_{\rm BD}$ and $R_{\rm on,SP}$ lost as a result of the $\alpha>0^{\circ}$ sidewall inducing local charge imbalance and pinching off the depletion region at the surface.

The electric field profile of the optimized vertical and $\alpha = 10^{\circ}$ semi-SJ devices are shown in Fig. 5. In contrast to the full-SJ devices, the total $V_{\rm BD}$ includes the voltage sustained across the n-BAL as well as the mesa SJ-region. The impact of the graded charge profile throughout the n-pillar is further illustrated in Fig.6, which considers the electric field distribution at the center of the drift region (x = 0) for a semi-SJ structure with a sidewall angle, $\alpha > 0^{\circ}$. When α is pivoted about the midpoint of the SJ region, despite the total area of both pillars being equal, the tilted geometry causes local charge imbalance at both the top and bottom of the SJ pillars. Thus, under the ideal charge balanced conditions, illustrated in the $Q_{\rm n}=Q_{\rm p}$ example, the graded charge profile is responsible for the deviation from the ideal, $\alpha = 0^{\circ}$ rectangular electric field, and thus a lower $V_{\rm BD}$ results [19]. It should be noted, that pivoting α at a depth of 4.5 μ m, below the midpoint of the mesa-region, results in the total charge of the n-pillar being \sim 5% lower than that of the charge balanced condition.

As charge imbalance is introduced via the under- or overdoping of the p-pillar, the voltage supported is lowered further, however, unlike the full-SJ, charge imbalance in the tilted semi-SJ is asymmetrical. Where $Q_n > Q_p$, a significant reduction in $V_{\rm BD}$ occurs due to the reduction of the electric field at the n-drift/n-BAL interface, pictured in red, which further leads to a reduction in the electric field supported within the n-BAL. The blue shaded areas are where the field is enhanced due to the imbalance, and voltage is recovered. As in the full-SJ case, this occurs at the top of the mesa in the $Q_n > Q_p$ case. Conversely, under conditions where $Q_{\rm n} < Q_{\rm p}$, the reduction in $V_{\rm BD}$ is less pronounced as the charge imbalance reduces the field only at the top of the SJ region. At the n-drift/n-BAL interface and throughout the n-BAL, the electric field remains at its peak and can be marginally increased, hence, the peak $V_{\rm BD}$ for the $\alpha = 10^{\circ}$ structure occurring at a higher $N_{\rm A}$ value than the vertical $\alpha = 0^{\circ}$ structure. Therefore, high $Q_{\rm n}$ conditions reduce the $V_{\rm BD}$ of a semi-SJ to a greater extent than high Q_p conditions [5].

In general, the graded charge profile modulates the electric field even when charge imbalance is present [19]. The introduction of $\alpha=10^\circ$ for the proposed semi-SJ fractionally increases the $R_{\rm ON,SP}$ by 5% due to slight pinching at the surface. However, this could be recovered by the inclusion of an n-type $t_{\rm top}$ region with increased doping. Therefore, the graded charge profile in combination with the n-BAL provides a wide implantation window for the semi-SJ structures without comprising the $V_{\rm BD}$ or $R_{\rm ON,SP}$. Without the n-BAL, in the case of the vertical full-SJ devices seen in Fig. 4, over- or underdoping the p-region has a symmetrical detrimental impact, sharply reducing the $V_{\rm BD}$.

C. Reverse Characteristics

The structures simulated in this study have been optimized to support a $V_{\rm BD} > 2.1$ kV. As discussed in Section III-B, the peak $V_{\rm BD}$ of the proposed semi-SJ with $\alpha = 10^{\circ}$ is achieved at high Q_p conditions. In turn, this pushes the peak electric field away from the surface and deeper in the structure, lowering the electric field at the surface. The reduced electric field at the surface combined with a reduced Schottky contact area, due to the introduction of α , results in a significant reduction of leakage current. This can be seen in Fig. 7, where the leakage current is reduced by one order of magnitude compared to our previous fully optimized full-SJs and by two orders of magnitude when compared to either of the 0° vertical full-SJs. Indeed, the proposed device displays a leakage current that is comparable that of the planar device. It should be noted, however, that although the planar SBD achieves a comparable $V_{\rm BD}$, the doping of the drift region is an order of magnitude lower and thus the $R_{ON,SP}$ is significantly higher.

The potential distribution at the onset of $V_{\rm BD}$ for the proposed semi-SJ can be seen in Fig. 8. It can be seen that the potential contours are evenly distributed throughout the device and thus the electric field demonstrates near-rectangular characteristics.

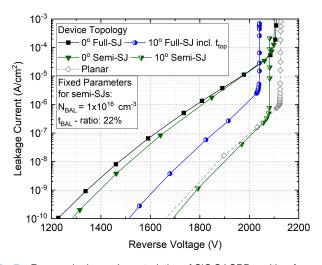


Fig. 7. Reverse leakage characteristics of SiC SJ SBDs, with reference to a planar SBD optimized to 2.1 kV.

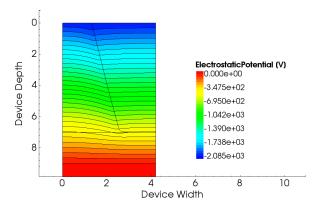


Fig. 8. Potential distribution at the onset of $V_{\rm BD}$ at 2085 V, for an optimized 10° semi-SJ (axes units: μ m).

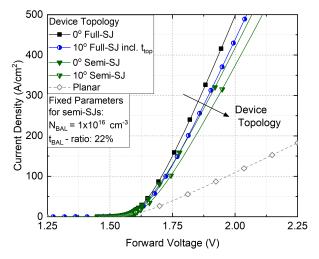


Fig. 9. Forward voltage characteristics of the proposed SJs, with reference to a planar SBD optimized to 2.1 kV.

D. Forward Characteristics

In Fig. 9, the forward voltage drop across the simulated SJ devices can be seen and are compared to an ideal planar SBD with an equivalent t_{drift} . All structures have a Ni

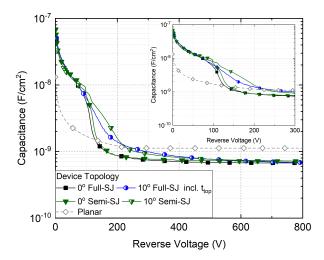


Fig. 10. *C*–*V* characteristics of SiC SJs with varying device topologies.

Schottky contact and can be seen to turn-on around 1.6 V, consistent with the work function of Ni. All the SJ structures simulated have a comparable $R_{\rm ON,SP}$. Both the full- and semi-0° SJs achieve a lower $R_{\rm ON,SP}$ than their equivalent $\alpha=10^\circ$ counterparts. The $R_{\rm ON,SP}$ is higher in the $\alpha=10^\circ$ structures due to increased JFET action—a result of the p-pillars being closer together at the surface due to the sidewall tilt. In the $\alpha=10^\circ$ full-SJ, the pinching is partially reduced due to the introduction of the more highly doped $t_{\rm top}$ region. The $t_{\rm top}$ region also helps to rebalance the top of the structure and recover the lost $V_{\rm BD}$ [15], a result of $\alpha>0^\circ$ inducing local charge imbalance in the structure. The $t_{\rm top}$ region could also be introduced into the $\alpha=10^\circ$ semi-SJ.

E. Capacitance-Voltage and Switching Characteristics

C-V simulations were performed on the proposed devices and compared to that of both the vertical full-SJ and the planar SBD within the study, as can be seen in Fig. 10. The SJs exhibit the characteristic nonlinear SJ response as a result of the lateral expansion of the depletion region from the SJ pillars. The depletion region can be seen to expand rapidly throughout the charge balanced vertical full-SJ with a sharp decrease in dc/dV, the cause of the "snappy" switching response within SJ structures. Likewise, the depletion region expansion throughout the vertical semi-SJ is also rapid. However, the thin and highly doped N_{BAL} marginally slows the expansion of the depletion region, due to the additional unbalanced charge. In comparison, the $\alpha = 10^{\circ}$ structures exhibit a delayed expansion of the depletion region, a result of the $\alpha > 0^{\circ}$ and the introduction of the graded charge profile. It can be seen that the $\alpha = 10^{\circ}$ semi-SJ has the most gradual dc/dV response.

Reverse recovery simulations shows that the simulated SJ structures offer fast switching, as expected from majority carrier devices. The results from the reverse recovery simulation can be seen in Fig. 11 where the *dI/dt* was set at 1000 A/(cm²·µs), comparable to the experimental results demonstrated by Kimoto and Cooper [20]. The 0° full-SJ can be seen to exhibit the characteristic "snappy" SJ response,

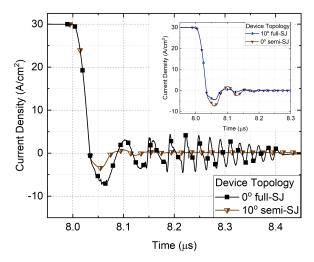


Fig. 11. Reverse recovery characteristics for both full- and semi-SJs with vertical 10° trench sidewalls.

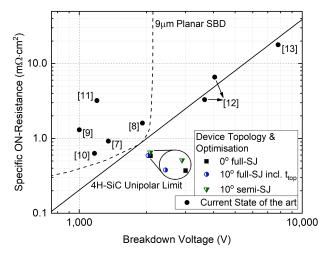


Fig. 12. Proposed SJ devices compared against the current fabricated state-of-the-art SiC SJs [7]–[13], plotted against the SiC 1-D-limit and a planar $9-\mu m$ SBD.

as detailed in Section III-D, producing a peak reverse recovery current (I_{RR}) of 7.5 A/cm². It can be seen that the proposed semi-SJ topology suppresses the ringing of the switching response and also reduces the peak I_{RR} by 50% to 3.5 A/cm², a result of both the delayed depletion region expansion (due to the graded charge profile throughout the n-pillar) and the unbalanced n_{BAL} .

IV. BENCHMARKING TO OTHER SJ DEVICES

The optimized SiC full-SJ and semi-SJ structures have been compared with the current state-of-the-art SJ devices from other experimental and commercial demonstrations, as well as other computational studies, as shown in Fig. 12. The devices are plotted against Kimoto's updated unipolar limit [21] and also against the optimization curve of a 1-D planar Schottky diode with a 9- μ m drift region, the dashed line representing a sweep of the drift region doping. Fig. 12 shows that the optimized SJ devices improve the tradeoff between $V_{\rm BD}$ and $R_{\rm ON,SP}$, pushing the devices below the SiC unipolar limit. However, it must be noted that although all structures

achieve comparable a $V_{\rm BD}$ and $R_{\rm ON,SP}$, the proposed semi-SJ achieves these characteristics with an improved implantation window, a reduced trench aspect ratio and improved switching characteristics.

V. CONCLUSION

In this article, a semi-SJ structure is proposed with a drift length of 9 μ m. Variants with and without a trench sidewall angle of 10° are compared and benchmarked to a planar SBD and a full-SJ. The structures are designed to achieve a $V_{\rm BD}$ of 2.1 kV and in turn, offer a guide for SiC SJ fabrication.

It was found that the introduction of $\alpha>0^\circ$, into both full- and semi-SJs, induced a graded charge profile throughout the n-pillar and widens the implantation window. However, the tilted sidewall angle brings about charge imbalance, due to the asymmetric pillar geometry reducing the $V_{\rm BD}$ and increasing the $R_{\rm ON,SP}$. In the case of the full-SJ, it is necessary to use a highly doped surface region to rebalance the surface of the structure and reduce the effects of pinching, so recovering both the $V_{\rm BD}$ and $R_{\rm ON,SP}$. In contrast, when the tilted sidewall angle is imposed upon the semi-SJ topology, the change in $V_{\rm BD}$ and $R_{\rm ON,SP}$ is so marginal, there is no need for the added processing complication of the $t_{\rm top}$ region. Furthermore, the $V_{\rm BD}$ achieved with a significantly reduced leakage current, a result of the reduced electric field at the surface.

In conclusion, the $\alpha=10^{\circ}$ semi-SJ with a $t_{\rm BAL}$ -ratio of 22% offers the designer an equivalent $V_{\rm BD}$ and $R_{\rm ON,SP}$ to the full-SJ but with two orders of magnitude less leakage, an implantation window up to 34% wider, softer switching characteristics, and a reduced aspect ratio when compared to the full vertical SJ.

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