InP/GaAsSb Double Heterojunction Bipolar Transistor Emitter-Fin Technology With $f_{MAX} = 1.2$ THz

Akshay M. Arabhavi, *Graduate Student Member, IEEE*, Filippo Ciabattini, Sara Hamzeloui, Ralf Flückiger, Tamara Saranovac, Daxin Han, *Graduate Student Member, IEEE*, Diego Marti, Giorgio Bonomo, Rimjhim Chaudhary, Olivier Ostinelli, and Colombo R. Bolognesi, *Fellow, IEEE*

***Abstract*— We report a new InP/GaAsSb double heterojunction bipolar transistor (DHBT) emitter fin architecture with a record $f_{MAX} = 1.2$ THz, a simultaneous $f_T = 475$ GHz, and $BV_{CEO} = 5.4$ V. The resulting $BV_{CEO} \times f_{MAX} = 6.48$ THz-V is unparalleled in semiconductor technology. Devices were realized with a 20-nm-thick compositionally and impurity graded GaAsSb-base and a 125-nm InP collector. The performance arises because the process allows: 1) a tunable base–emitter access distance down to 10 nm; 2) the use of thicker base contact metals; and 3) the minimization of parasitic capacitances and resistances via precise lateral wet etching of the base–collector (B/C) mesa. Perhaps more significantly, InP/GaAsSb DHBTs with $f_{MAX} \geq 1$ THz are demonstrated with emitter lengths as long as 9.4 μm and areas as high as 1.645 μm^2. Such an area is $>6\times$ larger than previously reported terahertz (THz) DHBTs, representing a breakthrough in THz transistor scalability. This attractive performance level is achieved with a very low dissipated power density which makes InP/GaAsSb DHBTs well-suited for high-efficiency millimeter- and submillimeter-wave applications. Furthermore, we provide the first large-signal characterization of a THz transistor with 94 GHz load-pull measurements showing a peak power-added-efficiency (PAE) of 32.5% (40% collector efficiency) and a maximum saturated power of 6.67 mW/μm^2 or 1.17 mW/μm of emitter length in a common-emitter configuration. Devices operate stably under large-signal conditions, with voltages nearly twice higher than those for peak small-signal performance.**

***Index Terms*— Double heterojunction bipolar transistors (DHBTs), GaAsSb, InP, maximum oscillation frequency, terahertz (THz).**

I. Introduction

TYPE-II double heterojunction bipolar transistors (DHBTs) based on InP/GaAsSb were developed to alleviate the electron blocking effect at the base–collector heterojunction encountered in "Type-I" GaInAs-based DHBTs [1]. The staggered band alignment allows using a pure InP collector resulting in a simplified base–collector heterojunction design. A conduction band offset of ~150 meV between the GaAsSb-base and the InP-collector eases electron injection into the collector. Other advantages of the InP collector include reproducibility, ease of manufacturing, high thermal conductivity, and higher breakdown voltages for a given cutoff frequency. To date, Type-II DHBTs showed attractive RF performances with maximum oscillation frequencies f_{MAX} over 800 GHz with open-base common-emitter breakdown voltage $BV_{CEO} > 4.5$ V [2]–[4]. Nippon Telegraph and Telephone Corporation (NTT) reported transferred substrate InP/GaAsSb DHBTs with a record $f_T = 813$ GHz [4]. Low offset/knee voltages, promising large-signal properties with over 30% power-added-efficiency (PAE) at 94 GHz [5], and superior linearity characteristics position InP/GaAsSb-based DHBTs well for submillimeter wave (mm-wave) applications [6].

In extending DHBTs to higher frequencies, the base and collector layer thicknesses are generally lowered to minimize the base–collector transit delay contributions. Recently, a scaling roadmap has been laid out in this direction for Type-II DHBTs to attain $f_T > 1$ THz [7]. Although the base and collector transit delay times decrease with vertical scaling, the higher base sheet resistance and junction capacitance increase the *RC*-delay resulting in reduced power gain cutoff frequency (f_{MAX}). In mm-wave and sub-mm-wave circuits such as oscillators and power amplifiers, f_{MAX} becomes more relevant than f_T in defining the useful frequency range of the device [8]. For a given base–collector layer thickness, reducing parasitic capacitances and resistances is the key to achieving a higher maximum oscillation frequency (f_{MAX}). In the present work, we describe a new emitter electrode fin process designed to push the f_{MAX} of the DHBTs beyond 1 THz without reducing f_T and BV_{CEO}. The new emitter electrode fin process enables arbitrary optimization of the base access distance (down to 10 nm) and the use of thick base metal. The extrinsic base–collector junction area was also aggressively undercut by wet etching until the base contact width was equal to one transfer length. We show (0.25×4.4) μm^2 DHBTs

Manuscript received November 8, 2021; revised December 9, 2021; accepted December 21, 2021. Date of publication January 6, 2022; date of current version March 28, 2022. This work was supported in part by the Swiss National Science Foundation Project ULTIMATE under Grant 200021L_169413. This article is an extended version of a paper presented at IEDM 2021. The review of this article was arranged by Editor T. Grasser. *(Corresponding author: Colombo R. Bolognesi.)*

The authors are with the Laboratory for Millimeter-Wave Electronics, Department of Information Technology and Electrical Engineering (D-ITET) ETH Zürich, 8092 Zürich, Switzerland (e-mail: colombo@ieee.org).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2021.3138379.

Digital Object Identifier 10.1109/TED.2021.3138379

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

TABLE I
EPITAXIAL LAYER STRUCTURE

Material	Doping (cm^{-3})	Thickness
$Ga_{0.47}In_{0.53}As$ → $Ga_{0.25}In_{0.75}As$	Si : 3.9×10^{19}	10 nm
InP	Si : 1.4×10^{19}	20 nm
InP	Si : 2.2×10^{16}	5 nm
$Ga_{0.22}In_{0.78}P$ → InP	Si : 2.2×10^{16}	10 nm
$Ga_{0.22}In_{0.78}P$	Si : 2.2×10^{16}	5 nm
$GaAs_{0.42}Sb_{0.58}$ → $GaAs_{0.61}Sb_{0.39}$	C : 8.5×10^{19}	20 nm
InP	Si : 1.0×10^{17}	125 nm
InP	S : 2.9×10^{19}	50 nm
$Ga_{0.47}In_{0.53}As$	Si : 4.0×10^{19}	20 nm
InP	S : 2.9×10^{19}	300 nm
InP semi-insulating substrate		350 µm

with a maximum oscillation frequency $f_{MAX} = 1.2$ THz with $f_T = 475$ GHz, and a high breakdown voltage $BV_{CEO} = 5.4$ V. The resulting $BV_{CEO} \times f_{MAX} = 6.48$ THz-V is unparalleled in semiconductor technology, significantly exceeding GaN or InP HEMT metrics [9], [10]. Unprecedented scalability is demonstrated: for the first time, DHBTs with $f_{MAX} > 1$ THz are made with emitter lengths of up to 9.4 μm and areas of $A_E = 1.645$ μm^2. The fastest GaInAs DHBTs to date showed $f_{MAX} = 1.15$ THz with $BV_{CEO} < 3.5$ V, and $f_{AVG} \times BV_{CEO} = (f_T \times f_{MAX})^{1/2} \times BV_{CEO} < 2.73$ THz-V with an emitter area of $(0.13 \times 2.0) = 0.26$ μm^2 [11]. In contrast, the present work yields, among others, $f_{AVG} \times BV_{CEO} = 4.08$ THz-V with $A_E = 1.1$ μm^2.

II. DEVICE FABRICATION

The DHBT epitaxial layers described in Table I were grown by metal-organic vapor-phase epitaxy (MOVPE) on 2-inch semi-insulating InP substrates. A graded GaInP/InP emitter eliminates the conduction band offset at the emitter-base (E/B) interface and minimizes emitter size effects [12]. The 20-nm $GaAs_xSb_{1-x}$ base is implemented with the As-mole fraction ramped from $x = 0.61$ at the emitter to $x = 0.42$ at the collector interface. The base layer also involves a linear grading of the carbon p-doping with an average level of 8.5×10^{19} cm^{-3}. The overall structure is similar to [2], except for a thinner 20 nm $n+$ InP emitter and 10 nm GaInAs emitter contact layers to minimize the emitter undercut etching.

In our previous works [2], the heavily doped 165 nm InP/GaInAs emitter layers prevented the shorting of the emitter with the self-aligned (to the emitter) base metal. The fabrication flow for these devices is reported elsewhere [2]. The resulting distance between the emitter and base metal (base access distance) ∼50 nm is predefined due to directional wet etching of InP. A reduced access distance would require a thinner heavily doped emitter resulting in thinner base metal thickness and higher base metal resistance. A new emitter-fin process (described below) was developed upon redesigning the total emitter thickness reduced from 185 to 50 nm to circumvent the compromise between the access distance and metal thickness.

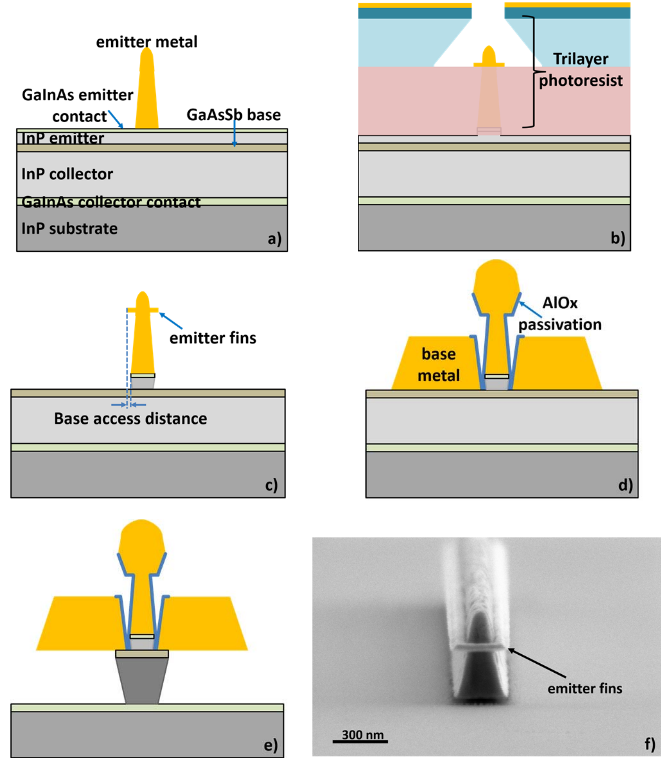

Fig. 1. Simplified schematic view of key emitter fin fabrication steps: (a) emitter metal; (b) emitter fin formation using a trilayer photoresist; (c) emitter mesa showing the base access distance; (d) self-aligned base contacts and AlO_x passivation; and (e) narrow base–collector mesa. *Note*: schematics not to scale. (f) SEM micrograph of the emitter after mesa formation.

Fig. 1 illustrates the salient steps of the new emitter fin formation process. Fabrication begins by patterning the emitter electrode metal by e-beam lithography (EBL) and Ti/Pt/Au deposition by e-beam evaporation. Next, the thin $n+$ GaInAs contact layer is etched by Ar sputtering, simultaneously smoothing the emitter metal edge roughness. Horizontal fins are then formed at the top of the emitter electrode using a trilayer photoresist and EBL [Fig. 1(b)]. The bottom resist layer consists of polydimethylglutarimide (PMGI), and the top two layers are P(MMA-MAA) copolymer and polymethyl methacrylate (PMMA-950K), respectively. The e-beam dose and the methyl isobutyl ketone-isopropyl alcohol (MIBK-IPA) solvent-based developing solutions were optimized to 1) define the desired fin-width; 2) have sufficient under-cut in the copolymer layer to ease the lift-off; and 3) remain insensitive to the bottom PMGI layer. After developing the resists, the emitter-fin is formed by e-beam evaporation and lift-off. The fin width, defined by EBL, arbitrarily sets the base access distance because the base metal is self-aligned to the emitter fins. After the fin formation, the InP emitter is etched in a phosphoric acid solution. Fig. 1(f) shows an SEM image after etching the emitter mesa, clearly showing the emitter metal fin electrode. The base contacts, self-aligned to the emitter fins, are patterned by a third EBL step. Soon after the development of the pattern, the samples are transferred into the e-beam evaporator, where a Pd/Ni/Pt/Au metal stack is evaporated after a quick cleaning of the base surface by an *in situ* Ar-sputtering. TEM-XRD analysis shows the diffusion

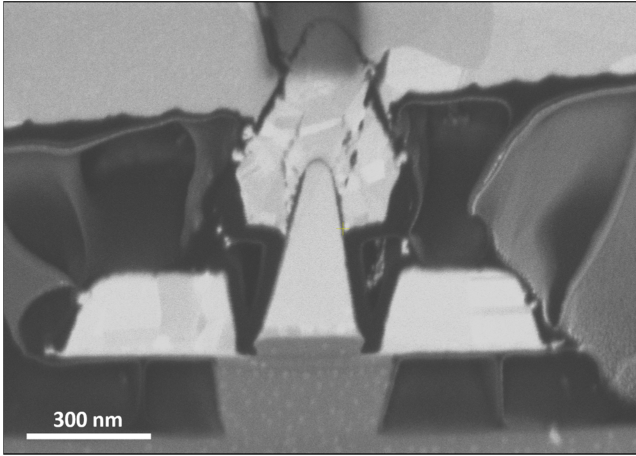

Fig. 2. SEM image of the completed device cross section with an emitter width of 250 nm and a 35 nm E/B access distance. The fin process allows much thinner semiconductor emitters compared to the standard process (Fig. 3).

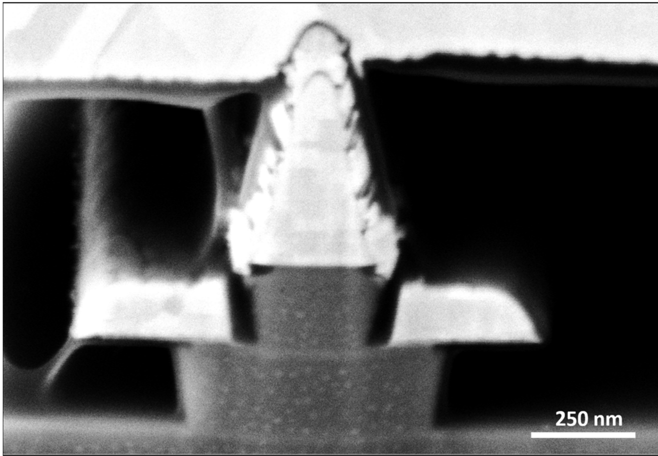

Fig. 3. SEM image of the cross section of the completed device with an emitter width of 250 nm fabricated using the standard emitter formation process. The E/B access distance is 50 nm.

of Pd and Ni into the base layer equally in the vertical and lateral directions. Hence, Pd/Ni composite thickness should be below 5 nm to prevent an emitter-base short in devices with a very small base access distance. The resulting contact resistivity $\rho_{B,C} \approx 1\ \Omega \cdot \mu m^2$. The process allows for a >50% thicker base contact metal compared to [2] because the base metal is no longer self-aligned to the emitter metal edge but to the emitter-fin located much higher with respect to the base layer (Figs. 2 and 3). After the base contact formation, the E/B region and the emitter are passivated using a conformal thin AlO_x deposited by Atomic Layer Deposition. The AlO_x film is blanket etched by inductively coupled plasma-reactive ion etching (ICP-RIE) using the emitter metal as a shadow mask, thus allowing AlO_x to remain in the gap between the emitter mesa and the base contact. The base layer is etched with a combination of dry (ICP-RIE) and wet etching. Wet undercut etching of the base–collector mesa is optimized to achieve an effective base contact width ~40 nm equal to the transfer length: only a transfer length equivalent of base material remains under the base metal contact. Further reductions in base contact width become deleterious because of an increased base resistance and a current gain reduction. A low-temperature (≤190 °C) Teflon based etch-back planarization completes the fabrication to support electron-beam evaporated coplanar probe pads. A focussed ion beam/scanning electron microscope (FIB/SEM) cross-section of the complete device with an emitter width of 250 nm is shown in Fig. 2. It is compared to a cross-sectional SEM image of a 250-nm wide device fabricated using our standard process in Fig. 3, showing that the emitter fin process allows thinner semiconductor emitter layers and thicker base metals to be used.

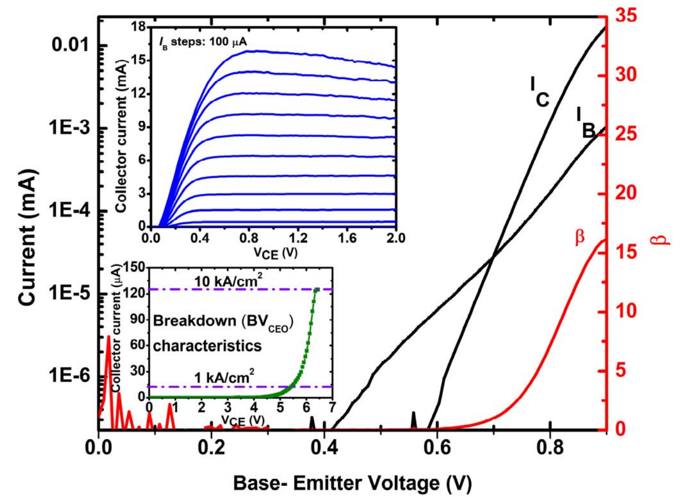

Fig. 4. Gummel characteristics ($V_{CB} = 0$ V) of a 0.25 × 4.4 μm^2 DHBT with a 35-nm base access distance. The dc gain as a function of V_{BE} is also plotted. *Insets*: Corresponding common-emitter I–V curves for I_B ranging from 0 to 1 mA and OPEN-base–collector breakdown characteristics for BV_{CEO} measurement.

III. Results and Discussion

A. DC Measurements

The DHBT static performance was parameterized using an HP4156B test instrument. Gummel characteristics with $V_{BC} = 0$ V for a (0.25 × 4.4) μm^2 DHBT with a 35-nm base access distance are shown in Fig. 4. The collector/base current ideality factors are $n_C = 1.09$ and $n_B = 1.85$, respectively. A maximum common-emitter current gain of $\beta = 16$ is measured with this geometry, whereas large-area devices fabricated entirely by wet etching process on the same material show a maximum $\beta = 42$. The obtained β and n_B values are attributed to 1) the reduced base access distance; 2) dry etching damage; and 3) the aggressive B/C undercut etching and collector current spreading. Fig. 4(a) shows the corresponding I_C–V_{CE} characteristics. The negative slope of the I–V curves at higher currents and voltages is due to self-heating. The open-base common-emitter breakdown characteristics plotted in Fig. 4(b) shows a $BV_{CEO} = 5.4$ V defined at $J_C = 1$ kA/cm² = 0.01 mA/μm^2, or > 6.5 V for $J_C = 10$ kA/cm² (as used in [11]). The devices show low offset and knee voltages along with a relatively high breakdown voltage, which is favorable for high-efficiency high-power applications.

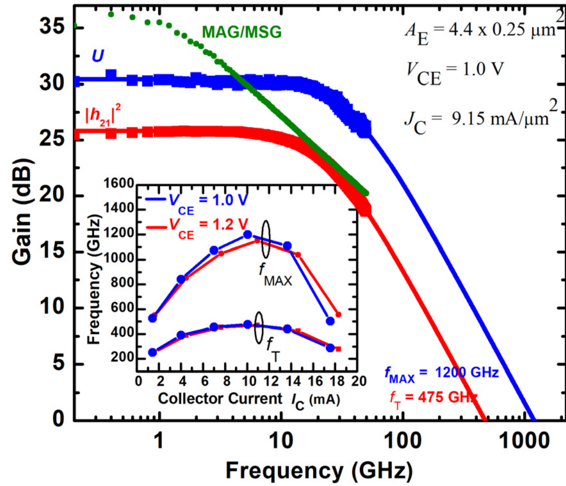

Fig. 5. Measured small-signal current gain $|h_{21}|^2$, MAG/MSG and Mason's unilateral gain U. f_T and f_{MAX} are determined from single-pole fits and extrapolations. *Inset*: Bias dependence of f_T and f_{MAX} versus current at $V_{CE} = 1.0$ and 1.2 V.

B. Small-Signal RF Measurements

The small-signal RF performance was measured on a PNA-X vector network analyzer from 0.02 to 50 GHz (with an input power of –30 dBm). An off-wafer impedance standard and line/reflect/reflect/match (LRRM) calibration were used to set the reference planes to the probe tips. Following broadly used short-open de-embedding, Mason's unilateral power gain U and the common-emitter short-circuit current gain $|h_{21}|^2$ are plotted against frequency in Fig. 5. Extrapolations from single-pole fits using the entire frequency dataset yield a peak $f_{MAX} = 1.2$ THz with $f_T = 475$ GHz at $V_{CE} = 1.0$ V. The same extrapolation range was also used in [11]. The current density at peak f_T is $J_C = 9.15$ mA/μm^2. The collector current dependence of f_T and f_{MAX} for $V_{CE} = 1.0$ and 1.2 V is shown in Fig. 5 inset. The small-signal equivalent circuit (SSEC) model extracted/optimized from the measured S-parameters at $V_{CE} = 1.0$ V is shown in Fig. 6. The SSEC elements were initially extracted as per [13], and further optimized using the gradient optimizer in Keysight's advanced design system (ADS) to fit the equivalent circuit model to the measurements. The measured/simulated S-parameters with U, maximum available gain/maximum stable gain (MAG/MSG), and $|h_{21}|^2$ are plotted in Fig. 7, showing good fits. Extrapolations at –20 dB/dec of the modeled U_{model} from 50 GHz $\leq f \leq$ 0.5 THz confirm the experimentally determined $f_{MAX} = 1.2$ THz. Work is under way to characterize the emitter fin DHBTs at higher frequencies using E&M optimized probing and on-wafer calibration structures (not included in the present process development mask set) [14]. Past experience shows extension to higher measurement frequencies does not affect conclusions drawn from measurements up to 50 GHz on our transistors [14]. Results will be reported in due time.

The present f_{MAX} improvement is achieved by minimizing the $(R_B C_{BC})_{EFF}$ denominator contribution to f_{MAX} [15]

$$f_{MAX} = \sqrt{\frac{f_T}{8\pi (R_B C_{BC})_{EFF}}}$$

$$(R_B C_{BC})_{EFF} = R_{B,in} C_{BC,in} + R_{B,ex}(C_{BC,in} + C_{BC,ex}) \quad (1)$$

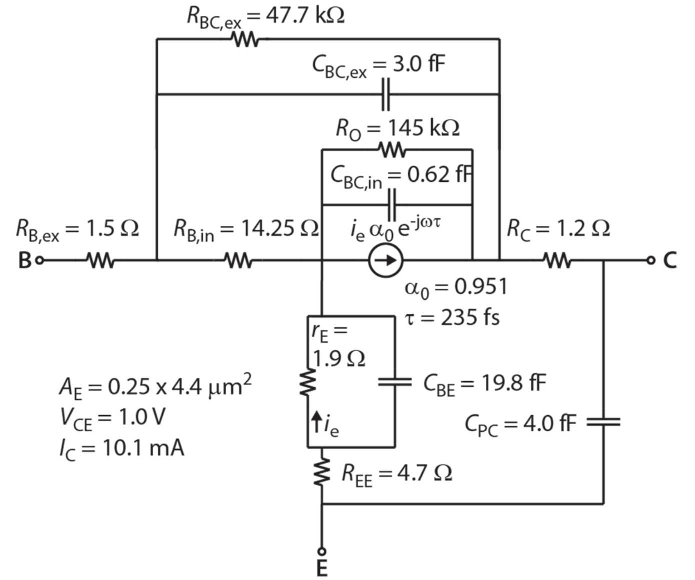

Fig. 6. Extracted SSEC model at the peak f_T/f_{MAX} bias condition.

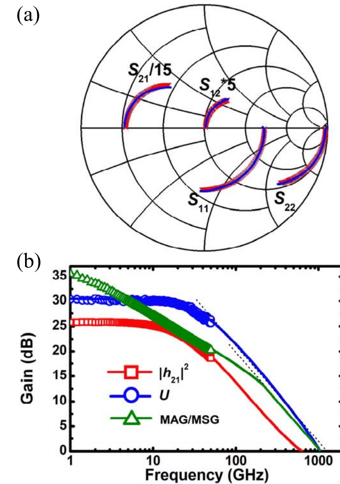

Fig. 7. (a) Measured/simulated S-parameters for Fig. 6 model. (b) Measured/simulated $|h_{21}|^2$, MAG/MSG, and $U(f)$ showing good fit quality. 20 dB/dec extrapolations of the modeled U_m from frequencies as high 0.5 THz confirm $f_{MAX} = 1.2$ THz. For $f \geq 0.5$ THz, the U_m modeled roll-off increases: verification would require reliable U data in the 0.5–1 THz range.

(where $R_{B,in}$, $R_{B,ex}$ and $C_{BC,in}$, $C_{BC,ex}$ are the intrinsic and extrinsic base resistances and B/C capacitances, respectively), by reducing the base access distance through our new emitter fin formation, increasing the base metal thickness, and reducing the collector-to-emitter area ratio. A shorter access distance reduces the base resistance as well as the B/C capacitance. Even though the fin process allows the controlled reduction of the base access distance down to ∼10 nm, recombination at the base contact degrades the dc current gain β, and creates a tradeoff between the base access resistance and β. Injected electrons diffusing laterally toward the base contacts give rise to a base contact recombination current. Fig. 6 in [16] indicates that $\beta < 10$ for access distances approaching the base thickness (20 nm). DHBTs with access distances as low as 20 nm also show $f_{MAX} > 1$ THz but are not considered further

TABLE II
COMPARISON OF f_T/f_{MAX} AND BASE–COLLECTOR PARASITICS FOR THE STANDARD PROCESS [2] AND THE PRESENT EMITTER-FIN PROCESS

	Existing process technology	This work (emitter fin process)
Device size	0.25 × 4.4 μm²	0.25 × 4.4 μm²
β	30	16
f_T/f_{MAX} (GHz)	486/790	475/1200
$R_{B,in}$ (Ω)	15.84	14.25
$R_{B,ex}$ (Ω)	4.61	1.50
$C_{BC,in}$ (fF)	0.69	0.62
$C_{BC,ex}$ (fF)	3.36	3.00

here because of their low gain. The inset of Fig. 6 in [16] shows a FIB/SEM image of a device with an extremely small base-access distance ~10 nm. Table II contrasts the SSEC elements and DC/RF figures-of-merit from this work with a DHBT of the same A_E from our previous process: evident reductions in the total base resistance and B/C capacitance are seen. Inserting the extracted values of base resistances and capacitances in the approximation of (1) yields an estimated $f_{MAX} = 1.15$ THz for the emitter fin process, in fair agreement with the extracted f_{MAX}.

The base metal resistance contribution to the overall base resistance cannot be discounted for highly scaled devices. The base metal resistance charges both the intrinsic and extrinsic BC-capacitances of the device. In Rode *et al.* [17], a thicker base metal formed by dual-deposited base contacts is one of several process enhancements used to lower the overall base resistance and improve f_{MAX}. A simplified analytical expression for base metal resistance R_{bm} considering its distributed nature of the base potential along the length of the emitter is derived in [18] and [19]

$$R_{bm} = \frac{1}{2} \cdot \frac{\rho_{bm} \cdot L_E}{T_{bm} \cdot W_{bm}} \cdot \left(\frac{\tan K - K}{K \cdot \tan^2 K} \right)$$

and

$$K \cdot \tan K = \frac{\rho_{bm} \cdot L_E}{T_{bm} \cdot W_{bm}} \cdot \frac{I_B}{2 \cdot V_T} \tag{2}$$

where ρ_{bm} is the metal resistivity, L_E is the length of the emitter, T_{bm} and W_{bm} are the thickness and width of the base metal, I_B is the base current in one of the two base contacts, and V_T is the thermal voltage. Fig. 8 plots the base metal resistance as a function of emitter length for various base metal thicknesses calculated for the devices with 0.175 μm emitter width. For longer devices, the base metal resistance becomes a significant contributor to the overall base resistance, as seen from the dashed lines. The total base metal resistance (R_{tot}) plotted with triangular symbols was calculated as

$$R_{tot} \cong R_{bm} + \frac{R_{sh}}{2 \cdot L_E} \cdot \left[\frac{W_E}{6} + W_{gap} + \sqrt{\frac{\rho_{bc}}{R_{sh}}} \right] \tag{3}$$

where R_{sh} is the base sheet resistance, W_E is the emitter width, W_{gap} is the E/B access distance, and ρ_{bc} is the base

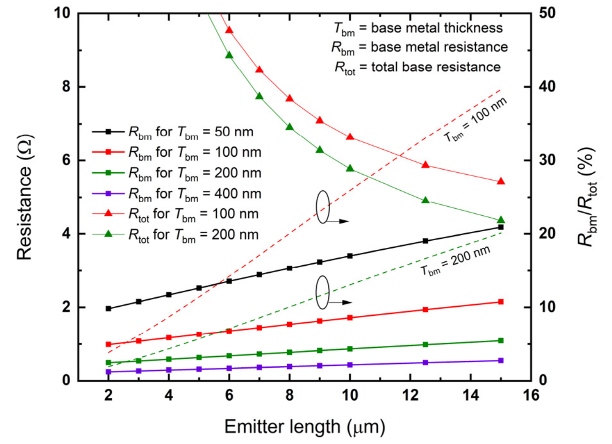

Fig. 8. Variation of base metal resistance with base metallization thickness for various emitter lengths (square markers). Calculated total base resistance for two base metal thicknesses as a function of emitter length is shown in curves with triangular markers. On the right y-axis: the percentage contribution of metal resistance for two base metal thicknesses as a function of emitter length (dashed lines). The calculations are for devices with 175 nm emitter width and a 35-nm E/B access distance, at collector current density of 10 mA/μm^2.

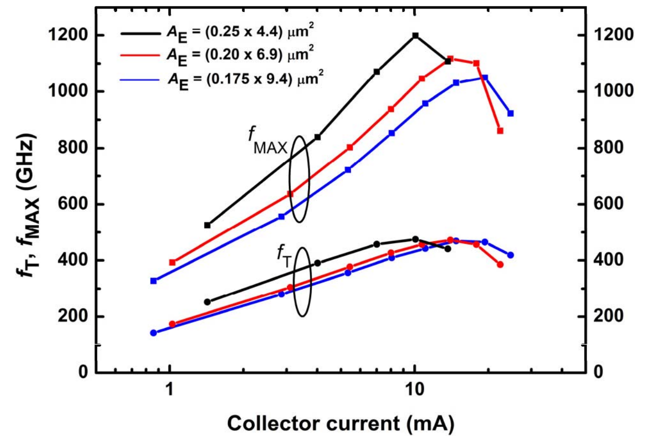

Fig. 9. Plot of f_T/f_{MAX} versus collector current for various emitter mesa sizes with an E/B access distance of 35 nm. Several emitter sizes achieve $f_{MAX} > 1$ THz, including an emitter mesa length of 9.4 μm with $A_E = 1.645$ μm^2. The previous state-of-the-art result of $f_{MAX} = 1.15$ THz was for $A_E = 0.26$ μm^2 [11], emphasizing the present breakthrough in DHBT scalability.

contact resistivity. The current emitter-fin process allows an increase in the base metal thickness to ~300 nm. With such a low base metal resistance contribution, devices with an emitter length of 9.4 μm achieve an unprecedented $f_{MAX} > 1$ THz—this represents a breakthrough in terahertz (THz) DHBT scalability. Fig. 9 plots f_T/f_{MAX} versus I_C for various geometries. Specifically, (0.20 × 6.9) μm^2 emitter devices show a peak $f_{MAX} = 1.10$ THz compared to 1.05 THz for (0.175 × 9.4) μm^2 DHBTs.

The present results are contrasted to the fastest reported GaInAs/InP [11] and SiGe HBTs [20] in Table III. Type-II DHBTs offer significantly higher $f_{T,MAX} \times BV_{CEO}$ products compared to the other technologies. The dissipated power density in mW/μm^2 at the peak f_{MAX} bias point is also 4.6× times lower in the devices presented here. Lower power

TABLE III
COMPARATIVE ASSESSMENT OF STATE-OF-THE-ART SiGe HBT, TYPE-I AND TYPE-II InP DHBTs

	SiGe HBT [20]	Type-I: GaInAs [11]	Type-II: GaAsSb [present work]
Peak f_T (GHz)	505	520	475
Peak f_{MAX} (THz)	0.72	1.15	1.20
Emitter Area (μm^2)	8×(0.105×1.0)	0.13×2.0	0.25×4.4
BV_{CEO} (V)	1.6	3.5	5.4
$f_T \times BV_{CEO}$ (THz-V)	0.81	1.82	2.56
$f_{MAX} \times BV_{CEO}$ (THz-V)	1.15	4.03	6.48
V_{CE}/I_C (V/mA)	1.14 / 28.90	1.6 / 6.90	1.0 / 10.06
P_D/A_E (mW/μm^2)	42.31	42.46	9.15

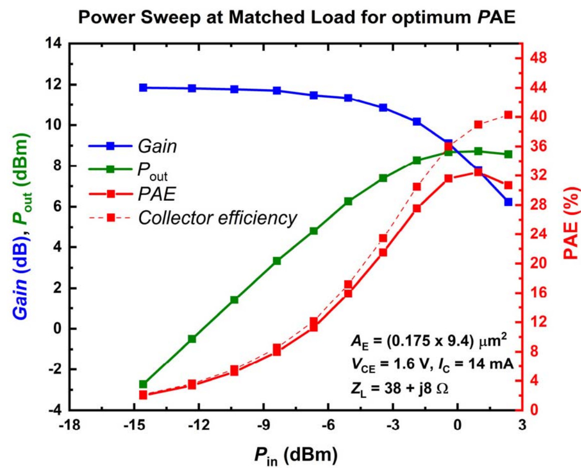

Fig. 10. 94 GHz single-tone CW power characteristics of a (0.175 × 9.4) μm^2 DHBT with optimally matched load impedance for peak efficiency.

dissipation is advantageous in terms of efficiency, reduced self-heating, and higher device reliability.

C. Large-Signal Measurements at 94 GHz

Large-signal measurements characterize the high-power capabilities of the devices at high frequencies. We performed single tone continuous-wave (CW) power measurements at 94 GHz, using an active loop load-pull setup described in [21], on single finger (0.175 × 9.4) μm^2 DHBTs biased for class-A operation. The source impedance was set to 50 Ω, and the load impedance was swept to determine the optimal load match for best saturation output power $P_{out,sat}$ and PAE. The best efficiency and saturated output power were obtained at $V_{CE} = 1.6$ and 1.9 V, respectively. These voltages are significantly higher than that yielding peak f_T/f_{MAX}. In all cases, the collector current density was ~8.5 mA/μm^2 at low-P_{in}.

Fig. 10 shows the power characteristics of the device at $V_{CE} = 1.6$ V and $I_B = 1$ mA. An excellent PAE = 32.5% is obtained with simultaneous $P_{out,sat} = 8.73$ dBm and a gain of 7.8 dB at 94 GHz. The collector efficiency is 40.3%, and the linear gain of the device at this bias is 11.85 dB.

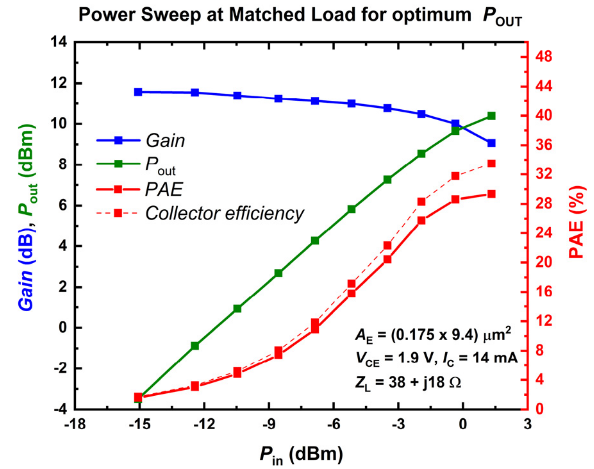

Fig. 11. 94 GHz single-tone CW power characteristics of a (0.175 × 9.4) μm^2 DHBT biased and matched for peak output power.

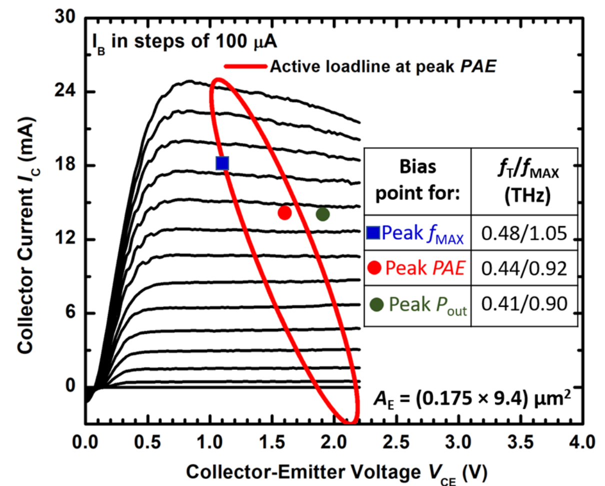

Fig. 12. Reconstructed 94 GHz dynamic loadline at peak PAE superposed on the common-emitter I–V curves. The bias points and their corresponding f_T/f_{MAX} at peak f_{MAX}, PAE and P_{OUT} performance are also noted.

The peak saturated output power at $V_{CE} = 1.9$ V and $V_{BE} = 832$ mV is 10.4 dBm with a corresponding gain of 9.1 dB and PAE = 29.3%, as shown in Fig. 11. This corresponds to a power density of 6.67 mW/μm^2 (1.17 W/mm). It is interesting to note that the optimum load impedances Z_L for peak efficiency and maximum output power are quite similar, indicating excellent device versatility. Importantly, the V_{CE} biases used in the above large-signal measurements far exceed the $V_{CE} = 1.0$ V required for peak small-signal performance (Fig. 5): our 0.175 μm wide devices with peak f_{MAX} = 1.05 THz operate stably, with no evidence of degradation. Such device stability under aggressive large-signal operation suggests inherent reliability advantages in the InP-GaAsSb material system. Physical grounds behind the expected high reliability of InP/GaAsSb DHBTs were discussed in [3]. In contrast, 0.25 μm InP/GaInAs DHBTs with f_{MAX} = 650 GHz (and peak PAE = 35% at 10 GHz) were load-pulled at a lower (V_{CE} = 1 V) bias than needed for peak f_T/f_{MAX} performance (V_{CE} = 1.6–1.8 V) to avoid device degradation [22].

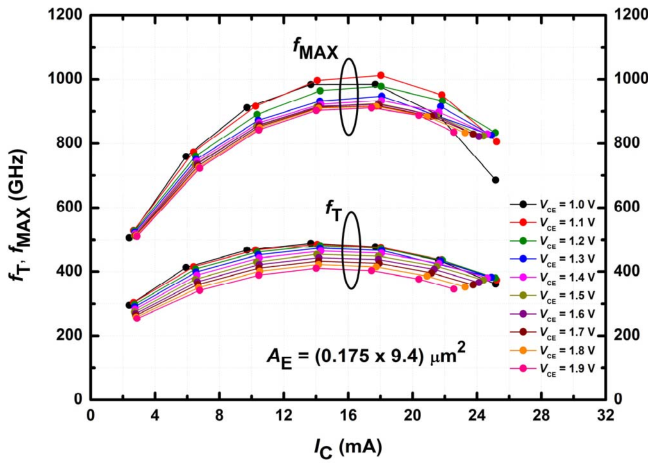

Fig. 13. Bias dependence of f_T and f_{MAX} versus collector current for $V_{CE} = 1.0$ to 1.9 V for the (0.175 × 9.4) μm² DHBT.

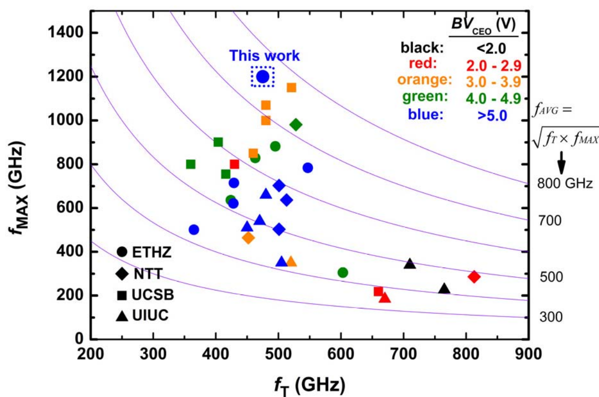

Fig. 14. Survey of reported InP DHBT metrics. Breakdown voltages are color-coded. This work sets new milestones for DHBTs with unparalleled $f_{MAX} \times BV_{CEO} = 6.48$ THz-V. $f_{AVG} \times BV_{CEO} > 4$ THz-V is the highest for DHBTs, nearly matching the 4.49 THz-V from GaN HEMTs [9].

Fig. 12 shows the measured 94-GHz dynamic load line for the bias point at peak efficiency superposed on the I–V curves. The f_T/f_{MAX} values at bias points for peak f_{MAX}, PAE, and P_{OUT} performance are also noted. In addition, Fig. 13 plots the variation of f_T/f_{MAX} versus I_C for $V_{CE} = 1.0$–1.9 V, revealing a ~10% reduction in f_{MAX} at $V_{CE} = 1.9$ V compared to the peak performance. When biased near peak small-signal performance at $V_{CE} = 1.2$ V, the device shows a PAE = 27.4% with simultaneous $P_{out,sat} = 7$ dBm and 6.3 dB gain (12 dB linear gain at low P_{in}) because even the weakest input power level of –15 dBm drives the transistor into the knee region and quasi-saturation. The present power performance involves no thermal management measures: significant improvements can still be achieved by substrate thinning and/or transferring devices to thermally conductive substrates like AlN or SiC.

Modern high bit rate telecommunications applications such as 5G+ networks use higher-order modulation formats with high peak-to-average power ratios, and a lower input power (power back-off, P_{BO}) is commonly used to maintain linearity and a low bit-error-rate. Because power-back-off reduces output power and PAE, it is pertinent to consider linear performance as well: at a 3-dB back-off point from $P_{out,sat}$, the 94 GHz output power is 7.4 dBm with a gain and PAE of 10.7 dB and 20%, respectively. A PAE of >12% is maintained with $P_{BO} = 6$ dB.

IV. Conclusion and Future Work

We demonstrated a new emitter fin process yielding a record $f_{MAX} = 1.2$ THz in a (0.25 × 4.4) μm² InP/GaAsSb DHBT. The devices offer $f_{MAX} \times BV_{CEO} = 6.48$ THz-V, the highest ever reported for a transistor. Thanks to thick base metal contacts, 9.4 μm long devices also achieve $f_{MAX} > 1$ THz for an emitter area of 1.645 μm². In comparison, the previous InP DHBT state-of-the-art reported $f_{MAX} = 1.15$ THz with $BV_{CEO} = 3.5$ V and $\beta \sim 17$ and a 0.26 μm² emitter area [11]. Fig. 14 puts our work in perspective with other InP DHBT technologies from the literature with color-coding for breakdown voltages. The use of a quaternary Type-II base layer as in [23] further improves f_T and enhances the dc current gain β. This results in a better balance between f_T and f_{MAX} without altering other figures of merit.

Defining $f_{AVG} = (f_T \times f_{MAX})^{1/2}$ for balanced performance also leads to a record InP DHBT metric of $f_{AVG} \times BV_{CEO} > 4$ THz-V, approaching the 4.49 THz-V of 20-nm GaN HEMTs [9] (reaching 4.9 THz-V with the less stringent BV_{CEO} definition from [11]). Our results also compare well to the highest performance reported for InP HEMTs with $f_T/f_{MAX} = 0.61/1.5$ THz and an OFF-state breakdown voltage $BV_{DS} = 3$ V, corresponding to $f_{MAX} \times BV_{DS} = 4.5$ THz-V and $f_{AVG} \times BV_{DS} < 2.9$ THz-V [10].

Work is under way to implement the present emitter fin device architecture using improved probe pad designs and on-wafer calibration structures along the lines of [14] to enable meaningful device characterization well above 100 GHz.

Despite aggressive scaling (see Fig. 2) down to an emitter width of 0.175 μm, THz InP/GaAsSb DHBTs demonstrate stable operation at voltages nearly 2× higher than those required for peak small-signal performance f_T/f_{MAX}, with an impressive peak PAE = 32.5% and saturated output power density of 1.17 mW/μm or 6.69 mW/μm² at 94 GHz in common-emitter operation. The (0.175 × 9.4) μm² transistors maintain a remarkable $f_{MAX} \geq 900$ GHz up to $V_{CE} = 1.9$ V, well above the 1.1 V needed for peak small-signal performance. The output power can be improved in a common-base configuration. The present scaling breakthrough, with the availability of THz transistors with larger junction areas capable of operation under high input drive and higher collector voltages opens opportunities for the generation of significant signal power at mm-wave and sub-mm wave frequencies. Device transfer to thermally conductive substrates [4] will significantly boost output power levels.

Acknowledgment

The authors would like to thank the staff of FIRST Laboratory at ETH Zurich, Zurich, Switzerland, for their support.

References

[1] C. R. Bolognesi, M. W. Dvorak, N. Matine, O. J. Pitts, and S. P. Watkins, "Ultrahigh performance staggered lineup ('type-II') InP/GaAsSb/InP NpN double heterojunction bipolar transistors," *Jpn. J. Appl. Phys.*, vol. 41, no. 2, pp. 1131–1135, Feb. 2002, doi: 10.1143/JJAP.41.1131.

[2] A. M. Arabhavi, W. Quan, O. Ostinelli, and C. R. Bolognesi, "Scaling of InP/GaAsSb DHBTs: A simultaneous $f_T/f_{MAX} = 463/829$ GHz in a 10 μm long emitter," in *Proc. IEEE BCICTS*, Oct. 2018, pp. 132–135, doi: 10.1109/BCICTS.2018.8551036.

[3] C. R. Bolognesi, R. Flückiger, M. Alexandrova, W. Quan, R. Lövblom, and O. Ostinelli, "InP/GaAsSb DHBTs for THz applications and improved extraction of their cutoff frequencies," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2016, pp. 723–726, doi: 10.1109/IEDM.2016.7838506.

[4] Y. Shiratori, T. Hoshi, and H. Matsuzaki, "Ultra-high speed InP/GaAsSb-based type-II double-heterojunction bipolar transistors and transfer technology onto SiC substrate," in *Proc. IEEE BCICTS*, Monterey, CA, USA, Nov. 2020, pp. 1–4, doi: 10.1109/BCICTS48439.2020.9392903.

[5] W. Quan, A. M. Arabhavi, D. Marti, S. Hamzeloui, O. Ostinelli, and C. R. Bolognesi, "InP/GaAsSb DHBT power performance with 30% class-A PAE at 94 GHz," in *Proc. IEEE BiCMOS Compound Semiconductor Integr. Circuits Technol. Symp. (BCICTS)*, Nashville, TN, USA, Nov. 2019, doi: 10.1109/BCICTS45179.2019.8972718.

[6] H. Xu, E. Iverson, K. Y. Cheng, M. Stuenkel, and M. Feng, "Nonlinearity characterization of submicron type-I InP/InGaAs/InP and type-I/II AlInP/GaAsSb/InP DHBTs," in *Proc. Compound Manuf. Tech. Conf. (CS MANTECH)*, Boston, MA, USA, Apr. 2012, Paper 6b.3.

[7] X. Wen *et al.*, "Performance prediction of InP/GaAsSb double heterojunction bipolar transistors for THz applications," *J. Appl. Phys.*, vol. 130, no. 3, Jul. 2021, Art. no. 034502, doi: 10.1063/5.0054197.

[8] M. Božanić and S. Sinha, "Emerging transistor technologies capable of terahertz amplification: A way to re-engineer terahertz radar sensors," *Sensors*, vol. 19, no. 11, p. 2454, May 2019, doi: 10.3390/s19112454.

[9] Y. Tang *et al.*, "Ultrahigh-speed GaN high-electron-mobility transistors with f_T/f_{max} of 454/444 GHz," *IEEE Electron Device Lett.*, vol. 36, no. 6, pp. 549–551, Jun. 2015, doi: 10.1109/LED.2015.2421311.

[10] X. Mei *et al.*, "First demonstration of amplification at 1 THz using 25-nm InP high electron mobility transistor process," *IEEE Electron Device Lett.*, vol. 36, no. 4, pp. 327–329, Apr. 2015, doi: 10.1109/LED.2015.2407193.

[11] M. Urteaga, R. Pierson, P. Rowell, V. Jain, E. Lobisser, and M. J. W. Rodwell, "130 nm InP DHBTs with $f_T > 0.52$ THz and $f_{max} > 1.1$ THz," in *Proc. 69th Device Res. Conf.*, Jun. 2011, pp. 281–282, doi: 10.1109/DRC.2011.5994532.

[12] R. Lövblom, R. Flückiger, O. Ostinelli, M. Alexandrova, and C. R. Bolognesi, "Emitter size effect in GaAsSb-based DHBTs with AlInP and GaInP emitters," *IEEE Electron Device Lett.*, vol. 34, no. 5, pp. 602–604, May 2013, doi: 10.1109/LED.2013.2250897.

[13] M. Rudolph, *Introduction to Modeling HBTs*. Norwood, MA, USA: Artech House, 2006.

[14] M. Deng *et al.*, "Design of on-wafer TRL calibration kit for InP technologies characterization up to 500 GHz," *IEEE Trans. Electron Devices*, vol. 67, no. 12, pp. 5441–5447, Dec. 2020, doi: 10.1109/TED.2020.3033834.

[15] K. Kurishima, "An analytic expression of f_{max} for HBT's," *IEEE Trans. Electron Devices*, vol. 43, no. 12, pp. 2074–2079, Dec. 1996.

[16] A. M. Arabhavi *et al.*, "InP/GaAsSb double heterojunction bipolar technology with $f_{MAX} = 1.2$ THz," presented at the IEDM Tech. Dig., Dec. 2021.

[17] J. C. Rode *et al.*, "Indium phosphide heterobipolar transistor technology beyond 1-THz bandwidth," *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp. 2779–2785, Sep. 2015, doi: 10.1109/TED.2015.2455231.

[18] W. Liu, "Emitter-length design for microwave power heterojunction bipolar transistors," *Solid-State Electron.*, vol. 36, no. 6, pp. 885–890, 1993, doi: 10.1016/0038-1101(93)90011-E.

[19] J. R. Hauser, "The effects of distributed base potential on emitter-current injection density and effective base resistance for stripe transistor geometries," *IEEE Trans. Electron Devices*, vol. ED-11, no. 5, pp. 238–242, May 1964, doi: 10.1109/T-ED.1964.15318.

[20] B. Heinemann *et al.*, "SiGe HBT with f_x/f_{max} of 505 GHz/720 GHz," in *IEDM Tech. Dig.*, Dec. 2016, pp. 3.1.1–3.1.4, doi: 10.1109/IEDM.2016.7838335.

[21] V. Teppati *et al.*, "A W-band on-wafer active load–pull system based on down-conversion techniques," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 1, pp. 148–153, Jan. 2014, doi: 10.1109/TMTT.2013.2292042.

[22] P. Sakalas, M. Schroter, T. Nardmann, and H. Zirath, "Harmonic distortion analysis of InP HBTs with 650 GHz f_{max} for high data rate communication systems," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS)*, Oct. 2017, pp. 1–4, doi: 10.1109/CSICS.2017.8240429.

[23] C. R. Bolognesi *et al.*, "Advances in InP/Ga(In)AsSb double heterojunction bipolar transistors (DHBTs)," *Jpn. J. Appl. Phys.*, vol. 58, Mar. 2019, Art. no. SB0802, doi: 10.7567/1347-4065/ab02e6.