Self-Aligned Double Injection-Function TFT for Deep Sub-Micrometer Channels' Length—Application to Solution-Processed Indium Gallium Zinc Oxide

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***Abstract*—We propose and demonstrate self-aligned Double Injection Function Thin Film Transistor (DIF-TFT) architecture that mitigates short channel effects in 200 nm channel on non-scaled insulator (100 nm SiO_2). In this conceptual design, a combination of ohmic-like injection contact and a high injection-barrier metal allows maintaining the high ON currents while suppressing drain-induced barrier lowering (DIBL) effects. Using an industrial 2-D device simulator (Sentaurus), we propose two methods to realize the DIF concept. We use one of them to demonstrate, experimentally, a DIF-TFT based on solution-processed indium gallium zinc oxide (IGZO). Using molybdenum as the ohmic contact and platinum as the high injection barrier, we compare three transistors' source-contacts: ohmic, Schottky, and DIF. The fabricated DIF-TFT exhibits saturation at sub 1 V drain bias with only about a factor of 2 loss in ON current compared to the ohmic contact.**

***Index Terms*—Indium gallium zinc oxide (IGZO), MOS devices, semiconductor devices, short channel, zinc oxide.**

I. INTRODUCTION

THIN Film Transistor (TFT) technology [1] allows the scalability and profitability for major manufacturing companies in today's consumer electronics market. One can find TFTs in TVs, [2] laptops, mobile phones, and wearable electronics, and recently it was suggested as a candidate for flexible CPUs [3]. Compared to a standard MOSFET process, the TFT architecture can be implemented with relative ease, making it an ideal candidate for the end of the process electronics or as a standalone technology. TFTs can be fabricated using silicon, amorphous silicon, amorphous metal oxide semiconductors (AOS), or organic materials [4]. Although each semiconductor material has its benefits, it is generally accepted that amorphous semiconductors lead to low-cost applications.

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The challenge with most amorphous semiconductors is that they do not lend themselves easily to both n- and p-type doping, thus not allowing for the standard MOSFET contacts, p-n diode, to be used for suppressing the OFF current. Two separate solutions were initially employed. First, instead of having a reverse p-n diode that becomes conductive following the channel inversion, a Schottky diode was used with a specific injection barrier that becomes significantly smaller following inversion [5]. Second, instead of relying on inversion, using undoped, de-doped, or intrinsic semiconductors allows for low OFF currents while accumulation achieves high ON currents. The second approach is primarily found in amorphous silicon [1] and organic semiconductors [6].

Today, the Schottky contact TFT architecture is known as the source gated transistor [7]–[9]. In parallel to this field, the Schottky barrier contact found its application also in short channel vertical organic FETs [10]–[14]. As both approaches rely on well-established physical phenomena, one can find detailed theoretical analysis of these structures [15]–[17]. Short channel transistors could suffer from a plethora of short channel effects such as drain-induced barrier lowering (DIBL), channel length modulation, hot carriers, and V_T shift (roll-off) [18]. Shannon and Gerstner [15] brought the context of Schottky contacts to short channel (lateral) transistors, keeping the output conductance low. Also, for vertical type FETs, which have an inherently short channel, an apparent saturation was reported only for a relatively high Schottky barrier [19].

The downside of making the injecting contact a Schottky type is that it comes at the expense of the ON currents' values limited by the Schottky barrier. The introduction of field relief plate in lateral FETs [8] or electric field shield in vertical ones [20] allows lifting the requirement for a high injection barrier. However, this method is most effective for lateral FETs of above micrometer channel lengths (2–4 μm in Sporea *et al.* [8]). Strategies for mitigation of short channel effects can also be found in CMOS technology. Still, the approach seems to modify the channel's edges and not modify the contacts [21]–[23].

Here, we suggest a new strategy which we term Double Injection Function (DIF) source electrode. Our new source electrode design allows high ON current while reducing

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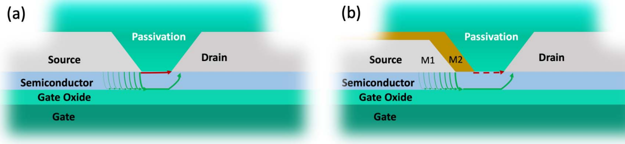

Fig. 1. Cross-sections showing the BGTC TFT layout of (a) traditional single metal electrode and (b) DIF source.

the short channel effects. Furthermore, we demonstrate a ∼200 nm channel length device using a single lithography step utilizing self-aligned angular deposition to control the device dimensions. In our design, we will make use of three primary contacts [5]. The first is the non-limiting or ohmic contact. The second is the Schottky contact exhibiting a high injection barrier. The third would be a tunneling contact, where with the aid of doping and applied bias, it may become almost non-limiting [5]. We expect our methodology to be important where scaling down [24] or over-scaling [25], [26] are not sufficient or not viable.

II. Architecture and Device Operation

Fig. 1 presents the layout of a traditional TFT [Fig. 1(a)] alongside that of the proposed DIF source electrode [Fig. 1(b)].

For traditional bottom gate top contact (BGTC) FET, Fig. 1(a), as the channel length is reduced, it reaches a point that the electric drain-field can directly extract charges from the source regardless of the gate. Fig. 1(a) illustrates the main current paths taken in a short-channel TFT device. The green arrows represent the preferred current path controlled by the gate, and the solid red arrow represents the parasitic leakage current between the source and drain. As mentioned earlier, one option to suppress the parasitic current is to increase the source injection barrier [15], [19]. However, in a high barrier configuration, the device current is limited by the reverse bias Schottky junction, thus significantly limiting the ON current.

The new architecture uses a DIF source electrode [Fig. 1(b)]. The edge of the source-electrode facing the drain-electrode is injection-limited while the rest of the source electrode is ohmic. In Fig. 1(b), we implement the DIF using a double work-function (DWF) approach. Here, M1 source metal (farthest from the drain) forms an ohmic contact to the semiconductor while M2 shields M1 and forms a Schottky contact. Fig. 1(b) illustrates the OFF current path by a dashed red arrow to denote the high injection barrier of M2 is limiting it. The green arrows mark the ON current path originating from the ohmic contact (M1) and flowing below M2, next to the insulator interface. Therefore, when the double work function transistor is at an OFF state, the high barrier source edge limits the parasitic leakage currents. On the other hand, when the transistor is at the ON state, carriers originating from the ohmic contact allow the high ON current.

III. Simulation

To understand how the new DIF source contact operates and compare it to traditional BGTC, we use the Synopsys 2-D TCAD simulation tool, Sentaurus. For the simulations to be relevant to the devices we fabricate, choosing the appropriate physical models and utilizing adequate values for the material's properties are essential. Hence, we use the semiconductor material parameters of indium gallium zinc oxide (IGZO). Since the properties of IGZO are sensitive to stoichiometry and general processing conditions, we had to extract or fit some of the parameters to the results of our fabrication process [27]. The methodology was first to fabricate and measure a 10 μm channel length TFT, having molybdenum ohmic contacts. Next, the measured characteristics were analyzed and then fitted using the Sentaurs TCAD simulation. The role of the numerical fitting was to allow us to better suggest relevant IGZO density of states. These would primarily be the tail states and the oxygen vacancies, as illustrated in Fig. 2. In Table I, we collate the complete list of the parameters we used.

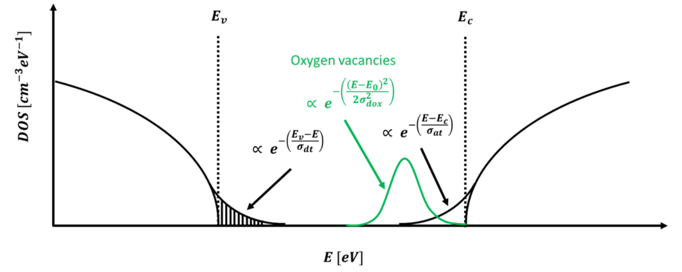

Fig. 2. Illustration of the simulated density of states distribution for the IGZO material.

TABLE I

IGZO Material Parameter List for TCAD Simulation (a) Literature Reported [29], (b) Measured, and (c) Fitted

Parameter symbol	Value
$q\chi\,[eV]$	4.16^a
$E_g[eV]$	3.2^a
$\mu_n[cm^2V^{-1}s^{-1}]$	1.5^b
ε_{IGZO}	10^a
$N_{dox}[cm^{-3}eV^{-1}]$	$2*10^{17c}$
$\sigma_{dox}[eV]$	0.12^c
$E_0[eV]$	4.36^c
$N_{dt}[cm^{-3}eV^{-1}]$	$1.55*10^{20a}$
$E_{dt}[eV]$	0.1^a
$N_{at}[cm^{-3}eV^{-1}]$	$1*10^{20c}$
$E_{at}[eV]$	0.1^a

In Table I, χ is the electron affinity, E_g is the electronic bandgap, μ_n is the electron mobility, and $\varepsilon_{\text{IGZO}}$ is the relative dielectric constant. The oxygen vacancies are considered as a Gaussian distribution of states. N_{dox}, σ_{ox}, and E_0 are oxygen-vacancy density, standard deviation, and central energy. The exponential band tails of the conduction (valence) band are characterized by the density N_{dt} (N_{at}) and tail parameter E_{dt} (E_{at}). Note that vacuum-deposited IGZO [28] and transistor made of, are superior to those we produced using the sol-gel method.

Using "our IGZO" parameters, we simulate the short channel performance of BGTC devices. Fig. 3 shows the

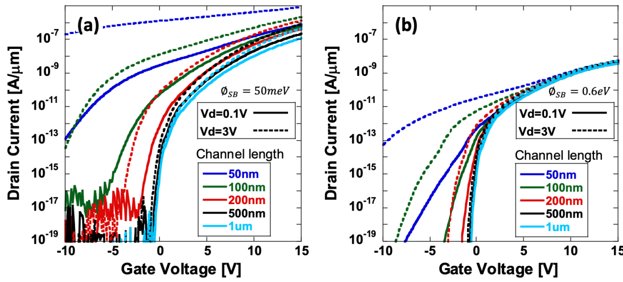

Fig. 3. Simulated Transfer characteristics on different channel lengths BGTC architecture for (a) Ohmic and (b) Schottky (0.6 eV barrier height) source contact. The current is normalized to the channel's width.

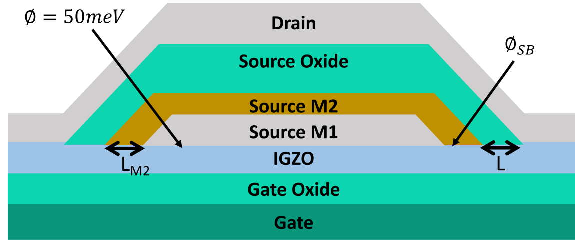

Fig. 4. Schematic of the layout of a double work function source transistor designed to be fabricated using a self-aligned method. Note the symmetric structure where the channel length is marked by L and the Schottky contact metal length is L_{M2}.

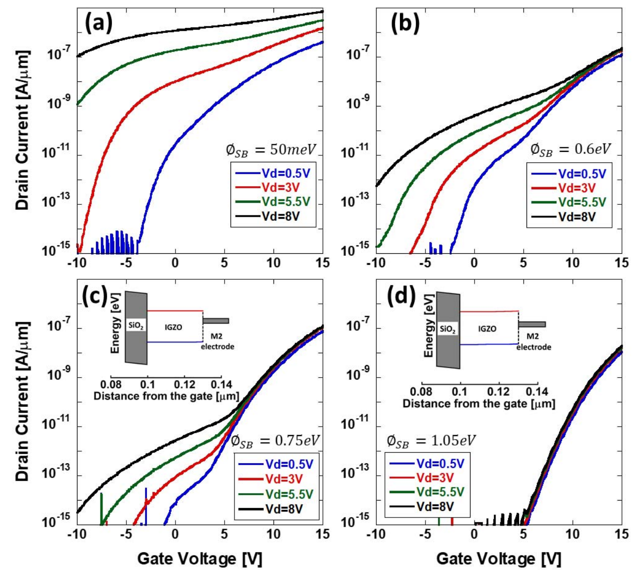

Fig. 5. Simulated transfer curves of DWF TFTs where $L = L_{m2} = 200$ nm and for M2 ϕ_{sb} being equal to (a) 50 meV, (b) 0.6 eV, (c) 0.75 eV, and (d) 1.05 eV. The current is normalized to the channel's width W. The inset of (c) and (d) shows the band diagram under M2 at $V_{gs} = 0$ V and $V_{ds} = 0.5$ V.

transfer characteristics of an Ohmic contact IGZO-based TFTs [Fig. 3(a)] compared to similar TFTs with a source Schottky barrier of 0.6 eV, i.e., source gated TFTs [Fig. 3(b)].

Fig. 3(a) shows that the IGZO TFT starts to suffer from short-channel effects once the channel length is reduced to below 0.5 μm. On the other hand, a 0.6 eV source contact barrier reduces the short channel effects [Fig. 3(b)]. At the ON state, the current is contact-limited and independent of the channel length. Also, the $V_d = 0.1$ V solid line and the $V_d = 3$ V dashed line overlap at the ON state. This overlap is the manifestation of the source gated transistors entering saturation in the output characteristics and at relatively low drain bias [7], [9]. However, at this barrier height (0.6 eV), the maximum current is already suppressed by two orders of magnitude, while the subthreshold slopes are still far from ideal. The motivation for the new design presented in Fig. 1(b) is defined above. We propose using source contact such that part of it forms an ohmic contact and the part facing the drain forms a high injection barrier. In Fig. 1(b), we implement the concept using two different metals, but other approaches as modifying the semiconductor [30], its surface [31], or interface [32] would also be valid options.

When choosing the representative structure to be simulated here, we opted for a design that suits the fabrication capabilities of our lab (more details in the experimental results). The device has a lateral symmetry where the source is in the middle and the drain is encompassing the source stack (Fig. 4). The bottom source metal (M1) forms an ohmic contact to the IGZO while the top source metal (M2) forms a Schottky contact. In this unique architecture, the high barrier metal covers the ohmic metal completely. Most importantly, it extends M1 toward the drain. The source dielectric, which physically separates the source and drain electrodes, defines the channel length. In the following, we would refer to the lateral M2 coverage length as L_{m2}, the lateral source dielectric coverage length as L, and the M2 metal energy barrier height for injection as ϕ_{sb}. Note that the structure symmetry creates transistors on both sides which are connected in parallel (i.e., W is doubled). Also, the drain and source oxide may act as a parasitic top gate which is minimized through the thickness and slope of the source oxide.

As mentioned earlier, in an ideal double work function TFT, the high barrier metal (M2) has to limit the number of charges at the interface with the IGZO (i.e., create depletion) and serve as a termination point for the drain electric field (i.e., provide a shield for M1). Additionally, the low injection barrier of M1 is such that it will not limit the current and thus allow for a high ON current.

To examine the effect of having a double work function, we plot in Fig. 5 the transfer characteristics of a series of TFTs where the injection barrier of M2 varies between $\phi_{sb} = 50$ meV and $\phi_{sb} = 1.05$ eV. The injection barrier of M1 is fixed at 50 meV (i.e., ohmic).

In Fig. 5, different sub-figures show the effect of M2 injection barrier height (ϕ_{sb}) on the device characteristics. From (a) to (d), ϕ_{sb} increases, and the short channel effects weaken. For the relatively small barrier, Fig. 5(a) and (b), the results are similar to Fig. 3(a) and (b), respectively. Note that while in Fig. 3(b) the reduction of maximum current, at low V_d, was 10^2, and here, it is merely a factor of 2 [Fig. 5(b)]. Enhancing ϕ_{sb} to 1.05 eV so that the subthreshold slope is "fixed" too, the penalty in the ON current is only 10×.

To better understand the DWF operation mechanism, we re-examine Fig. 5(b) and (c). Two distinct features are identified, one governing the OFF currents and one controlling the ON

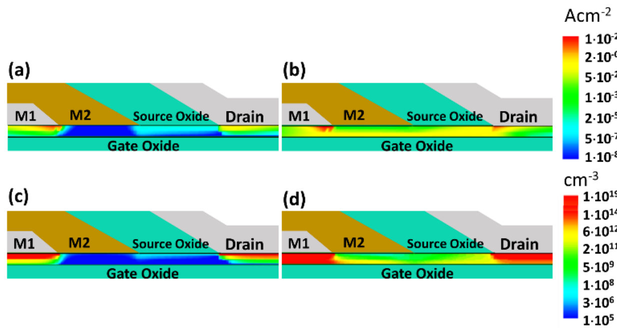

Fig. 6. (a) and (b) Current concentration and (c) and (d) electron density for gate bias of (a) and (c) $V_{gs} = -5$ V and (b) and (d) $V_{gs} = 7.5$ V. The applied drain bias and the source barrier were $V_{ds} = 5.5$ V and $\phi_{sb} = 0.75$ eV, respectively.

currents. Using the device parameters of Fig. 5(c), we examine the current and charge distribution for gate bias voltages of $V_{gs} = -5$ V and $V_{gs} = +7.5$ V. Fig. 6(a) and (b) present the current density distribution across the semiconductor layer.

In Fig. 6(a), OFF state, M2 metal creates a low-current region marked in dark blue. Visually, M2 blocks any current that might have been drawn from M1 by the drain. Moving to Fig. 6(b), ON state, the gate bias opens a channel below M2. Namely, the role of the gate is primarily to open and allow the current to penetrate the barrier imposed by M2. This mechanism marks the main difference between the known source gated transistor [7], [9] and the suggested DWF transistor. We do not limit the injection into the semiconductor, only what enters the channel.

Fig. 6(c) and (d) present the charge density distribution under the same working conditions as in Fig. 6(a) and (b). Examining the charge density and remembering that the background doping is $N_{dox} = 2 \times 10^{17}$ cm^{-3} (Table I), Fig. 6(c) directly shows the depletion formed under M2. The 0.75 eV barrier and the 30 nm layer thickness result in complete depletion of the layer underneath M2 (the dark blue region). At the ON state, Fig. 6(d), the channel forms and penetrates the depletion induced by M2. However, one can also spot a few non-idealities in the current distribution. For the OFF state, Fig. 6(a) and (c), we note an injection from the edge of M2 directly toward the edge of the drain electrode. In Fig. 6(c), the cyan streak extending across the channel and next to its top surface marks the direct injection from source to drain. This "current streak" is the source for the hump that dominates the OFF state in Fig. 5(c). As this "current streak," and associated hump, depends on the conductivity of the film's top, a lower residual doping could assist in suppressing it. Nevertheless, the higher injection barrier of Fig. 5(d) eliminates this "current streak." A direct comparison between Figs. 5(d) and 3(b) is not possible due to the structural differences between Figs. 4 and 1(b). The results in Fig. 5 also include the effect of the drain electrode being a parasitic top gate.

IV. Device Fabrication

Details of a similar process can be found in Sheleg and Tessler [33]. The fabrication starts with a p-doped silicon wafer having a 100 nm high quality thermally grown SiO_2 layer (4″, Nova electronic materials). The doped silicon served as the bottom gate and the SiO_2 as a gate insulator. The IGZO film was deposited by Sol-Gel solution using a procedure similar to Chen *et al.* [27]. The IGZO precursor was prepared by mixing 0.1 M zinc Nitrate Hydrate $(Zn(NO_3)_2 \cdot xH_2O)$, 0.1 M gallium(III) Nitrate Hydrate $(Ga(NO_3)_3 \cdot xH_2O)$, and 0.1 M indium(III) Nitrate Hydrate $(In(NO_3)_3 \cdot xH_2O)$ all in 2-Methoxyethanol (all IGZO precursor materials were purchased from Sigma Aldrich). The solution was left to stir overnight, followed by spin-coating at 3000 RPM for 30 s and a 150 °C drying step to yield ~5 nm-thick layer. The spin coat-dry sequence was repeated several times to achieve the required overall film thickness. Lastly, the sample was annealed at 350 °C for 3 h in ambient conditions and allowed to cool slowly to room temperature.

The IGZO-covered substrate was spin-coated with LOR resist and photoresist to use an overdeveloped pattern resulting in a mushroom-like cross-section profile. Then, the different source materials (metals and dielectric) were deposited at different angles relative to the mushroom profile to achieve the needed layer coverage. Next, the electrode was exposed using a lift-off technique and annealed at 350 °C in ambient conditions. Then, the top silver drain metal was deposited using a thermal evaporator through a shadow mask to complete the device with no post-metal deposition annealing step to limit oxygen diffusion and oxidation of the drain electrode. In a top view, the source and drain electrodes are deposited at 90 °C to facilitate contact outside the transistor area. The overall channel length realized was approximately 200 nm.

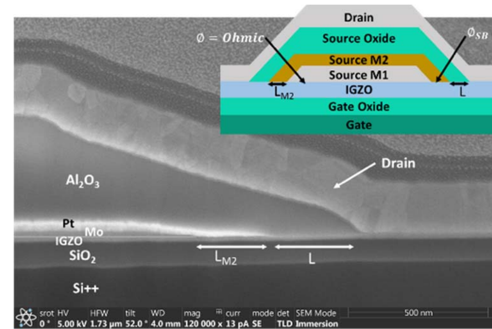

Fig. 7. DWF-TFT cross-section FIB image.

V. Experimental Results and Discussion

To set the scene, we show in Fig. 7 a cross-section SEM-FIB image focused on the right side of the symmetric design presented as an inset (Fig. 4). The FIB image shows the IGZO film on top of the Si/SiO_2 substrate. The source M1 metal is a 25 nm-thick molybdenum (Mo), and M2 is a 35 nm thick platinum (Pt). Lastly, the source dielectric is 400 nm Al_2O_3, and the top drain contact is silver (Ag).

Fig. 8 shows the electrical characteristics of transistors having molybdenum [Fig. 8(a) and (b)] and platinum [Fig. 8(c) and (d)] source contact.

Fig. 8(a) and (c), similar to Fig. 3(a) and (b), show the effect of Schottky contact in enhancing the subthreshold slope and reducing the apparent threshold (or on) voltage-shift (roll-off).

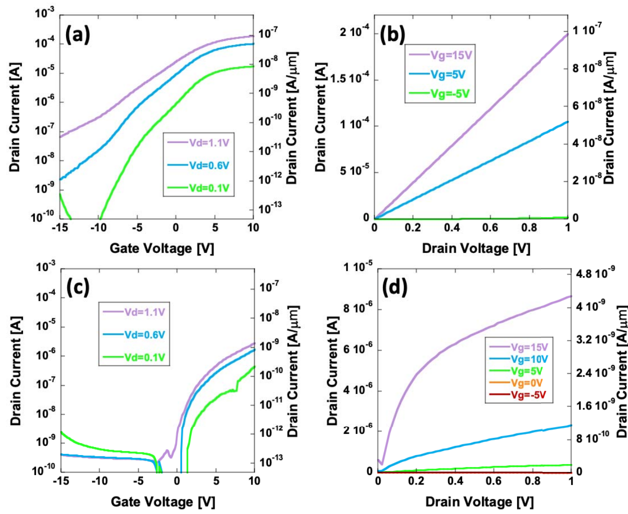

Fig. 8. Measured transfer and output characteristics with a single source metal (a) and (b) molybdenum and (c) and (d) platinum. The IGZO thickness is ~15 nm. Right axis-the current is normalized to the channel's width W = 2024 μm.

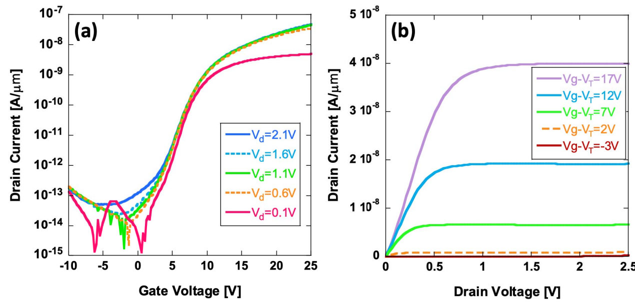

Fig. 9. (a) Transfer and (b) output characteristics of the Mo/Pt source contact. The IGZO is made from a 10 nm layer with a 70:15:15 metal atom ratio and a 20 nm layer with a 1:1:1 atom in the sol-gel solution. The current is normalized to the channel's width W = 2024 μm.

These results confirm that molybdenum and platinum are ohmic and Schottky contacts, respectively. Fig. 8(b) and (d) output characteristics illustrate the known source-gated transistor effect where the injection barrier promotes the appearance of saturation in the output characteristics of short-channel transistors. Please note the factor of 20 between the maximum currents of the molybdenum and platinum transistors.

Next, a combination of platinum on molybdenum source metal was fabricated in the proposed configuration (Fig. 7) with the same IGZO solution thickness and atom ratio. After detailed analysis using experiments and simulations, we concluded that when we deposit on the IGZO four different materials (molybdenum, platinum, alumina, and silver), we lose our ability to control the oxygen vacancies concentration in the IGZO film. As the entire DWF source electrode approach relies on controlling the depletion under the electrode, not controlling the vacancies (doping) makes it hopeless.

Raising the Ga content is known to enhance stability [32], [34] but also to reduce mobility. Hence, we adapted the multi-stack approach [34] employing 10 nm of (70:15:15) IGZO as the channel followed by 20 nm of (1:1:1) IGZO. Fig. 9 shows the characteristics of the multi-stacked DWF TFT.

Comparing Fig. 9 to Fig. 8(a) and (b), we note that the DWF (or DIF) structure loses less than an order of magnitude in current, compared to ohmic contact, while providing perfect saturation at low drain–source voltage.

VI. Conclusion

We have introduced a new thin-film transistor architecture that mitigates short channel effects and demonstrated it in solution-processed sol-gel IGZO BGTC TFT. The new design relies on a patterned source electrode such that the edge facing the drain is a Schottky contact while the rest is ohmic. Using simulations and experiments, we show systematically how the DIF operates. Specifically, Fig. 9 shows ideal output characteristics with saturation at drain voltages below 1 V. Moreover, compared to the ohmic contact device with no saturation [Fig. 8(a) and (b)], there is only about a factor of 2 loss in ON current. This loss is to be compared to known methods that would result in several orders of magnitude reduction in the ON current as a penalty for mitigating the short channel effects [15].

Acknowledgment

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