Compact Unipolar XNOR/XOR Circuit Using Multimodal Thin-Film Transistors

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***Abstract*— A novel compact realization of the XNOR/XOR function is demonstrated with multimodal transistors (MMTs). The multimodal thin-film transistors (MMT's) structure allows efficient use of layout area in an implementation optimized for unipolar thin-film transistor (TFT) technologies, which may serve as a multipurpose element for conventional and emerging large-area electronics. Microcrystalline silicon device fabrication is complemented by physical simulations.**

***Index Terms*— Digital circuits, layout optimization, microcrystalline silicon, multimodal transistor (MMT), physical simulation, Schottky barrier, thin-film transistor (TFT), XNOR, XOR.**

I. Introduction

XNOR and XOR are convenient for executing not only the identity operation, parity checking [1], encryption [2], and display control [3] but also computation, e.g., binary neural networks [4]. Beyond CMOS implementations [5], large-area electronic (LAE) circuit designers face additional challenges that retard progress in low-cost technologies [6]–[9]. As circuit failure increases with complexity and impacts yield [6], designs should be compact, comprising few thin-film transistors (TFTs), with robust operation that withstands imprecise fabrication [10], [11].

The XNOR function can be achieved in several ways (Table I), each with its own tradeoffs [5]. Using multiple control gates can enable logic at the device level [12], but requires ambipolar conduction, and is incompatible with low-cost, unipolar fabrication technologies. In TFT realizations, biasing devices deep into the OFF-state is problematic, due to either thin-film material ambipolarity or back-channel conduction, making elegant designs based on pass transistor logic [13] untenable. Many compact implementations rely on both the input signals and their complements, which add further complexity [5]. Approaches with monolithically integrated TFTs [14], [15] or incorporating other types of devices [15] complicate fabrication with additional processing steps.

Here, we show a TFT implementation of XNOR/XOR (Fig. 1) using multimodal transistors (MMTs) [16]. The device (Fig. 2) enables highly functional, compact circuits, due to the split control of charge injection and transport.

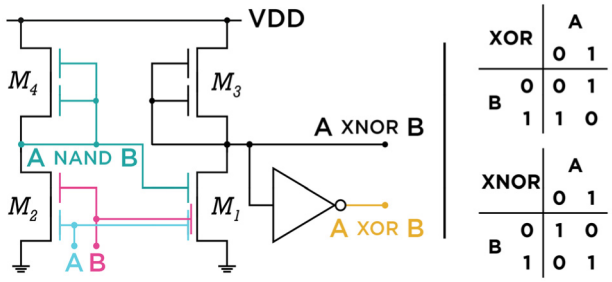

Fig. 1. Two-input XNOR and XOR function implementation using multimodal transistors (MMTs) M1 and M2 as inputs and zero-V_{GS} loads, M3 and M4. The respective truth tables are also shown.

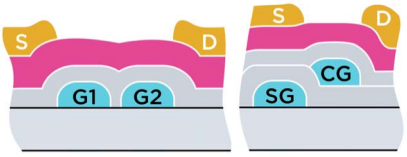

Fig. 2. Schematic of a two-input MMT device (left) and a TFT with two gates in series (right). Functionally, both devices perform the NAND function between their inputs (source control gate, SG, and channel control gate, CG for the MMT; and gates, G1 and G2, for the TFT), but the MMT enables more efficient use of layout area.

II. Multimodal Transistor Structure and Operation

By the introduction of an energy barrier engineered at the source contact, the MMT [16] separates its charge injection operation (modulated by a control gate that overlaps the source, SG) from channel transport (via the channel gate CG) (Fig. 2). MMTs can be realized in various material systems, including common unipolar semiconductors used in thin-film technologies.

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TABLE I
CIRCUIT ARCHITECTURES FOR IMPLEMENTING XNOR/XOR OPERATIONS

Reference	Number of devices (Core circuit)	Technology	Suitable for unipolar realization?	Clock/periphery circuits?	Additional information
Wang et al., 1994 [5]	4 – 6 MOSFETs	Si (CMOS)	No	No	Simulation only. 4T XNOR requires complementary signals and 2T driving output. 6T design does not require complementary signals.
Garg et al., 2020 [12]	1 TFET (4 gates)	Si	No	No	Simulation only. XNOR requires source-gate and drain-gate overlaps with different metal work functions. Prone to variability in overlaps and layer thicknesses.
Marcović et al., 2000 [13]	2 – 4 MOSFETs	Si (CMOS)	No	No	Synthesis of pass-transistor logic. No simulation or measurement.
Kwon et al., 2019 [14]	12 x OTFTs (24 gates) for XOR	OSC (monolithic integration)	No	No	Complicated process with n-type and p-type OSC used for complementary OTFT function. Device count for XNOR undisclosed.
Wu et al., 2020 [15]	2 TFTs, 2 RRAMs	IGZO (monolithic integration)	Yes	Discrete components used: 3 resistors, 2 capacitors, 3 ICs	Complicated process with additional devices stacked in 3D and rotated by 90 °.
This work	**2 MMTs (5 gates) – simulation 3 MMTs (6 gates) – measured**	**μ-Si**	**Yes**	**Simulation: 3 zero-V_{GS} MMTs as active loads Measurement: 2 load resistors for XNOR.**	**Devices fabricated in standard process. MMTs offer unipolar conduction due to source energy barrier.**

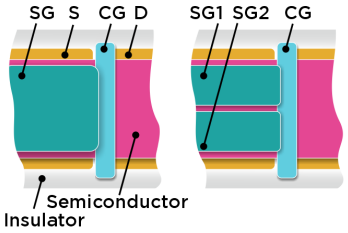

Fig. 3. Schematic top views of MMT devices with a single source control gate (left) and with two source control gates, SG1 and SG2, in parallel (right).

Although mainly benefitting analog design, the MMT also offers advantages for digital circuits, most notably robust performance in a minimal layout [16]. By the placement of SG vertically over the source, the area occupied is minimized when compared with a conventional TFT with two inputs in series (Fig. 2). The MMT can also have multiple source control gates (SG*n*) in parallel (Fig. 3), further augmenting functionality. In designing the transistor, care is required in establishing the relative positions of the gates, to ensure that the source is not under the influence of electric field from CG, as this would result in unwanted crosstalk between the two inputs (see [16] and its Supplementary Material).

Typical MMT functionality is illustrated by the transfer characteristics in Fig. 4, taken by varying the applied voltage to SG and CG, respectively. SG modulates the charge injection process through its overlap of the source electrode [17], [18]. The energy barrier deliberately introduced at the source ensures source-side pinch-off of the accumulated channel, leading to saturation at low drain voltages and flat output characteristics, in a manner similar to source-gated transistors [11], [19], [20]. The source barrier also ensures

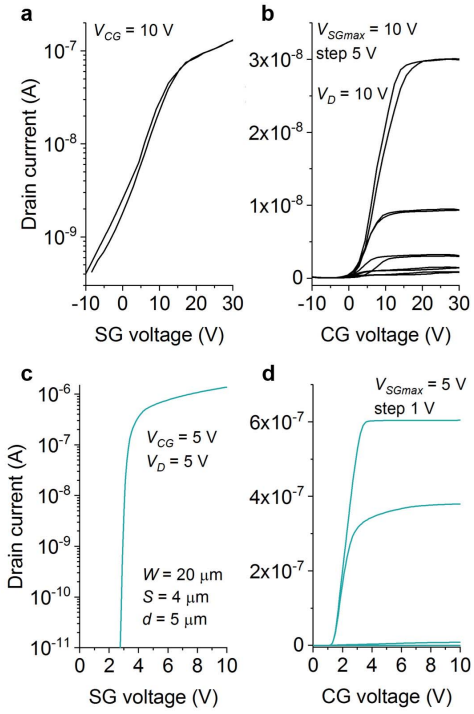

Fig. 4. (a) and (b) Measured (forward and reverse scans) and (c) and (d) simulated MMT transfer curves plotted against (a) and (c) SG voltage and (b) and (d) CG voltage.

that the source contact region is responsible for controlling the magnitude of the drain current, in contrast to a conventional TFT, in which this role is exclusively attributed to the channel region. CG voltage application then simply toggles the ON-OFF state of conduction of the channel, so that when sufficiently

accumulated, the current of a magnitude determined by SG can flow to the drain. Hence, the CG transfer characteristics plateau when the channel becomes less resistive than the source injection area (see transfer curves in Fig. 4). For analog control, CG acts as an enable function in series with the analog signal. In logic applications, the inputs to SG or CG can operate as being in series; if either one is in its OFF-state [21], the device will produce no drain current, performing the NAND function when connected to a resistive load.

III. Device Simulation and Fabrication

A. MMT Device and xnor Circuit Simulation

Amorphous silicon (a-Si) top gate MMTs were simulated as a proof of concept using Silvaco Atlas TCAD v.5.24.1.R and default material parameters. SG and CG are at the same vertical distance from the semiconductor (gate oxide thickness $t_i = 40$ nm) and are separated by a 1 μm gap. An overhang on SG was included to ensure the electric field created a continuous accumulation layer for charges to flow. Furthermore, the dimensions include: source SG overlap $S = 4$ μm; source–drain separation $d = 5$ μm; and semiconductor thickness $t_s = 40$ nm. The CG length was 4 μm and self-aligned to the drain. A Schottky barrier was defined for the source by setting its work function $WF = 4.67$ eV with barrier-lowering parameter $\alpha = 4$ nm. *Al* was set for drain and gate metals with 3×10^{20} cm^2 n-type doping under the drain to form an ohmic contact. The width ratio between the drive and load transistors, W_{M1-M2}/W_{M3-M4}, was 20. See [16] for complete simulation parameters, including common unipolar semiconductors used in thin-film technologies.

The circuit (Fig. 1) was simulated using Silvaco's mixed-mode capability, which allows exploring the device behavior in a circuit when no SPICE model exists. For M1, two parallel MMTs half as the width of M2 was used, as the simulation structures are 2-D. The inverter was created using an additional two-MMT inverter stage for the purpose of this functional demonstration.

B. MMT and xnor Circuit Fabrication and Measurement

A Corial 210D system was used for fabricating initial MMT prototypes in a mature, low-temperature (<200 °C) inductively coupled plasma chemical vapor deposition (ICP-CVD) microcrystalline Si (μ-Si) technology. The equipment can perform all process steps (including deposition and etching), for rapid small-scale prototyping. Staggered, bottom-gate MMTs included separate patterning of each gate layer, starting with SG. Both *Al* gate steps were followed by 100 nm SiO_2 gate insulator layers. Following the 40 nm μ-Si, a 20 nm field plate insulator was deposited. The contact window was defined by etching, and Cr was used to create the Schottky source and drain contacts. See [16] for the full process.

MMT XNOR circuits were created by wire-bonding three MMTs (Fig. 5) using a West Bond 7476E with Al thread and load resistances, $R_L = 500$ MΩ. Electrical characterization used a Wentworth probe station connected to two Keysight B2902A source/measure units (SMUs).

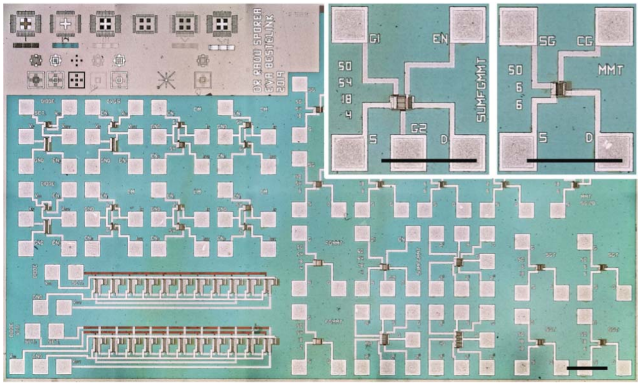

Fig. 5. Micrograph of fabricated microcrystalline MMT devices and circuits. Inset: individual MMT devices with single device (MMT) and two source control gates (SUMFGMMT). The latter contains a floating gate and a much thicker total gate insulator. Hence, in the present study, three conventional MMT devices have been used to realize the circuit. Scale bars: 500 μm.

IV. Circuit Operation

The core function of the circuit is realized by transistors M1 and M2 and their pull-up resistors (1). The two inputs are fed in parallel to SGs of M1, which thus performs the OR operation. M2 produces the NAND operation between the two inputs, A and B, and this is used to gate the signal generated by M1. Finally, M1's connection to R_L inverts the output.

$$\begin{aligned} A \text{ XNOR } B &= (A \cdot B) + (\overline{A} \cdot \overline{B}) \\ &\equiv (A \cdot B) + \overline{(A + B)} \\ &\equiv \overline{(A + B) \cdot \overline{(A \cdot B)}} \end{aligned} \tag{1}$$

The XOR function can be trivially obtained by negating the drain voltage of M1 (2)

$$A \text{XOR} B = \overline{A \text{XNOR} B}. \tag{2}$$

V. Results

We have focused here on qualitatively demonstrating logic functionality which takes direct advantage of the MMT's features and operation. Trivial functions, such as NOT (SG and CG connected together as input, or SG/CG as input with CG/SG connected to the rail), NAND-2 (two inputs applied on SG and CG, respectively), and NOR-*n* (*n* inputs connected to SG*n* with CG to the rail), are of course possible and are comprised within the operation of the XNOR/XOR circuit.

Fig. 6 shows the simulated and measured behavior of the MMT-based XNOR circuit. This functional demonstration shows the quasi-static operation as an identity function, i.e., the output is true when inputs have the same value.

While our measured demonstrator used external pull-up resistors, practical implementations would likely include active loads, which can easily be implemented as layout-efficient zero-V_{GS} devices, where the technology permits [22]. The unipolar (in this case only n-type) nature of the realization increases the circuit's relevance to many thin-film material systems. It does, however, lead to static power dissipation (on the order of ~100 nW per branch for this technology and geometry) when transistors M1 or M2 are on, but in operation,

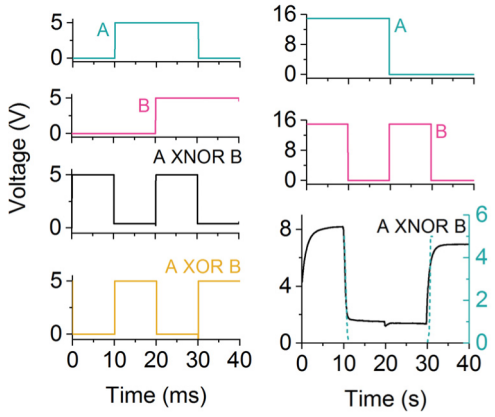

Fig. 6. Simulated (left) and measured (right) waveforms for the MMT-based unipolar XNOR circuit. The dotted line shows the simulated transient behavior obtained for an *RC* constant equivalent to that of the fabricated circuit and dc probing setup.

only one of the two branches of the circuit may be conducting at one time.

VI. Discussion

A. Limitations of the Fabricated Circuit

The measured waveforms fall short of the simulated behavior in both transient response and steady-state output voltage level. The discrepancies are explained by the modest electrical characteristics of these initial prototype MMTs.

First, the measured circuit uses significantly higher supply and input voltages. Referring to Fig. 4, it is apparent that the subthreshold swing of the fabricated devices is, at approximately 8 V/decade, far higher than what would be expected in an optimized a-Si, μ-Si, LTPS, or oxide technology.

Second, for an input voltage range of 0–16 V, the output of the measured circuit only swings between 2 and 8 V. Both values are a consequence of the limitations exhibited by the transfer characteristics. As SG voltage increases from 0 to 16 V, the output current rises from ~2 to ~60 nA. As such, for a constant value pull-up resistor, the output voltage swing is severely limited. Increasing the load resistance would allow the output node to approach the negative rail when the transistor (e.g., M1) is fully on, but the same load resistor would create a large voltage drop due to the comparatively large OFF-current when M1 is not conducting, leading to an unsatisfactory logic "1" voltage level. An improved subthreshold swing and a larger on/off ratio would permit a much wider output swing.

A related non-ideality is seen in the different voltage levels attained at the output in the two conditions of logic "1" state. When both inputs are high, CG of M1 is pulled low by M2, which is turned on. M1 will pass an OFF-current limited by CG. Conversely, when the two inputs are in logic "0" state, CG of M1 is pulled high by M4 (as M2 is off). In this condition, M1 will also be off, but its leakage current will be limited by SG. The marginally different OFF-current obtained when M1 is turned off, by either CG or SG, is responsible for the discrepancy in output voltage. Naturally, if the on/off ratio of the MMT is increased, e.g., beyond three orders for both CG and SG, this discrepancy will be insignificant even if it persists. Our previous work shows that MMTs realized in the same process can indeed operate with a much higher ON/OFF ratio [16].

Turning our attention to the dynamic characteristics, the measured waveforms show a much larger time constant than the simulated ones. Our intention here was to show the qualitative behavior of the circuit. Hence, the wire-bonding and probing approaches we have used are well-suited for d.c. measurements, but not for studying transients. The low transconductance (tens of nA) and high load resistance ($5 \times 10^8\ \Omega$) directly lead to low transit frequencies in these devices. From the rise and fall times in Fig. 6, we can estimate a capacitance of ~1–3 nF at the output node of the circuit. This is plausible given the setup we have used (d.c. probes, SSMA cables, long BNC cables, breadboard for wiring the load circuit, SMU). In a practical circuit, the load capacitance at the output will depend on the interconnect and fan-out requirements, but it may reasonably be estimated in hundreds of fF for such technologies, allowing us to conclude that operation close to the kHz range would be practical, even at these reduced current levels. The simulated circuit drove a single inverter (used to produce the A XOR B signal), and transistors, e.g., M1, were ~20 times more powerful, yielding rise and fall times of 10.7 and 3.97 μs, respectively, for a practical switching speed in the range of 20 kHz. By adding a 40 nF load capacitor, we obtain an *RC* product roughly similar to that of the fabricated circuit, and the simulated transients closely match the measured waveforms (Fig. 6, dashed line).

B. Considerations for Logic Function Implementations With MMTs

The MMT architecture allows efficient use of the device layout by stacking the SG input(s) in the source area. This compact design inherits the traits of the source-gated transistor (SGT) being also highly robust against process variations and bias stress [10], [16], [23].

Using two distinct mechanisms to turn on the device (injection control via SG and transport control via CG), the MMT can operate at lower input voltages than two conventional TFT channels controlled in series (Fig. 2). Together with the low saturation voltage of such devices, it is conceivable that such logic gates would operate with a sizeable noise margin [11], [24].

There is an obvious trade-off between: fabrication technology complexity and cost; circuit area; speed; and power dissipation [5]. Our implementation is thus well-suited to low-frequency, low-cost techniques in which fabrication yield and layout area are the principal concerns [6]. Moreover, the versatility of the MMT permits facile integration of several analog and digital functions, including signal amplification and conversion in highly compact circuit blocks [16], [25]. A typical application would be in distributed LAE sensor systems, in which local decision and signal conditioning are essential for conserving energy and communication bandwidth. The equivalence operation (XNOR) may be performed for understanding the correlation of several sensed quantities

and for activation of subsequent processes. In the biological or physiological domain, such markers would be evolving extremely slowly, and thus sub-μW circuits with very low bandwidth would be appropriate.

VII. Conclusion

We have implemented the XNOR function using unipolar, multimodal TFTs. The circuit requires few components and takes advantage of the MMT's construction, resulting in a compact layout, applicable to numerous TFT technologies. This digital circuit complements the valuable analog functionality of the MMT, with an outlook to efficient signal conditioning and decision implementation for cost-effective, distributed, and disposable sensors.

Acknowledgment

Devices were fabricated on the NanoRennes platform.

References

[1] B. Li, M. Yang, S. Mohajer, W. Qian, and D. J. Lilja, "Tier-code: An XOR-based raid-6 code with improved write and degraded-mode read performance," in *Proc. IEEE Int. Conf. Netw., Archit. Storage (NAS)*, Oct. 2018, pp. 1–10, doi: 10.1109/NAS.2018.8515729.

[2] X. Wu and W. Sun, "Extended capabilities for XOR-based visual cryptography," *IEEE Trans. Inf. Forensics Security*, vol. 9, no. 10, pp. 1592–1605, Oct. 2014, doi: 10.1109/TIFS.2014.2346014.

[3] B.-D. Choi and E.-S. Kim, "Counting-based digital-to-analog converter scheme for compact column driver with low-temperature polycrystalline silicon thin-film transistors," *Jpn. J. Appl. Phys.*, vol. 47, no. 3, pp. 1906–1912, Mar. 2008, doi: 10.1143/JJAP.47.1906.

[4] E. Ozer *et al.*, "Binary neural network as a flexible integrated circuit for odour classification," in *Proc. IEEE Int. Conf. Flexible Printable Sensors Syst. (FLEPS)*, Aug. 2020, pp. 20–23, doi: 10.1109/FLEPS49123.2020.9239529.

[5] J.-M. Wang, S.-C. Fang, and W.-S. Feng, "New efficient designs for XOR and XNOR functions on the transistor level," *IEEE J. Solid-State Circuits*, vol. 29, no. 7, pp. 780–786, Jul. 1994, doi: 10.1109/4.303715.

[6] A. F. Paterson and T. D. Anthopoulos, "Enabling thin-film transistor technologies and the device metrics that matter," *Nature Commun.*, vol. 9, no. 1, pp. 1–4, Dec. 2018, doi: 10.1038/s41467-018-07424-2.

[7] J. Noh, M. Jung, Y. Jung, C. Yeom, M. Pyo, and G. Cho, "Key issues with printed flexible thin film transistors and their application in disposable RF sensors," *Proc. IEEE*, vol. 103, no. 4, pp. 554–566, Apr. 2015, doi: 10.1109/JPROC.2015.2410303.

[8] R. D. Bringans and J. Veres, "Challenges and opportunities in flexible electronics," in *IEDM Tech. Dig.*, Feb. 2016, pp. 1–2, doi: 10.1109/IEDM.2016.7838361.

[9] Y. Qu *et al.*, "Organic and inorganic passivation of p-type SnO thin-film transistors with different active layer thicknesses," *Semicond. Sci. Technol.*, vol. 33, May 2018, Art. no. 075001, doi: 10.1088/1361-6641/aac3c4.

[10] R. A. Sporea, A. S. Alshammari, S. Georgakopoulos, J. Underwood, M. Shkunov, and S. R. P. Silva, "Micron-scale inkjet-assisted digital lithography for large-area flexible electronics," in *Proc. Eur. Solid-State Device Res. Conf. (ESSDERC)*, Sep. 2013, pp. 280–283, doi: 10.1109/ESSDERC.2013.6818873.

[11] R. A. Sporea, M. J. Trainor, N. D. Young, J. M. Shannon, and S. R. P. Silva, "Source-gated transistors for order-of-magnitude performance improvements in thin-film digital circuits," *Sci. Rep.*, vol. 4, no. 1, pp. 1–7, Mar. 2014, doi: 10.1038/srep04295.

[12] S. Garg and S. Saurabh, "Realizing XOR and XNOR functions using tunnel field-effect transistors," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 1001–1009, Sep. 2020, doi: 10.1109/JEDS.2020.3025266.

[13] D. Marković, B. Nikolić, and V. G. Oklobdžija, "General method in synthesis of pass-transistor circuits," *Microelectron. J.*, vol. 31, nos. 11–12, pp. 991–998, Dec. 2000, doi: 10.1016/S0026-2692(00)00088-4.

[14] J. Kwon, Y. Takeda, R. Shiwaku, S. Tokito, K. Cho, and S. Jung, "Three-dimensional monolithic integration in flexible printed organic transistors," *Nature Commun.*, vol. 10, no. 1, pp. 1–10, Jan. 2019, doi: 10.1038/s41467-018-07904-5.

[15] J. Wu, F. Mo, T. Saraya, T. Hiramoto, and M. Kobayashi, "A monolithic 3D integration of RRAM array with oxide semiconductor FET for in-memory computing in quantized neural network AI applications," *IEEE Trans. Electron Devices*, vol. 67, no. 12, pp. 5322–5328, Dec. 2020, doi: 10.1109/VLSITechnology18217.2020.9265062.

[16] E. Bestelink, O. de Sagazan, L. Motte, B. Schultes, S. R. P. Silva, and R. A. Sporea, "Versatile thin-film transistor with independent control of charge injection and transport," *Adv. Intell. Syst.*, vol. 3, no. 1, Oct. 2020, Art. no. 2000199, doi: 10.1002/aisy.202000199.

[17] J. M. Shannon, R. A. Sporea, S. Georgakopoulos, M. Shkunov, and S. R. P. Silva, "Low-field behavior of source-gated transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 8, pp. 2444–2449, Aug. 2013, doi: 10.1109/TED.2013.2264547.

[18] A. Valletta, L. Mariucci, M. Rapisarda, and G. Fortunato, "Principle of operation and modeling of source-gated transistors," *J. Appl. Phys.*, vol. 114, no. 6, Aug. 2013, Art. no. 064501, doi: 10.1063/1.4817502.

[19] R. A. Sporea and S. R. P. Silva, "Design considerations for the source region of Schottky-barrier source-gated transistors," in *Proc. Int. Semiconductor Conf. (CAS)*, Oct. 2017, pp. 155–158, doi: 10.1109/SMICND.2017.8101185.

[20] J. Zhang *et al.*, "Extremely high-gain source-gated transistors," *Proc. Nat. Acad. Sci. USA*, vol. 116, no. 11, pp. 4843–4848, Mar. 2019, doi: 10.1073/pnas.1820756116.

[21] E. Bestelink, T. Landers, and R. A. Sporea, "Turn-off mechanisms in thin-film source-gated transistors with applications to power devices and rectification," *Appl. Phys. Lett.*, vol. 114, no. 18, pp. 1–4, May 2019, doi: 10.1063/1.5088681.

[22] E. Bestelink *et al.*, "Compact source-gated transistor analog circuits for ubiquitous sensors," *IEEE Sensors J.*, vol. 20, no. 24, pp. 1–11, Jul. 2020, doi: 10.1109/jsen.2020.3012413.

[23] J. M. Shannon, "Stable transistors in hydrogenated amorphous silicon," *Appl. Phys. Lett.*, vol. 85, no. 2, pp. 326–328, Jul. 2004, doi: 10.1063/1.1772518.

[24] Q. Cui, M. Si, R. A. Sporea, and X. Guo, "Simple noise margin model for optimal design of unipolar thin-film transistor logic circuits," *IEEE Trans. Electron Devices*, vol. 60, no. 5, pp. 1782–1785, May 2013, doi: 10.1109/TED.2013.2251346.

[25] E. Bestelink, O. de Sagazan, and R. A. Sporea, "P-18: Ultra-compact multi-level digital-to-analog converter based on linear multimodal thin-film transistors," in *SID Symp. Dig. Tech. Papers*, Aug. 2020, vol. 51, no. 1, pp. 1375–1378, doi: 10.1002/sdtp.14141.