Analysis of Current Capability of SiC Power MOSFETs Under Avalanche Conditions

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***Abstract*— The phenomenon of reduced energy capability of power metal–oxide–semiconductor field-effect transistors (MOSFETs) at high avalanche currents is investigated in commercial 1.2-kV 4H-SiC MOSFETs. Unclamped inductive switching (UIS) measurements as well as electrical transport simulations are used to identify the current paths and maximum avalanche currents, providing insight into the design limits. The investigated devices show a reduced energy capability for avalanche current above 52 A due to the latching of the parasitic bipolar junction transistor (BJT). The BJT also limits the maximum switchable current to $\leq$102 A. Based on the measurements and simulations, a procedure utilizing UIS measurements for identification of design limits is presented.**

***Index Terms*— Avalanche, reliability, robustness, silicon carbide, thermal runaway.**

I. Introduction

POWER metal–oxide–semiconductor field-effect transistors (MOSFETs) undergo avalanche generation when switching in the presence of parasitic inductances [1]. However, avalanche multiplication has a positive temperature coefficient and, therefore, can only lead to runaway when a secondary mechanism with a negative temperature coefficient (NTC) dominates. The secondary mechanism can be due to the limitation of the material, such as reaching intrinsic temperature, or due to a significant leakage through the gate dielectric. It can also occur when the parasitic bipolar junction transistor (BJT) latches [2]–[7]. Furthermore, in Si IGBTs, it has been demonstrated that filamentation may occur, where the filament will be pinned to field crowding areas of the parasitic BJTs [8].

Research has demonstrated such failures limiting the avalanche current capability in silicon IGBTs using simulations [6], [8] as well as unclamped inductive switching (UIS) measurements [9]. In Si MOSFETs, trench gate [10], [11] and L-shaped structures [12] were investigated and showed a trade-off between cell design parameter variations and avalanche current capability. Thus, avalanche current capability tests can be used as feedback for the design and optimization of robust devices. For such purposes, analytical models for simpler structures of silicon power diodes were developed [13]. However, reliable models for three-terminal devices are still not available.

Compared to Si, 4H-SiC has a higher intrinsic temperature (T_{int}) and heat capacitance [5], [14]–[16] and, therefore, a larger margin before reaching thermal runaway [17]. This makes secondary mechanisms, such as the BJT, viable failure processes to consider during device design.

Studies to understand the limits of avalanche ruggedness in 4H-SiC use 1-D thermal models to estimate the junction temperature [5], calculate threshold voltage reductions [1], as well as perform postfailure device decapsulation [1], [18]–[20]. However, accurate experimental procedures for distinguishing the mechanisms that limit the avalanche current capability of 4H-SiC power MOSFETs have not been presented.

This work uses a systematic approach to understand the current path during avalanche. The dynamics of the current path is shown via simulation and its effect on avalanche ruggedness is discussed. A suggestion for a fast assessment of reliability of the devices and for establishing a safe operating area (SOA) for avalanche mechanisms is presented. As devices under test (DUTs), commercial 1.2-kV 80-mΩ power MOSFETs from Wolfspeed are used [21].

In Section II, experimental testing of destructive UIS is used to demonstrate the avalanche current limit of the MOSFETs. This is supplemented by simulations of avalanche breakdown in Section III to show how the BJT current evolves with temperature becoming the limiting mechanism. In Section III-B, 2-D electrothermal simulations of inductive switching are presented and the critical conditions for thermal runaway are discussed.

II. Avalanche Current Capability Tests

Destructive UIS tests are performed on 1.2-kV, 80-mΩ rated C2M0080120D devices from Wolfspeed [21]. A test circuit as shown in the inset of Fig. 1 is used for this experiment. This test setup includes a load inductor in series with the DUT. A capacitor bank is initially charged to the target energy and is used to magnetize the inductor to the desired current value.

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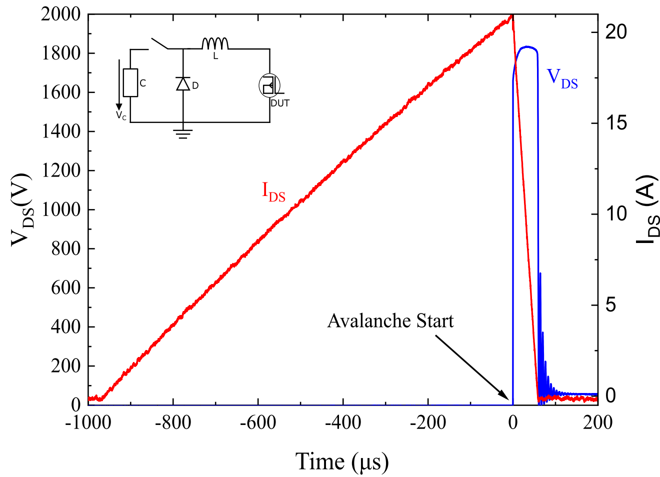

Fig. 1. UIS typical waveform and a UIS setup (inset).

It is then disconnected 2 μs before the gate of the DUT is turned off. When the gate is turned off, the inductor forces the MOSFET to supply a respective current by undergoing avalanche. The waveform for this test is shown in Fig. 1. The values of inductors used in this experiment are 0.25, 0.47, 1.47, 2.67, and 5.1 mH and the avalanche current, $I_{\mathbf{AV}}$, reaches values from 20 A to the maximum current at which the respective device fails. The energy dissipated on the device, $E_{\mathbf{AV}}$, is calculated from the time integral of power before failure.

Results of the UIS test are shown in Fig. 2. The maximum E_{AV} versus I_{AV} is shown where two distinct regions can be identified: up to $I_{\mathrm{AV}} \leq$ of 52 A, the maximum E_{AV} is independent of I_{AV} or the value of the inductance used. The simulated high lattice temperature reached in this condition is shown to be $\approx$1500 K. However, for I_{AV} above this value, energy dissipated on the DUTs decreases approximately linearly with current. It is also slightly lower for higher inductances. On the other hand, the duration of avalanche, t_{AV}, shown in Fig. 2(b), shows an exponential decrease with current. Due to nonhomogeneity of the devices, originating from process and manufacturing variability of commercial products, there is a slight variation in the specific values [22]–[24]. The difference in E_{AV} and the duration of avalanche, t_{AV}, between inductors in the second region is within the range of this experimental spread.

The linear decrease in E_{AV} continues until a maximum I_{AV} measured, above which the device fails during switching ($E_{\mathrm{crit}} = 0$ is 94–102 A).

III. Device Simulation

A. Isothermal Tests and Temperature-Dependent Parameters

Electrical transport simulations of a 4H-SiC power MOSFET are performed using Sentaurus device software from Synopsys [25]. 4H-SiC material parameters for the simulation are taken from advanced calibration of Sentaurus [25] unless otherwise stated. Anisotropy of 4H-SiC is implemented in solving Poisson, mobility, impact ionization, and thermal

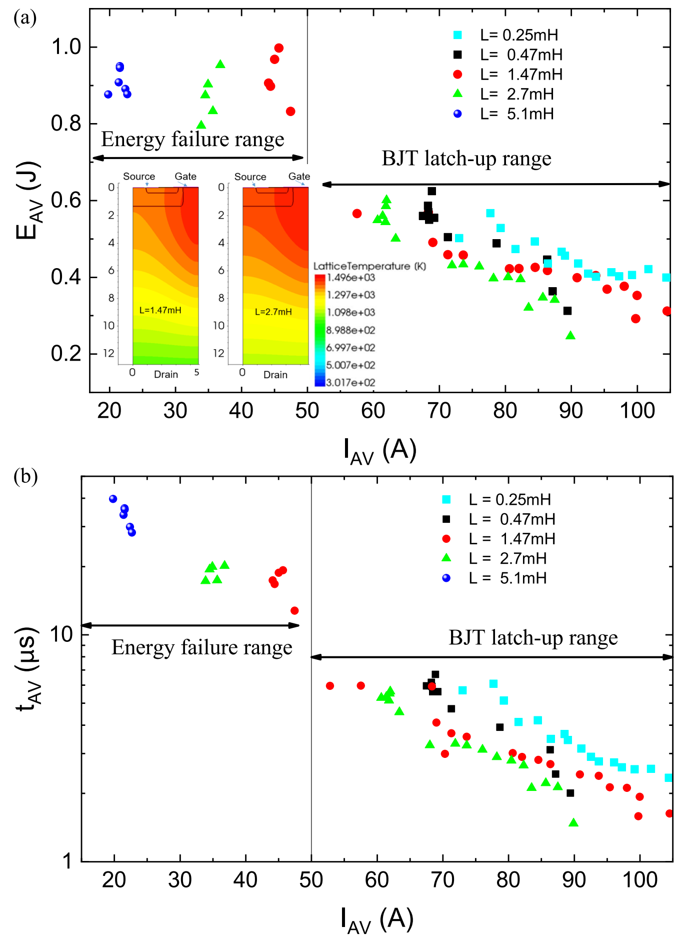

Fig. 2. (a) UIS experimental results of E_{AV} as a function of I_{AV} for various inductances. In the inset, the temperature distribution is shown. (b) Time in avalanche as a function of decreases exponentially with increase in I_{AV}.

conductivity equations in 4H-SiC. The device structure is optimized to fit the data sheet.

To understand the dynamics of the current path as a function of the current, independent of the self-heating phenomena, isothermal simulation of avalanche breakdown is first performed at 300 K [see Fig. 3]. The drain voltage is ramped to breakdown (V_{BR}) with the source and base grounded. The 2-D-current density plots are then analyzed to determine the dynamics of the current path as the avalanche-generated drain current increases.

The simulated current density plots are shown in Fig. 3(a) at different avalanche currents. At lower levels, current passes through the p-well (left panel). At higher drain current, injection from the source starts to increase (middle panel) and eventually dominates (right panel). This occurs when a large number of holes accumulate in front of the base region and recombine with the N-acceptor of the base, hence decreasing the potential difference. The electrostatic potential during this transition is shown in Fig. 3(b) and shows that at a drain current of 47 A at 300 K, the source-p-well barrier is overcome and electrons are injected from the source.

To perform simulations at higher temperatures, temperature-dependent transport models are implemented. These include

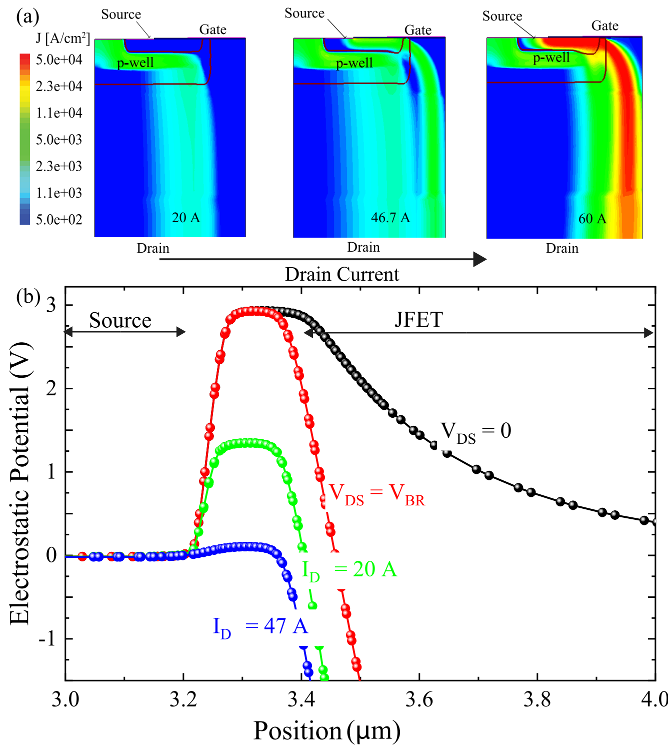

Fig. 3. (a) Current density distribution in a 4H-SiC MOSFET biased at V_{BR} showing the change in the current path with increasing magnitudes of drain current. The indicated junction line is not representative of the metallurgical junction, but an indication of the position of net-zero active carriers. (b) Electrostatic potential along the horizontal cross section near the top surface.

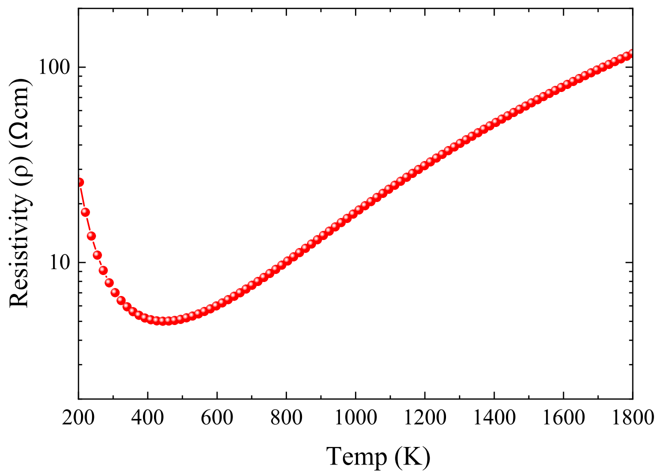

Fig. 4. 1-D model of resistivity of the p-well of the MOSFET showing resistivity increasing with temperature above 500 K.

temperature dependence of avalanche breakdown, which is simulated through the Okuto–Crowell model [26], [27], degradation of bulk mobility given by the Arora model [28], and temperature-dependent ionization of aluminum. The effect of these processes results in the temperature dependence of resistivity shown in Fig. 4.

Below ≈500 K, the resistivity decreases with temperature due to increasing ionization of aluminum [29]–[31]. Above

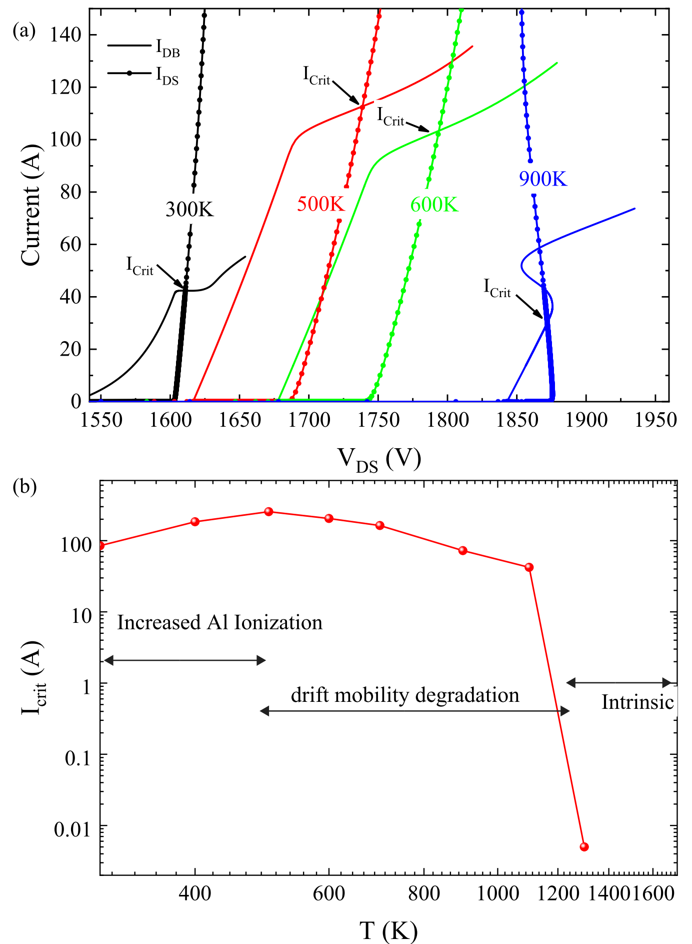

Fig. 5. (a) Avalanche current of a 4H-SiC power MOSFET at different temperatures showing the rise of I_{DB} at the onset of avalanche until injection from the source I_{DS} starts and rapidly dominates. (b) Evolution of I_{crit} with temperature and due to the different dominating mechanisms.

≈500 K, the dominating mechanism is drift mobility degradation, leading to increasing the resistivity.

Performing isothermal simulations for temperatures from 300 to 1500 K, the base (I_{DB}) and source currents (I_{DS}) are shown in Fig. 5(a) for selected temperatures. The drain current where the source starts to dominate ($I_{DS} = I_{DB}$) is extracted for each temperature and shown in Fig. 5(b). This avalanche current is referred to as the critical current threshold (I_{crit}) for latching the BJT. This current increases up to 500 K, due to the change in resistivity shown in Fig. 4. Above this current, the mobility degradation dominates.

B. Electrothermal Simulations

The influence of increased current and temperature is independently shown in the previous section. The combined effect that occurs during a real UIS under dc-link bias is investigated with electrothermal simulations. The test circuit used is shown in Fig. 6 (inset).

UIS tests are simulated charging a 0.47-mH load inductor to peak avalanche currents (I_{AV}) varying from 34 to 105 A. Simulated destructive and nondestructive UIS are shown in Fig. 6 for I_{AV} = 34 A and I_{AV} ≈ 105 A, respectively. The DUT

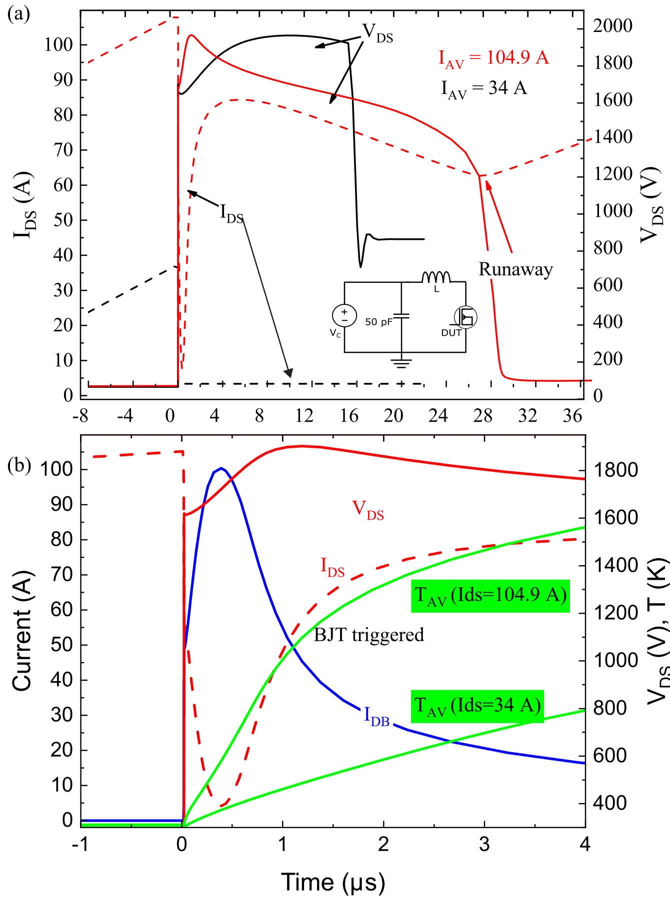

Fig. 6. (a) Electrothermal simulation of a UIS waveform of a 1.2-kV, 80-mΩ 4H-SiC vertical power MOSFET. Comparison of currents and voltages between I_{AV} of 34 A versus 105 A. (b) Zoomed-in plot (bottom) to show the BJT latching for a test at $I_{AV} = 105$ A. The device temperature during avalanche for I_{AV} of 34 and 105 A is shown.

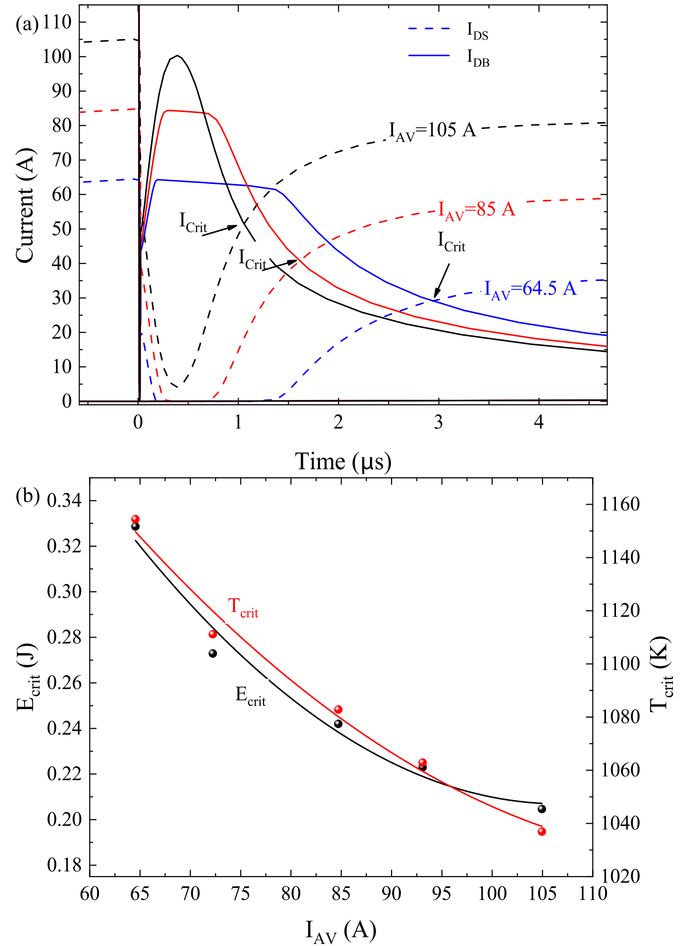

Fig. 7. (a) UIS simulations showing the BJT latching earlier (reaching I_{crit}) with increasing values of I_{AV}. Avalanche starts at 0 μs. (b) Energy dissipated at failure (E_{crit}) and the maximum junction temperature (T_{Max}) as a function of I_{AV} are shown for 0.47-mH inductance.

effectively dissipates and returns to preavalanche state at 34 A, where I_{DS} remains zero. For $I_{AV} \approx 105$ A, source injection increases sharply and subsequently surpasses the base current (I_{DB}) within approximately 1 μs (Fig. 6, lower panel). The temperature during this transient is also shown in this figure. Even though the temperature rises faster for $I_{AV} \approx 105$ A, it is still much lower than required for the intrinsic failure range ($T_{AV} \approx 1050$ K compared to T greater than 1500 K). The BJT is then triggered and the breakdown voltage drops.

Even though I_{DS} dominates at 1 μs, the simulation estimates runaway after 28 μs only, as the simulations in this study are performed for a single cell and assume uniformity across the entire structure. In real devices, material and fabrication nonhomogeneity between cells leads to hot spots and destructive failure due to the NTC of the BJT [3], [32]. Thus, the critical energy (E_{crit}) is defined in this work as the energy dissipated until I_{crit} is reached where the BJT current, I_{DS}, dominates. The temperature at which this occurs is defined as T_{crit}. Sensitivity to increasing avalanche current, in the simulations performed, the BJT does not latch for I_{AV} below 53 A. Above this value of current, the BJT latches within ≤ 5 μs. With increase in I_{AV}, the BJT latches faster, as shown in Fig. 7(a). The extracted values of E_{crit} and T_{crit} are shown in Fig. 7(b). E_{crit} and T_{crit} decrease with increased current, as high I_{DS} is leading to faster latching. Therefore, careful analysis of destructive UIS tests can identify the shortcomings of device design such as triggering BJT that leads to reduced energy capability [2], [4].

IV. Discussion

To accurately understand the capabilities of power MOSFETs under avalanche conditions, a simplified test is necessary to differentiate failure modes and identify whether the bottlenecks are related to the semiconductor, the dielectrics, or the metallization. For such purposes, understanding avalanche dynamics in 4H-SiC is important.

Avalanche processes dissipate a large amount of energy, which creates thermal stress ($\Delta T \propto (E)^{1/2}$) on the device [2]. Once the temperature reaches a critical value, T_{crit}, corresponding to an activation energy, E_{crit}, the device fails destructively. However, MOSFETs fail below the critical energy, in the presence of high current, when the parasitic BJT is triggered starting an NTC process [2], [3].

In this work, correct experimental design and understanding is provided to distinguish the two failure mechanisms. UIS

tests are used on C2M0080120D devices from Wolfspeed for this purpose. The use of destructive avalanche tests with increasing peak current gives a simplified and accurate analysis to understand failure mechanisms in 4H-SiC. UIS tests at a single peak current with varying inductance [10] can also be used. However, the measured influence of inductance in 4H-SiC is too small, as shown in Fig. 2, and thus, varying peak current provides better experimental resolution.

Results of UIS tests show that the devices in this study reached E_{crit} for avalanche currents below $I_{\text{AV}} \leq 52$ for the given test conditions. This is where the MOSFET has reached its peak temperature and thus dissipated maximal energy. This can be due to intrinsic temperature limit of 4H-SiC or thermal threshold of the gate oxide. Thus, the current capability of the device in this range is only a function of the load inductance showing low current capability for higher inductance. For inductance below 1.47 mH and current below 52 A, the device is avalanche capable.

For I_{AV} above this value, E_{AV} decreases approximately linearly with current as the BJT is triggered faster with increasing I_{AV}. In this case, E_{AV} remains below the critical value showing premature failure. In addition, this work shows that failure is not due to the displacement current as proposed in [12] or due to dV_{BR}/dT as is the case in power diodes [13]. Displacement current caused latching failure at switching only above $\approx$ 105 A in DUTs in this work. The measurements in this work, to the best of our knowledge, are the first to clearly distinguish the BJT latching from reaching the thermal threshold in 4H-SiC power MOSFETs. Previous UIS experiments in 4H-SiC MOSFETs [19] were not able to reach E_{crit} within their experimental boundary.

Simulations showed that even at 300 K, the parasitic BJT can be triggered if sufficient avalanche current is conducted through the device (see Fig. 3). The current path of this BJT is shown to be close to the MOSFET channel. This failure path was previously suspected to be thermal lowering of the MOSFET threshold [33]. However, in our prior works [34], we did not observe improvement in avalanche capability by biasing the gate at -10 V to inhibit the MOSFET channel from turning on. "The damage location" observed near the source metallization in posttest decapsulation in [5] is possibly due to the BJT injecting from the source at thermal runways.

Since the BJT latching becomes detrimental in the presence of manufacturing nonhomogeneity such as doping profile, designs that are rugged against these instabilities are necessary to improve reliability. These designs should eliminate the snapback of V_{BR} that occurs when the BJT latches. In this work, the simulated structure showed BJT latching above an $I_{\text{AV}} \approx 53$ A for 0.47 mH at dc-link bias and was experimentally found for I_{AV} above 52 A for 2.7 mH without the bias.

Either an oxide failure or reaching intrinsic temperature is responsible for failures below 52 A. Given that the oxide is exposed to high temperatures as well as a high channel current, oxide failure may be expected [35]. On the other hand, previous decapsulation experiments have shown failure locations to be uniformly distributed in the source metallization. Therefore, further tests that independently probe the oxide are required to confirm this hypothesis.

V. Conclusion

In this work, it is shown that thermal runaway can be rapidly triggered by temperature-induced latching of the parasitic BJT in vertical power MOSFETs. In C2M0080120D, the parasitic BJT is shown to be the bottleneck only above 52 A during avalanche conduction. Below 52 A, failure can occur either due to the gate-oxide leakage or intrinsic conduction. Destructive avalanche measurements and accompanying simulations can thus be used as fast feedback for checking the reliability of specific device architectures.

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