Modeling of Semiconductor Substrates for RF Applications: Part I—Static and Dynamic Physics of Carriers and Traps

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***Abstract*— This article aims to provide deep insight into the physics of substrates for RF applications under large-amplitude signal excitations. The impact of physical parameters on substrate-induced harmonic distortion is modeled and well understood, from a theoretical and quantitative standpoint. This article formulates the interplay between applied voltage signal (dc or RF), interface fixed charge, and trapped charge in a charge-balance analysis for high-resistivity and trap-rich (TR) substrates. A TCAD approach gives strong insight into the impact of such semiconductor material and interface properties on the RF substrate's effective resistivity and linearity. First, a static analysis reveals how TR interface passivation overcomes the parasitic surface conduction effect using the concept of deep Fermi-level pinning. Next, substrates are analyzed in response to dynamic excitation signals. Using step functions to pulse an MOS structure from strong negative to strong positive applied charge sheds light on carrier dynamics. The characteristic time constants associated with variations in trap occupancy and in free carrier densities are discussed. Finally, sinusoidal large-amplitude signals are considered to analyze harmonic distortion from several types of substrates at various RF frequencies.**

***Index Terms*— Carrier dynamics, coplanar waveguide (CPW) line, effective resistivity, Fermi-level pinning, harmonic distortion (HD), large-signal modeling, nonequilibrium, pulsed MOS, RF loss, RF substrate, TCAD modeling, trap-rich (TR) silicon-on-insulator (SOI).**

I. Introduction

SILICON-BASED technologies present a cost and volume-manufacturing advantage over other materials due to high-maturity processes available on 300-mm-diameter wafers. Today, the most advanced CMOS nodes, and in particular silicon-on-insulator (SOI) flavors, are boasting impressive RF figures of merit (FoMs), proposing an attractive path for cost-effective mass market productions of RF and mm-wave applications, including 5G, connected objects and smart sensors [Internet of Things (IoT)], and radars [1].

To enable advanced telecommunication schemes (4G, 5G, and so on), the aggregation of multiple frequency bands is employed in order to achieve high data throughput.

Circuit elements that behave in a nonlinear fashion are usually undesirable in a system chain, as they introduce signal distortion between the input and the output waveforms. In the frequency domain, this corresponds to a smearing of the spectral content, with distortion components being generated outside of the allocated band. Advanced telecommunication schemes have stringent linearity specifications [2]–[4], and this linearity burden is applied to all levels of the RF chip: from the active devices down to the substrate material [4].

Linearity and loss depend on the device performance but are also critically impacted by the substrate properties at RF. For these reasons (among others), SOI is well suited to high-frequency applications, due to its low-parasitic architecture that enables decoupling of active device optimization from the engineering of the underlying substrate materials, thanks to a physical separation by the buried oxide (BOX) layer.

To achieve low loss and highly linear substrates, high effective resistivity (ρ_{eff}) is required. To assess substrate-ρ_{eff} and substrate linearity of coplanar CMOS-type circuitry in general, coplanar waveguides (CPWs) are chosen as the test vehicle. The resistivity of semiconductors is by nature dependent on the local electric field. In low-doped high-resistivity (HR) substrates, it is typical for the semiconductor volume beneath the insulator to be in a conductive state due to (even low-level) parasitic fields present in the multilayer, such as originating from fixed charges present at the insulator/semiconductor interface. Then, a highly conductive channel-like layer is induced at the interface, locally lowering the resistivity beneath the circuits by a factor of 10^3–10^6. This in turn lowers the sensed ρ_{eff} by a factor of 10–10^4 to values as low as 1 Ω·cm. This is referred to as the parasitic surface conduction (PSC) effect that renders the use of an HR substrate ineffective [1], [5]. A breakthrough was made in the early 2000s by introducing a thin trap-rich (TR) polysilicon layer beneath the BOX in SOI technology [6], [7]. This layer mitigates the PSC effect by pinning the Fermi-level near midgap at the interface in a highly resistive state, enabling ρ_{eff} values of over 1 kΩ·cm, and is widespread in the RFIC industry today [4], [8].

These considerations motivate the development of both small- and large-signal RF models of silicon-based substrates.

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The linear modeling of silicon-based substrates, which can capture RF path loss, effective resistivity, and substrate crosstalk, is well established [1], [9].

In order to model the impact of substrate nonlinearities in metal–insulator–semiconductor (MIS) devices, a solid understanding of semiconductor physics is required.

Though much experimental RF data have been reported [1], [4], [8]–[11], no large-signal simulations accounting for carrier dynamics have been proposed to model RF substrates.

This is the objective of this article, which starts by presenting charge-balance analyses as a function of applied voltage signal (dc or RF), fixed interface charge, and ionized traps.

First, a static analysis is considered in order to illustrate the working principle of how TR layers overcome the PSC effect.

Next, substrates are analyzed in response to dynamic excitation signals. Using step functions to pulse an MIS structure from a strong negative applied charge to a strong positive applied charge provides physical insight into carrier dynamics.

Finally, sinusoidal transient large-amplitude signals are considered. Such excitations enable us to analyze quantitatively the harmonic distortion for various types of substrates.

Overall, strong insight into the impact of semiconductor material and interface properties on the RF substrate FoMs is achieved. Validations based on on-wafer RF measurements are presented in Part II [12].

II. Charge Compensation at Equilibrium

A. Free Carriers, Ionized Traps, and Fermi-Level Pinning

In a classical HR substrate, a PSC layer is induced made up of many free electrons that compensate the oxide charge (positive at SiO_2/Si interfaces). The working principle of the TR layer is to provide a different charge compensation mechanism. Indeed, the positive (negative) fixed charge Q_{ox} ($\equiv qN_{ox}$) must be compensated by negative (positive) charges in the semiconductor, but to maintain high resistivity, it is desired that the compensating charge not be made up of free carriers that contribute to conduction. Instead, ionized traps balance the charge, preferably such that the interface Fermi level is deep in the bandgap (i.e., low free carrier concentrations) ensuring a state of high resistivity.

As an example, let us consider an MOS capacitor structure defined on a semiconductor material, such as shown in Fig. 1, that may in general include donor and acceptor trap distributions $g_D(E)$ and $g_A(E)$ defined within the bulk volume.

The total charge density applied to this structure is

$$N_{\text{Applied}} = Q_{\text{dc}}/q + N_{\text{ox}} - Q_{\text{MS}}/q [\text{cm}^{-2}] \quad (1)$$

$$Q_{\text{dc}} = (V_{\text{dc}} - \phi_S) C_{\text{ox}} [\text{cm}^{-2}] \quad (2)$$

where Q_{dc} is the charge density on the metallic top electrode induced by the applied control voltage V_{dc} relative to the substrate and ϕ_S is the surface potential. The term $Q_{\text{MS}} = V_{\text{MS}} C_{\text{ox}}$ accounts for the charge induced by the difference between the work function of the metal and that of the semiconductor. $C_{\text{ox}} = \epsilon_{\text{ox}}/t_{\text{ox}}$ is the normalized oxide capacitance per unit area, expressed in F/cm^2, with ϵ_{ox} and t_{ox} defined as the oxide permittivity and thickness, respectively.

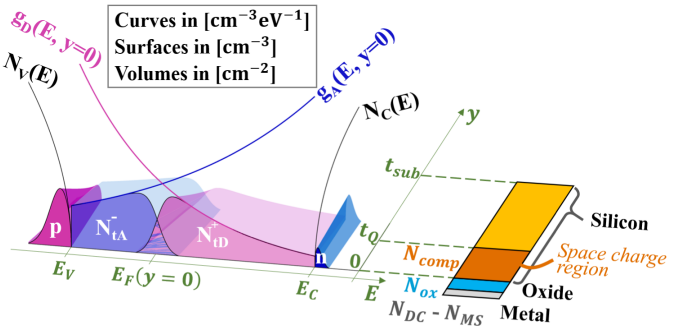

Fig. 1. Graphical representation of charge density distributions, in energy and depth, in a general MOS capacitor structure on a semiconductor substrate including arbitrary trap distributions.

At equilibrium, a compensation charge density N_{comp} is induced in the substrate to exactly counter-balance N_{Applied}

$$N_{\text{comp}} = -N_{\text{Applied}} \text{ at equilibrium } [\text{cm}^{-2}]. \quad (3)$$

It can be made of either free carriers or ionized traps

$$\begin{aligned} N_{\text{comp}} &= \int_0^{t_Q} \frac{\rho_q}{q}\, dy \ [\text{cm}^{-2}] \\ &= \int_0^{t_Q} N_{\text{free}}\, dy + \int_0^{t_Q} N_{\text{trap}}\, dy \\ &= \int_0^{t_Q} (p - n)\, dy + \int_0^{t_Q} \left(N_{tD}^+ - N_{tA}^-\right) dy \\ &= N_{\text{free}_{\text{INT}}} + N_{\text{trap}_{\text{INT}}} \end{aligned} \quad (4)$$

where we have defined the free and trapped interfacial charge densities $N_{\text{free}_{\text{INT}}}$ and $N_{\text{trap}_{\text{INT}}}$ obtained by integrating over the space charge depth t_Q to yield a charge density per unit interface area. N_{tD}^+ and N_{tA}^- are the ionized acceptor and donor trap densities, respectively (including thermal dopants, i.e., shallow trap states). Donor traps that are filled by an electron are neutral and are positively charged when empty, whereas acceptor traps are negatively charged when filled by an electron and are neutral when empty.

Beyond the space charge region, there is no net charge.[1]

Fig. 1 shows the key components of (4) for the case of an MOS capacitor defined on an arbitrary substrate that includes donor and acceptor trap distributions $g_D(E, y)$ and $g_A(E, y)$.

The density of states (DOS) available to electrons, holes, ionized donor traps, and ionized acceptor traps are $N_C(E)$, $N_V(E)$, $g_D(E)$, and $g_A(E)$, respectively. These four curves are plotted at the Si/SiO_2 interface in the $y = 0$ plane. Each of these distributions is then multiplied by the occupation function and integrated over energy

$$N_{tD}^+(\overline{r}) = \int_{E_V}^{E_C} g_D(E, \overline{r}) \cdot \left(1 - F(E, \overline{r})\right) dE [\text{cm}^{-3}] \quad (5)$$

$$N_{tA}^-(\overline{r}) = \int_{E_V}^{E_C} g_A(E, \overline{r}) \cdot F(E, \overline{r})\, dE [\text{cm}^{-3}] \quad (6)$$

$$n(\overline{r}) = \int_{E_C}^{E_{MC}} N_C(E) \cdot F(E, \overline{r})\, dE [\text{cm}^{-3}] \quad (7)$$

$$p(\overline{r}) = \int_{E_{mV}}^{E_V} N_V(E) \cdot \left(1 - F(E, \overline{r})\right) dE [\text{cm}^{-3}]. \quad (8)$$

[1]We write: $p(y) - n(y) + N_{tD}^+(y) - N_{tA}^-(y) = 0$ for $y > t_Q$.

The resulting area plots in the $y = 0$ plane represent the charge densities n, p, N_{tA}^{-}, and N_{tD}^{+} in cm^{-3} at the interface.

The interfacial trapped charge density $N_{\text{trap}_{\text{INT}}}$ is computed graphically as the difference between the purple and blue volumes situated between E_V and E_C and between $y = 0$ and $y = t_Q$. Similarly, $N_{\text{free}_{\text{INT}}}$ is computed as the difference between the purple volume situated below E_V and below t_Q and the blue volume situated above E_C and below t_Q.

B. Charge Compensation Analysis: HR Versus TR

Now, let us analyze the charge compensation mechanisms of an MOS capacitor in two distinct substrates of interest.

1) *HR:* An HR substrate without any traps: $g_D(E) = g_A(E) = 0$.
2) *TR:* A TR substrate with strong trap distributions.

For both substrates, two cases are considered.

1) A highly negative charge density $N_{\text{Applied}-}$ is imposed.
2) A highly positive charge density $N_{\text{Applied}+}$ is imposed.

In both cases, the two substrates provide the same compensation charge $N_{\text{comp}} = N_{\text{free}_{\text{INT}}} + N_{\text{trap}_{\text{INT}}} = -N_{\text{Applied}}$.

In case 1, we denote as E_{F-} the position of the Fermi level at the Si/SiO_2 interface ($y = 0$). Note that E_{F-} is different for the two considered substrates. Then, Fig. 2 (HR-1) and (TR-1) show the charge densities at the interface for both substrates, where the energy configuration is $E_F(y = 0) = E_{F-}$.

For the HR substrate, the compensation charge is entirely made up of the term $N_{\text{free}_{\text{INT}}}$. Therefore, in order to compensate for the highly negative applied charge $N_{\text{Applied}-}$, the Fermi level has moved close to the valence band edge, and a large free hole concentration p (purple area) is induced at the interface to provide the compensation.

For the TR substrate, trapped charge also contributes to N_{comp}. Fig. 2 (TR-1) highlights this, where large valued functions $g_D(E)$ and $g_A(E)$ have been introduced. One can see that the charge balance is mainly provided by the ionized trap densities N_{tA}^{-} and N_{tD}^{+} (blue and purple areas in the bandgap, respectively). Free carrier densities n and p are inevitably present but are in negligible quantity compared to the ionized trap terms in TR substrates. This is because many deep-level traps close to the interface provide the necessary compensation charge and maintain the Fermi level deep in the bandgap.

Note that in response to the negative $N_{\text{Applied}-}$, both (HR-1) substrate and the (TR-1) substrate must provide the same net positive compensation charge N_{comp}.

In case 2, we denote as E_{F+} (different for the two substrates) the position of the Fermi level at the interface.

For the HR substrate, the Fermi level has moved close to E_C, and a large free electron concentration n (blue area) is induced at the interface to provide the compensation.

For the TR substrate, a Fermi level E_{F+} situated deep in the bandgap is able to provide a charge configuration that compensates for $N_{\text{Applied}+}$. Also, once again, free carrier densities (that contribute to $N_{\text{free}_{\text{INT}}}$) are in negligible quantity.

In terms of RF substrate performance, a low value of N_{free} comes high effective substrate resistivity and strong substrate linearity. For TR substrates, N_{free} remains low for usual values of N_{Applied},[2] meaning that TR's RF performance depends little on the dc bias voltage.

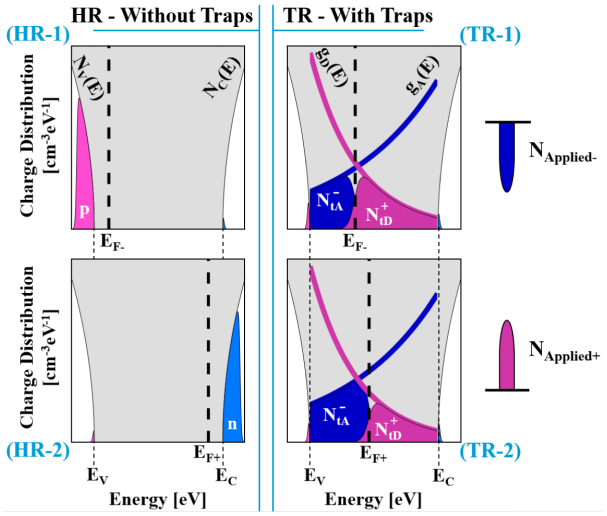

Fig. 2. Example of trap occupancy and free carrier density variation at the surface in response to a shift in the Fermi level from E_{F-} to E_{F+}. Initial configuration at E_{F-} (HR-1) and (TR-1). Second configuration at E_{F+} after some band bending due to some introduced positive charge [applied positive bias for example (HR-2) and (TR-2)].

In HR substrates, N_{free} is the dominating (only) compensation mechanism, requiring large swings in E_F and allowing for large swings in n and p (strong accumulation to strong inversion). This allows the substrate interface to be in conductive states, contributing to increased loss. Time-varying signals on such substrates induce applied charge variations $\Delta N_{\text{Applied}}$ that strongly influence the substrate's electrical parameters. Variations in substrate conductance and capacitance flow from variations in free carrier densities n and p that determine substrate impedance, making HR substrates quite nonlinear.

In TR substrates, N_{trap} is the dominating compensation term. In response to a $\Delta N_{\text{Applied}}$, compensation is achieved with only a small variation in E_F deep in the bandgap that produces large variations in N_{tD}^{+} and N_{tA}^{-}, thereby avoiding large values of the free carrier densities n and p. The Fermi level at the interface is said to be deeply pinned, locking the interface in a state of high resistivity, with little dependence on N_{Applied}, making TR substrates low loss and very linear.

C. Impact of the TR Layer on RF Performance

To evaluate the impact of a TR layer on the RF substrate FoMs, TCAD simulations were run on a CPW line structure. With reference to Fig. 3(a), the physical parameters are as follows:

1) Metal thickness of the CPW line $t_{\text{metal}} = 1\ \mu\text{m}$.
   a) Aluminum, with metal work function $\phi_M = 4.1$ eV.
   b) CPW dimensions $W_C/S/W_G = 26/12/200\ \mu\text{m}$.
2) Oxide thickness $t_{\text{ox}} = 400$ nm.
   a) With $N_{ox} = Q_{\text{ox}}/q = +10^{11}\ \text{cm}^{-2}$.

[2]By usual values of N_{Applied}, it is meant densities that will typically be encountered in RFICs, such as originating from a few volts on an MOS structure with an oxide thickness in the range of 1 μm and/or originating from fixed oxide charge densities at Si/SiO_2 interfaces in the range of $10^{11}\ \text{cm}^{-2}$.

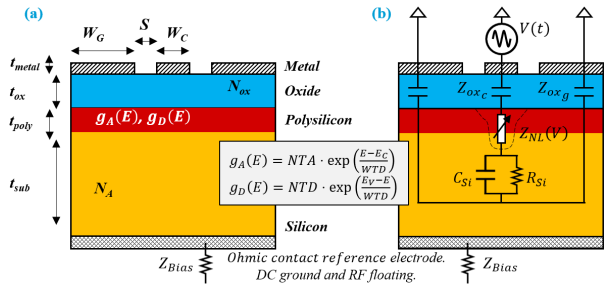

Fig. 3. Cross section of the simulated CPW structure on silicon-based substrates. (a) Physical parameters. (b) Simplified equivalent circuit model that roughly highlights the linear and nonlinear regions of the substrate under large-signal excitation. Inset: tail trap DOS equations.

3) Polysilicon thickness $t_{\text{poly}} = 1\ \mu$m using tail distributions $g_{\text{TA}}(E)$ and $g_{\text{TD}}(E)$ [13], [14] (equations inset in Fig. 3).
   a) Characteristic energies WTA = WTD = 40 meV.
   b) Density variable NTA = NTD = NT.
4) Silicon substrate thickness $t_{\text{sub}} = 500\ \mu$m.
   a) $N_A = 2.8 \times 10^{12}$ cm^{-3}, i.e., $\rho_{\text{nom}} = 5$ kΩ·cm.

Based on this CPW device, substrate performances were simulated (at 25 °C) for a range of trap densities NT, from 10^{16} to 10^{22} cm^{-3}eV^{-1}, and are presented in Fig. 4.

Below NT of 10^{18} cm^{-3}eV^{-1}, the traps are in negligible quantity and the substrate can be considered as an HR. In that case, Fig. 4(a) shows that the Fermi level at the SiO_2 interface is close to the conduction band, at around $E_V + 0.87$ eV, due to the fixed interface charge density N_{ox}. As a consequence, a PSC layer (many electrons) is present at the interface, which translates into a low effective resistivity and high levels of harmonics as shown in Fig. 4(c) and (d).

Substrate linearity is evaluated by the amount of generated second-harmonic power component $H2$ at the output of a CPW line when a pure sine excites its input. This is shown in the inset of Fig. 4(d), where $H2$ is computed for a simulation fundamental power of +15 dBm, which corresponds to a sinusoidal RF voltage amplitude of 1.78 V.

Fig. 4(b) shows the net interfacial density of free carriers $N_{\text{free}_{\text{INT}}}$ and the net interfacial density of trapped charges $N_{\text{trap}_{\text{INT}}}$ directly beneath the signal line of the simulated CPW structure. They are obtained from (4) by integrating up to a depth of $t_{\text{poly}} = 1\ \mu$m (finite boundary instead of using t_Q). At equilibrium, they can be directly compared to N_{Applied}.

V_{MS} is computed as −0.65 V. Therefore, at $V_{\text{dc}} = 0$, we calculate $-N_{\text{Applied}} \approx -1.35 \times 10^{11}$ cm^{-2} using (1). The dashed blue line in Fig. 4(b) plots this $-N_{\text{Applied}}$, and one can observe that the sum of the two curves $N_{\text{free}_{\text{INT}}}$ and $N_{\text{trap}_{\text{INT}}}$ (see (4)) approximately equals this value, for all simulated substrates, in agreement with (3).

As the trap density NT is increased in the polysilicon layer, the traps contribute more strongly ($N_{\text{trap}_{\text{INT}}}$ ↗) to the compensation of N_{Applied}. The Fermi level moves deeper into the bandgap [see Fig. 4(a)] and the free carriers contribute less ($N_{\text{free}_{\text{INT}}}$ ↘). The interface becomes more resistive, and the PSC layer weakens in conductance, which translates into a higher effective resistivity, as shown in Fig. 4(c), and to lower distortion levels, as shown in Fig. 4(d).

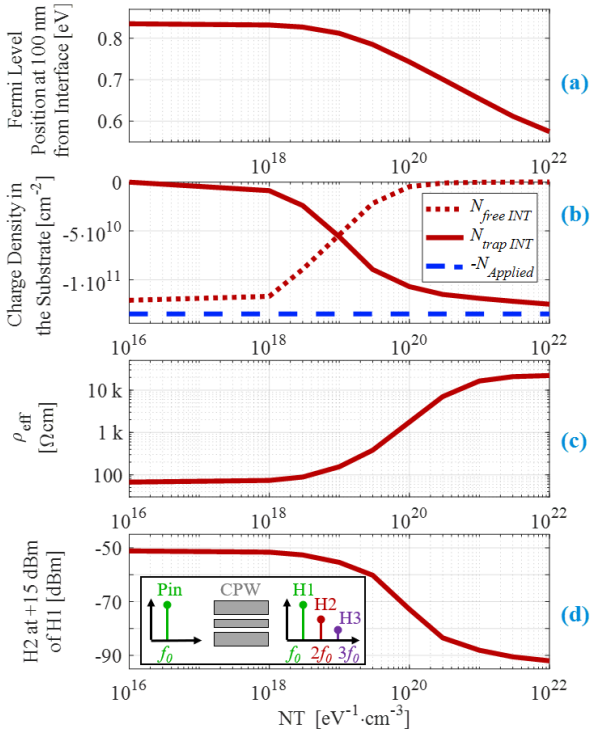

Fig. 4. Simulated electrical parameters of a CPW line on a TR substrate as a function of trap density NT in the polysilicon passivation layer (at 25 °C). The applied dc bias is 0 V. (a) Position of the Fermi level at 100 nm below the oxide layer. (b) Interfacial densities of free charge and trapped charge. (c) Effective resistivity, extracted above slow wave mode (>10 GHz). (d) Second-harmonic level for +15 dBm of output fundamental at $f_0 = 900$ MHz.

When NT increases above the range of 1×10^{20} cm^{-3}eV^{-1}, the polysilicon can really be considered as an effective TR layer since ρ_{eff} increases above 3-kΩ·cm $H2$ decreases below −80 dBm. A value of −80 dBm at $f_0 = 900$ MHz corresponds to the linearity quality of the commercially available eSI80 substrates from Soitec [4], [8] (benchmarked using CPWs of the same dimensions as here).

Notice how the total amount of trapped charge $N_{\text{trap}_{\text{INT}}}$ converges toward $-N_{\text{Applied}} = -1.35 \times 10^{11}$ cm^{-2} as NT increases, to compensate almost entirely the applied charge. When NT is low, it can be seen that $N_{\text{free}_{\text{INT}}}$ provides entirely this compensation charge $-N_{\text{Applied}}$.

All of the results presented in Fig. 4 were obtained without applying any net dc voltage between the CPW test structure and the semiconductor substrate. A dc bias will strongly affect the behavior of semiconductor substrates, by significantly contributing to N_{Applied}, as described by (1).

Fig. 5 then analyzes the substrate's small- and large-signal RF behavior as a function of varying dc bias voltage. This voltage is applied to the signal line relative to the two ground lines of the CPW. The substrate is also dc grounded (to the same potential as the CPW's ground lines) through a large bias resistor and is therefore RF floating. This biasing situation is close to the setup used during on-wafer RF measurements.

Fig. 5(a) shows that as the trap density NT increases, the interface Fermi level becomes more tightly pinned, to a deep position. This translates into a smaller variation of $N_{\text{free}_{\text{INT}}}$ as a function of the line voltage (dc and RF).

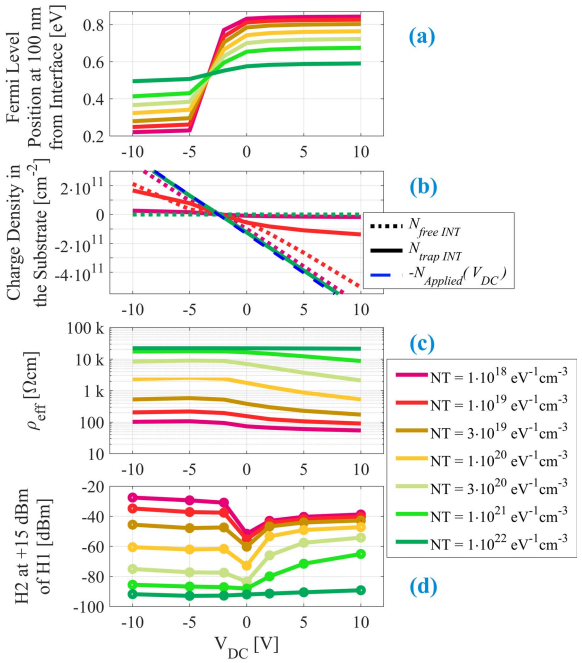

Fig. 5. Simulated electrical parameters of a CPW line as a function of applied dc voltage V_{dc}, for several TR substrates with various trap densities NT (at 25 °C). (a) Position of the Fermi level at 100 nm below the oxide layer. (b) Interfacial densities of free charge and trapped charge. (c) Effective resistivity, extracted above slow wave mode (>10 GHz). (d) Second-harmonic level for +15 dBm of output fundamental.

For the case of a large value of NT $= 1 \times 10^{22}$ cm^{-3}eV^{-1}, the substrate's FoMs ρ_{eff} and $H2$ have almost no bias dependence, due to the very tight Fermi-level pinning.

The sum of the curves $N_{\text{free}_{\text{INT}}}(V_{\text{dc}}) + N_{\text{trap}_{\text{INT}}}(V_{\text{dc}})$ of Fig. 5(b) gives the unique curve $-N_{\text{Applied}}(V_{\text{dc}})$, which is calculated according to (1) and plotted in a blue dashed line.

Figs. 4 and 5 show physical insight into the inner workings of HR and TR substrates and show the link between the physics and the RF performance metrics. Further comments on the results are reserved for Part II [12]. Model correlation to measured small- and large-signal data is also given in Part II [12], providing a first demonstration of accuracy in modeling both HR and TR samples.

III. Nonequilibrium Dynamics

So far, all of the above discussion has been in the framework of semiconductor materials that have reached equilibrium. In particular, all curves from all substrates of Figs. 4(a)–(c) and 5(a)–(c) are at equilibrium.

However, carriers and traps have finite response times, and equilibrium concentrations take time to be reached (finite inertia). Then, in response to a time-varying voltage signal, the equilibrium compensation charge in the substrate may not have time to establish itself, and this is particularly the case when considering large-amplitude and high-frequency signals. In general, under such conditions, (3) does not hold true.

To illustrate the response times, the CPW structure of Fig. 3 is analyzed using $t_{\text{ox}} = 400$ nm, N_{ox} set to 0 or 10^{11} cm^{-2}, p-type silicon substrate of nominal resistivity ρ_{Si} (variable) and without any TR layer, and a single midgap recombination center (uniform density of 10^{14} cm^{-3}).

A transient voltage signal is applied on the central CPW electrode, with the substrate potential set to the reference value of 0 V. Neutral electrodes at 0 V are defined for the two ground lines of the CPW. The applied voltage signal is initially at −10 V, and the substrate's initial equilibrium condition below the CPW central line is, therefore, an accumulation state. The line voltage is then ramped to +10 V with a 1-ps step time.

An analysis is then made on the carrier response times in the substrate by looking at the evolution of the free interfacial charge densities defined over a 1 μm depth as

$$p_{\text{INT}} \triangleq \int_0^{1\,\mu\text{m}} p(\overline{r})\ dy, n_{\text{INT}} \triangleq \int_0^{1\,\mu\text{m}} n(\overline{r})\ dy. \tag{9}$$

A. Response Time Analysis Without Fixed Oxide Charge

Fig. 6(a) and (b) then shows the evolution of the interfacial carrier concentrations over time below the signal line $p_{\text{INT}}(t)$, $n_{\text{INT}}(t)$, and $N_{\text{free}_{\text{INT}}}(t)$, considering a range of bulk P-type substrate resistivities, and with $N_{\text{ox}} = 0$ cm^{-2}. The introduced voltage step pulses the structure from a state of strong accumulation to a state of strong inversion, meaning that the large interfacial hole density p_{INT} must be repelled, and a large interfacial electron density n_{INT} must be induced.

It is important to note that the total number of electrons and holes in the system is very different at $t = +\infty$ than at $t = 0$, before and after the voltage step is applied. To reach the final equilibrium, free carriers must be generated/recombined.

However, the existing carriers in the substrate may spatially rearrange themselves in response to the pulse to minimize the global nonequilibrium while waiting for thermal generation/recombination of carriers to provide total equilibrium.

Thermal variations in carrier densities are approximately linear with time, as depicted by the dashed blue line in Fig. 6(a) whose slope is determined by the net generation/recombination rate. τth depends on many material parameters (trap energy distributions, capture cross sections, and surface rates). In the context of this work, the exact value of τth is not critical when studying substrate response to RF signals, as long as τth is significantly longer than 1 ns, which is a reasonable assertion.

Before final equilibrium is achieved through thermal generation after 1–10 ms, carriers undergo a rearrangement process within the silicon. However, carriers cannot respond instantaneously since they have finite inertia. Fig. 6(a) shows that the majority carriers in the accumulation layer respond in a finite time τ_{sub}, that is of the order of 1–10 ns. This time constant is the dielectric relaxation time of the substrate

$$\tau_{\text{sub}} = 2\pi\rho_{\text{Si}}\epsilon_{\text{Si}}\,[s]. \tag{10}$$

In the considered silicon substrates, this characteristic time depends on the nominal resistivity. For the 1-kΩ·cm and 50-Ω·cm substrates, τ_{sub} is calculated using (10) as 6.5 ns and 320 ps, respectively, and these values agree well with the observable response times from the TCAD results. τ_{sub} represents the time needed to repel the accumulation layer from the interface into the substrate. At the same time, available minority carriers from elsewhere in the substrate are attracted.

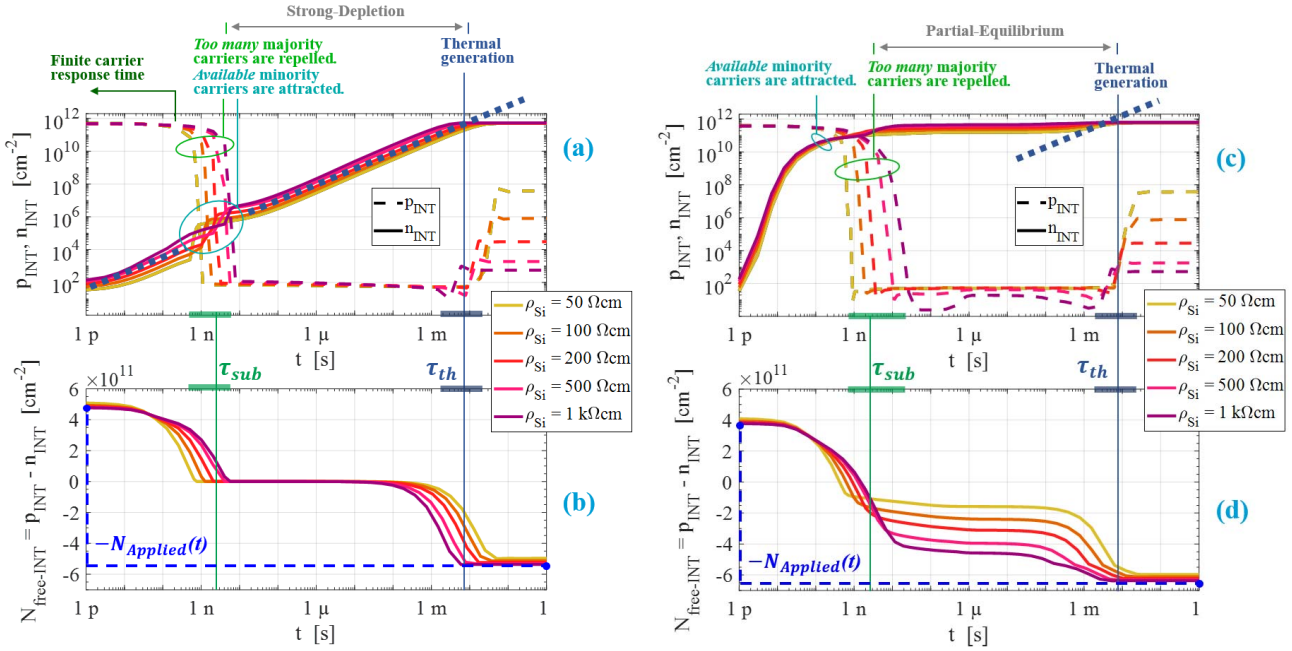

Fig. 6. Simulations of the evolution over time of interfacial free carrier densities in p-type substrates in response to a transient voltage pulse from −10 V (strong accumulation) to +10 V (strong inversion) with a 1 ps ramp time. (a) and (b) $N_{ox} = 0$ cm^{-2}. (c) and (d) $N_{ox} = 10^{11}$ cm^{-2}.

Between times τ_{sub} and τth, we say that the interface region is in a state of strong depletion and that the silicon below this interface is in a state of deep depletion.

1) The notion of strong depletion describes the interface at all times for which $N_{free_{INT}}(t) \ll N_{free_{INT}}(t = +\infty)$. This is highlighted in Fig. 6(a) and (b), which show that the interface is strongly depleted from τ_{sub} to τth.
2) The notion of deep depletion describes an extent of the space charge region into the substrate. The nonequilibrium depletion region is deeper than the final equilibrium one. Physically, this happens such that a large space charge region, negatively charged (ionized acceptor dopants), provides charge compensation to the applied +10 V, while free electrons are thermally generated.

Too many holes are repelled from the interface, in the sense that $p_{INT}(\tau_{sub} < t < \tau\text{th}) \ll p_{INT}(t = +\infty)$, and we have $n \cdot p \ll n_i^2$ in the nonequilibrium depletion region.

Once the time gets close to τth and almost enough electrons have been thermally generated, holes drift back to the interface to achieve the equilibrium concentrations. It is plain to see from Fig. 6(b) that (3) only holds true when $t = 0$ and when $t \gg \tau$th, i.e., when the system is at equilibrium.

Transient voltage simulations of an MOS device in 1-D using $N_{ox} = 0$ cm^{-2} from [15] provide similar results to those of Fig. 6(a) and (b) and support them.

B. Response Time Analysis With Fixed Oxide Charge

Let us now perform the same type of analysis on a substrate with a fixed interfacial charge density of $N_{ox} = 10^{11}$ cm^{-2}. Fig. 6(c) and (d) shows the evolution of the interfacial carrier concentrations $p_{INT}(t)$, $n_{INT}(t)$, and $N_{free_{INT}}(t)$.

Once again, the introduced voltage step pulses the structure from a state of strong accumulation to a state of strong inversion for all considered substrates. Once more, the large interfacial hole density p_{INT} must be repelled, and a large interfacial electron density n_{INT} must be induced.

Final equilibrium must once again be obtained by thermal generation and recombination and will only be established after 1–10 ms for the arbitrary (TCAD Atlas default) SRH parameters used in these simulations.

However, there are large reservoirs of electrons in the system, induced to the left and right of the signal CPW line by the positive N_{ox}. At the initial equilibrium point $t = 0$, there is an electronic PCS layer (inversion in p-type substrates) present over the entire wafer, except beneath the signal line where a state of accumulation is enforced by the initial applied −10 V.

As the voltage is ramped to +10 V, a partial equilibrium can be achieved quite rapidly because the number of available minority carriers is high, as they are present in large quantities in the PSC regions over the entire wafer.

Fig. 6(c) and (d) shows that at a time close to τ_{sub}, the carriers have had time to spatially rearrange themselves in response to the voltage step (without reaching equilibrium). The key difference compared to Fig. 6(a) and (b) is that the magnitude of electron response is larger, due to the availability of a much higher number of electrons in the system. The effect is that strong depletion is avoided at the interface, and a partial equilibrium is reached instead. Fig. 6(b) shows that strong depletion spans from $t = \tau_{sub}$ to $t = \tau$th, but in Fig. 6(d), a significant portion of the required electron density floods to the interface within a few nanoseconds. Though this partial equilibrium density $n_{INT}(\tau_{sub} < t < \tau\text{th})$ is not the final equilibrium density $n_{INT}(t = +\infty)$, the interface cannot be said to be in a state of depletion, and actually, fairly strong inversion is obtained within a short time.

The magnitude response of the attracted inversion layer is larger for lower doped substrates, as the available minority carrier density in the PSC electronic reservoirs is higher. The

PSC density in cm^{-2} in the regions adjacent to the central CPW line over 1 μm depth is approximately equal to

$$n_{\mathrm{PSC_{INT}}} \triangleq \int_0^{1\,\mu\mathrm{m}} n(\overline{r})\; dy \approx N_{\mathrm{ox}} - \int_0^{1\,\mu\mathrm{m}} N_A\; dy \qquad (11)$$

where N_A is the nominal substrate doping, in cm^{-3}. This is the available carrier density in the reservoirs adjacent to the central CPW line and is a function of the doping, as negatively ionized acceptor dopants provide partial charge compensation to N_{ox}. For the 1-kΩ·cm silicon, the reservoir density is analytically computed using (11) as 9.8×10^{10} cm^{-2} ($\approx N_{\mathrm{ox}}$). For the 50-Ω·cm substrate, $n_{\mathrm{PSC_{INT}}}$ is calculated as 6.7×10^{10} cm^{-2}. Fig. 6(d) highlights the fact that substrates with a higher reservoir density provide carriers in densities closer to the final equilibrium values. In all cases, partial equilibrium corresponds to a significant proportion of the final strong inversion density. The response time is not governed by τ_{sub}, as these carriers do not move through the substrate region characterized by ρ_{Si} but come instead from the PSC reservoirs. The TCAD simulations also revealed that the deep-depletion effect was extended to the depletion regions below the PSC layers adjacent to the signal electrode location. As minority carriers leave the PSC layer to flood below the signal electrode, some nonequilibrium is propagated to these regions, which they have too few interface minority carriers to balance the oxide charges. The depletion regions below these interfaces are then extended deeper into the substrate, to provide some compensation charge by pushing away majority carrier into the bulk, causing a net negative space charge in these regions due to the ionized acceptor dopants of the bulk.

Once more, too many holes are repelled from the interface, in the sense that $p_{\mathrm{INT}}(\tau_{\mathrm{sub}} < t < \tau\mathrm{th}) \ll p_{\mathrm{INT}}(t = +\infty)$, and (3) only holds for $t = 0$ and $t \gg \tau\mathrm{th}$ (at equilibrium).

C. Sinusoidal Excitation and Impact of Fundamental Frequency on Harmonic Distortion

We have overviewed carrier dynamics and response times in an MOS structure subjected to a large-amplitude voltage step. It is clear from those discussions that the frequency of a large-amplitude sine wave will determine the magnitude of free carrier response. To illustrate this, the same CPW MOS structure [shown in Fig. 3(b)] is subjected to an RF signal at frequency f with an amplitude of 2.5 V centered around a dc bias point of 0 V. The considered substrate is a 1-kΩ·cm p-type, without any polysilicon layer and with an interfacial oxide charge density of $N_{\mathrm{ox}} = 10^{11}$ cm^{-2}. The simulated interfacial free carrier density $N_{\mathrm{free_{INT}}}(t)$ is plotted against normalized time t/T in Fig. 7 for several frequencies $f = 1/T$.

At the very low frequency of $f = 1$ Hz, we can say that the substrate is in equilibrium at each point in time, and thus, the amplitude of the $N_{\mathrm{free_{INT}}}(t)$ response is maximum.

As the frequency is increased, the inertia of the dynamic effects limit the amplitude response of $N_{\mathrm{free_{INT}}}(t)$. This is observable already above a few hundreds of hertz, as the final equilibrium time is of the order of 1–10 ms (see Section III-B).

Above a few tens of kilohertz, we may consider that only carriers that were initially present in the MOS structure

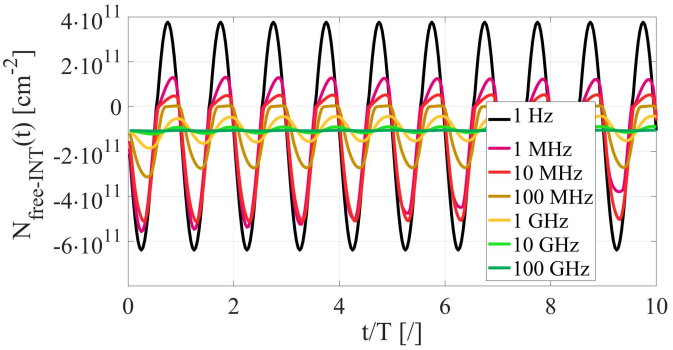

Fig. 7. Simulated interfacial free carrier density $N_{\mathrm{free_{INT}}}(t)$ below an MOS CPW line versus normalized time t/T for a 2.5-V amplitude sinusoidal excitation around 0-V dc bias for several frequencies $f = 1/T$ (at 25 °C). The substrate is a 1-kΩ·cm p-type with a 400-nm oxide characterized by $N_{\mathrm{ox}} = 10^{11}$ cm^{-2}. No TR layer is present.

can rearrange themselves within the substrate in response to the large signal. Up to a few hundreds of megahertz and with an interfacial charge density N_{ox} of 10^{11} cm^{-2} defined, partial equilibrium can be obtained within a few nanoseconds, and the variation in $N_{\mathrm{free_{INT}}}(t)$ still remains significant (see Section III-B).

However, as the frequency increases above a few gigahertz, the carrier response amplitude decreases significantly, as then even the existing carriers cannot follow the RF signal. This is in agreement with the carrier response times of the order of the nanosecond, for both minority and majority carriers.

This is highlighted in Fig. 8(a), which plots the amplitude of the net free interfacial charge density $\boldsymbol{A}\{N_{\mathrm{free_{INT}}}(t)\}$ as a function of frequency. The effective conductivity $\sigma_{\mathrm{eff}} = 1/\rho_{\mathrm{eff}}$ of the substrate is also plotted over frequency. Due to the conductive nature of an HR suffering from the PSC effect, the propagation at low frequencies is in the slow wave mode. In this mode, the E-field is mainly concentrated within the insulator that then dominates the substrate impedance, and the silicon region below it basically acts as an equipotential ac node.[3] Three dc bias conditions are considered in Fig. 8.

Fig. 8(b) shows the simulated second-harmonic distortion component $H2$ for a fundamental output power of $H1 = +15$ dBm as a function of fundamental frequency. It shows that the distortion is maximum around 1 GHz. This can be explained from the plots of Fig. 8(b) and based on the simplified equivalent circuit that is superimposed on the MOS CPW structure of Fig. 3(b). In that circuit, all impedances are linear except for the impedance $Z_{NL}(V)$ that models the silicon regions at the interface beneath the CPW line.

The $H2(f)$ curve can be understood from the facts that the following holds.

1) At lower frequencies, the dielectric impedances (in series) dominate and linearize the overall substrate impedance.
2) At higher frequencies, the substrate region below the CPW signal line becomes more linear due to the finite response times of carriers in the semiconductor, i.e., variations in $Z_{NL}(V)$ are dampened by carrier

[3]Referring to Fig. 3, the propagation is said to be in the slow wave mode at frequencies for which $1/(2\pi f C_{\mathrm{ox}}) > R_{\mathrm{Si}}$).

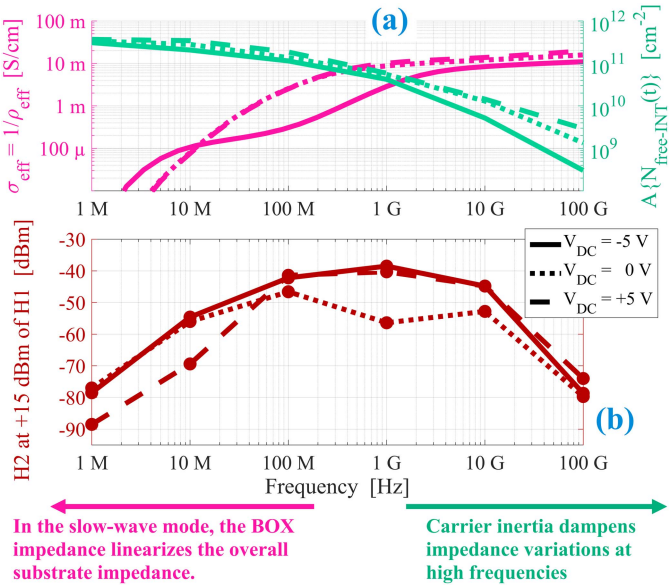

Fig. 8. TCAD results of a CPW line simulated on a 1-kΩ·cm p-type HR substrate with 400 nm of oxide and $N_{ox} = 10^{11}$ cm^{-2}, plotted over frequency at three dc bias points (at 25 °C). (a) Frequency dependence of the effective conductivity $\sigma_{eff} = 1/\rho_{eff}$ and the amplitude of the net free interfacial charge density $\boldsymbol{A}\{N_{free_{INT}}(t)\}$. (b) Frequency dependence of the second-harmonic distortion component $H2$ for a fundamental component power $H1$ of +15 dBm.

inertia. The overall substrate impedance then becomes more linear.

These two effects both tend to reduce harmonic distortion: the first in the low-frequency range and the second in the high-frequency range. The distortion is then maximum in the intermediate frequency range at around 1 GHz.

This corresponds to a frequency slightly before the end of the slow wave mode when the oxide impedance is no longer dominating[4] the total substrate impedance and before the amplitude response of $\boldsymbol{A}\{N_{free_{INT}}(t)\}$ and therefore $\boldsymbol{A}\{Z_{NL}(t)\}$ reduces any further.

It corresponds to a tradeoff point between the impacts of these two effects. We can then conclude by saying that the nonlinearity of an HR substrate depends on the frequency responses of both ρ_{eff} and $\boldsymbol{A}\{N_{free_{INT}}(t)\}$. Both of these parameters depend on the fixed oxide charge density N_{ox} at the Si/SiO$_2$ interface. The dielectric impedance, and hence the dielectric thickness, impacts strongly on the $\rho_{eff}(f)$ response.

The bell shape of the $H2(f)$ curve can then be shifted up or down in frequency depending on the slow wave transition frequency. For the case presented here, an HR with $N_{ox} = 10^{11}$ cm^{-2}, this transition frequency is in the range of 1 GHz. For TR-type substrates, it is typically in the range of a few megahertz. $H2(f)$ measurements will be presented in Part II, for several TR and several HR substrates, with N_{ox} up to 2.1×10^{12} cm^{-2}.

IV. Conclusion

For the first time to the authors' knowledge, this article provides detailed information on the physical behavior of RF substrates under large-amplitude excitations through quantitative analysis of HR and TR substrates.

Under such excitations, nonequilibrium states are fully considered and the dynamics of carriers analyzed, as they are responsible for governing impedance variations in response to the applied signals and hence govern nonlinear distortion.

By considering a wide range of fundamental excitation frequencies, these analyses allow us to evaluate the relative impact of the dielectric layer and that of free carrier inertia on the HD levels of HR and TR substrates.

The concept of available carriers is of high relevance when considering high-frequency large-amplitude signals that vary too rapidly for the total amount of free carriers to change significantly in response (through thermal recombination).

In Part II of this series [12], a wide range of substrate measurements and simulations are provided for several HR and TR samples with different material properties. An excellent model to hardware correlation is achieved over this broad range, due to the physical insight gained from this article, which enables all data trends in [12] to be well understood.

[4]It is not negligible but is not dominating either: at 1 GHz, $Z_{ox_c} + Z_{ox_g}$ accounts for roughly 65% of the norm of the overall total substrate impedance.

References

[1] M. Rack and J.-P. Raskin, "(Invited) SOI technologies for RF and millimeter wave applications," *ECS Trans.*, vol. 92, no. 4, pp. 79–94, Jul. 2019, doi: 10.1149/09204.0079ecst.

[2] J. L. Hilbert, *Tunable RF Components and Circuits: Applications in Mobile Handset*. Boca Raton, FL, USA: CRC Press, 2015.

[3] A. Kiayani, V. Lehtinen, L. Anttila, T. Lahteensuo, and M. Valkama, "Linearity challenges of LTE-advanced mobile transmitters: Requirements and potential solutions," *IEEE Commun. Mag.*, vol. 55, no. 6, pp. 170–179, Jun. 2017.

[4] C. Didier and E. Desbonnets. (Mar. 2016). *RF-SOI Wafer Characterization*. Soitec, Bernin, France, [Online]. Available: https://www.soitec.com/en/medias/all-white-papers

[5] Y. Wu, S. Gamble, B. M. Armstrong, V. F. Fusco, and J. A. C. Stewart, "SiO$_2$ interface layer effects on microwave loss of high-resistivity CPW line," *IEEE Microw. Guided Wave Lett.*, vol. 9, no. 1, pp. 10–12, Jun. 1999, doi: 10.1109/75.752108.

[6] H. S. Gamble *et al.*, "Low-loss CPW lines on surface stabilized highresistivity silicon," *IEEE Microw. Guided Wave Lett.*, vol. 9, no. 10, pp. 395–397, Oct. 1999, doi: 10.1109/75.798027.

[7] D. Lederer and J.-P. Raskin, "New substrate passivation method dedicated to HR SOI wafer fabrication with increased substrate resistivity," *IEEE Electron Device Lett.*, vol. 26, no. 11, pp. 805–807, Nov. 2005, doi: 10.1109/LED.2005.857730.

[8] F. Allibert *et al.*, "Engineering SOI substrates for RF to mmWave front-ends," *Microw. J.*, vol. 63, p. 72, Oct. 2020.

[9] M. Rack, L. Nyssens, and J.-P. Raskin, "Silicon-substrate enhancement technique enabling high quality integrated RF passives," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2019, pp. 1295–1298, doi: 10.1109/MWSYM.2019.8701095.

[10] C. R. Neve and J.-P. Raskin, "RF harmonic distortion of CPW lines on HR-Si and trap-rich HR-Si substrates," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 924–932, Apr. 2012, doi: 10.1109/TED.2012.2183598.

[11] C. R. Neve *et al.*, "Impact of Si substrate resistivity on the nonlinear behaviour of RF CPW transmission lines," in *Proc. Eur. Microw. Integr. Circuit Conf.*, Oct. 2008, pp. 36–39, doi: 10.1109/EMICC.2008.4772222.

[12] M. Rack *et al.*, "RF modeling of trap-rich passivated semiconductor substrates: Part II—Parameter impact on harmonic distortion," *IEEE Trans. Electron Devices*, vol. 68, no. 9, pp. 4606–4613, Sep. 2021.

[13] M. Kemp, M. Meunier, and C. G. Tannous, "Simulation of the amorphous silicon static induction transistor," *Solid-Stat Electron.*, vol. 32, no. 2, pp. 149–157, Feb. 1989, doi: 10.1016/0038-1101(89)90182-2.

[14] *Atlas User's Manual*, Silvaco Inc., Santa Clara, CA, USA, Aug. 2016.

[15] T. W. Collins and J. N. Churchill, "Exact modeling of the transient response of an MOS capacitor," *IEEE Trans. Electron Devices*, vol. ED-22, no. 3, pp. 90–101, Mar. 1975, doi: 10.1109/T-ED.1975.18086.