On the Operation Modes of Dual-Gate Reconfigurable Nanowire Transistors

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***Abstract*—We investigate the operation modes of a dual-gate reconfigurable field-effect transistor (RFET). To this end, dual-gate silicon-nanowire FETs are fabricated based on anisotropic wet etching of silicon and nickel silicidation yielding silicide-nanowire Schottky junctions at source and drain. We compare the program gate at source (PGAS) with the more usual program gate at drain (PGAD) operation mode. While in PGAD mode, ambipolar operation is suppressed, switching is deteriorated due to the injection through a Schottky barrier. Operating the RFET in PGAS mode yields a switching behavior close to a conventional MOSFET. This, however, needs to be traded off against strongly nonlinear output characteristics for small bias voltages. Our measurement results are supported by transport simulations employing a nonequilibrium Green's function approach.**

***Index Terms*—Electrostatic doping, lift-off, MOSFET, nanowire, program gate at drain (PGAD), program gate at source (PGAS), reconfigurable field-effect transistor (RFET), silicidation, silicon-on-insulator, tetramethylammonium hydroxide (TMAH).**

I. Introduction

IN RECENT years, device scaling close to the physical limit has spurred the move from geometrical to equivalent scaling [1] of conventional MOSFETs utilizing new device architectures, materials, and integration schemes to continue delivering integrated circuits with higher density and improved performance (power, speed). In addition, fabrication techniques, such as ion implantation, yielding *n*- as well as *p*-type conduction of an intrinsic semiconductor, gradually become less suitable as device structures are being continuously miniaturized into the deep nanoscale. The finite solid solubility of dopants and their increased ionization energy in nanoscale dimensions [2] could lead to increased parasitic resistances and capacitances in the source/drain regions. Furthermore, the statistical nature of ion implantation and dopant diffusion during an activation anneal makes it hard to implement well-defined potential profiles with sharp interface transitions within a small volume of semiconductor material. This leads to a variability in threshold voltage V_{th} from device to device due to random dopant distribution effects [3]. Moreover, the potential landscape created by physical doping stays fixed after an implantation/activation process, which only allows either *n*- or *p*-type unipolar operation.

The aforementioned issues are best addressed if doping in source/drain and channel can be avoided altogether. Recently, reconfigurable field-effect transistors (RFETs) have attracted increasing attention because they utilize electrostatic doping to create virtual *n*-/*p*-regions avoiding dopant-related issues. Moreover, they can be tuned to operate as *n*-/*p*-transistors with unipolar device operation similar to conventional MOSFETs [4]–[8]. Previous work using trigates [4], [5], i.e., two gates for creating virtual source/drain regions and the third one for ON/OFF switching, has demonstrated reconfigurable devices with high I_{ON}/I_{OFF} ratio and steep switching behavior. The adoption of three gates will certainly need more space and might become a key limiting factor for downscaling. Hence, devices using only a dual-gate architecture have been investigated [6]–[8] and the impact of process fluctuations in device fabrication has been studied [9]. In these devices, typically, the gate at the drain side is used to 'program' the device either to *n*- or *p*-type configuration, while the gate at the source side is used as the switching or control gate. However, while unipolar device operation is obtained with this program gate at drain (PGAD) mode, the inverse subthreshold slope is significantly larger than 60 mV/decade. This is obvious since the RFET in PGAD mode is simply a Schottky-barrier MOSFET with suppressed ambipolar operation [10]. In this work, we investigate the rather overlooked device operation mode with the program gate at source (PGAS) and compare it with the PGAD. As it

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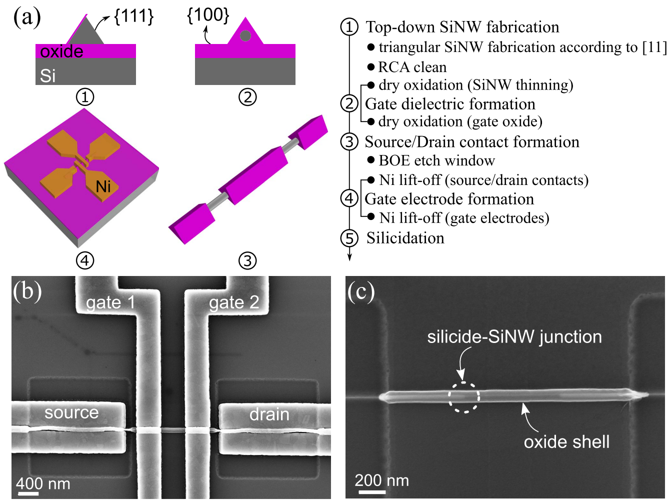

Fig. 1. (a) Schematics (dimension is not to scale) and key process steps in device fabrication. (b) Scanning electron micrographs of the final device after Ni lift-off and silicidation processes and (c) after selective removal of unreacted Ni (including gate electrodes). The dimensions of the device are: oxide thickness $t_{ox} > 15$ nm, diameter of SiNW $d_{SiNW} = \sim 25$ nm, distance between two gates $L_{CG,PG} = 450$ nm, distance between source and drain $L_{S,D} = 2\ \mu$m, and width of each gate $L_G = 500$ nm.

turns out, the PGAS mode yields a steeper switching behavior similar to a conventional MOSFET with the drawback of a larger OFF-state leakage. Furthermore, PGAD and PGAS show a distinctly different nonlinearity in the output characteristics with a stronger effect in the PGAS mode.

II. Device Fabrication

Reconfigurable silicon-nanowire (SiNW) FETs are fabricated using a top-down approach with a two-step wet chemical etching as described in [11]. Tetramethylammonium hydroxide (TMAH) instead of potassium hydroxide (KOH) is chosen as the wet chemical etchant of silicon to ensure a fully CMOS-compatible fabrication process. A {111} facet inclined at 54.74° with respect to the {100} facet is formed due to the distinct etch-rate anisotropy of different crystallographic planes [12] in an alkaline solution (i.e., TMAH) when a silicon nitride hardmask is defined in a line pattern along the [110] direction of a (100)-oriented silicon substrate. Exploiting the ability of SiN to act as effective diffusion barrier enables a local oxidation of the etched {111} facet. After selective removal of the SiN, a triangle bounded by two {111} facets is formed in a second TMAH etching since the {111} facet fabricated with the first TMAH etch step is protected by the grown, local oxide [see Fig. 1(a), step 1]. Atomic force microscopy is used to probe the surface roughness of the wet-etched {111} facet formed on a step structure (step height ~800 nm) in bulk silicon. The measured root-mean-square (rms) value of 0.3992 nm from a rectangular scanning area (800 nm × 250 nm) is well within the range of a commercial prime-grade silicon wafer (rms = 0.2–0.8 nm) [13]. If such a process is carried out on a (100)-oriented silicon-on-insulator substrate (p-type boron-doped, 10^{15} cm^{-3}, top-Si ~80 nm, buried oxide ~145 nm), the buried oxide acts as an etch-stop layer. Hence, the size of the triangle mainly depends on the thickness of the top-silicon layer. After a standard cleaning procedure (i.e., RCA clean [14]), a dry oxidation step is carried out to reduce the size of the SiNW and form a gate oxide at the same time. The dry oxidation is carried out for 3 min at a temperature of 1100 °C, i.e., higher than the viscous flow point. Although such a high temperature prevents a self-limiting oxidation [15], it allows transforming the cross section of the SiNW from triangular to a circular shape while minimizing the degradation of the Si–SiO_2 interface due to roughness induced by the oxidation process [16]. Next, etch windows are patterned in source/drain contact areas and opened up by removing the oxide shell with buffered oxide etch (BOE). Subsequently, nickel contacts and gates are fabricated with electron beam lithography using a bilayer PMMA resist, electron beam evaporation, and lift-off. Finally, the sample is annealed in forming gas (10 % H_2 in N_2) at 450 °C to grow silicide and drive the silicide–SiNW junction underneath the two gate electrodes to avoid a gate underlap and achieve good electrostatic control of the silicide–SiNW junctions. Fig. 1(c) shows this Ni intrusion into a SiNW surrounded by an oxide shell after the selective removal of the unreacted Ni in source/drain regions (which also removes the two gates). Fig. 1(b) shows a scanning electron micrograph of a fully fabricated reconfigurable dual-gate FET.

III. Device Characterization

I–V characteristics of the reconfigurable dual-gate FETs are measured in PGAD and PGAS modes and compared. For both operation modes, a constant voltage applied to the program gate (PG) generates a virtual n- or p-type doping section, whereas the other gate—called control gate (CG)—is used to switch the transistor.

Fig. 2 shows the transfer curves of an RFET in PGAD (blue curves in the left) and PGAS (red curves in the right) operation modes for both n- and p-type configurations with increasing V_{PG} values and their corresponding band diagrams. In the case of PGAD, a virtual n-doped section is created at the drain side if a positive voltage is applied to the program gate. In this case, carrier injection through the source-side Schottky barrier is modulated by different V_{CG} values, which makes the transistor behave similar to a conventional Schottky-barrier MOSFET. Therefore, the ON-state current mainly remains constant even if a larger V_{PG} is applied at the drain side. The transition of carrier injection from thermionic emission to tunneling through the source-side Schottky barrier is reflected in a kink in the transfer characteristic in Fig. 2(c). Such a kink is not visible for the n-type configuration in Fig. 2(a), which means that the Schottky barrier for hole injection is smaller than that for electrons. In the PGAS mode, a virtual n-type source contact is created with a positive V_{PG}, and the behavior of the device is similar to a conventional n-type MOSFET in terms of a steep inverse subthreshold slope. The ON-state current increases with a larger V_{PG} due to the increased carrier injection at the source-side Schottky junction.

Fig. 3 shows the transfer curves of the same device in PGAD and PGAS operation modes for both n- and p-type

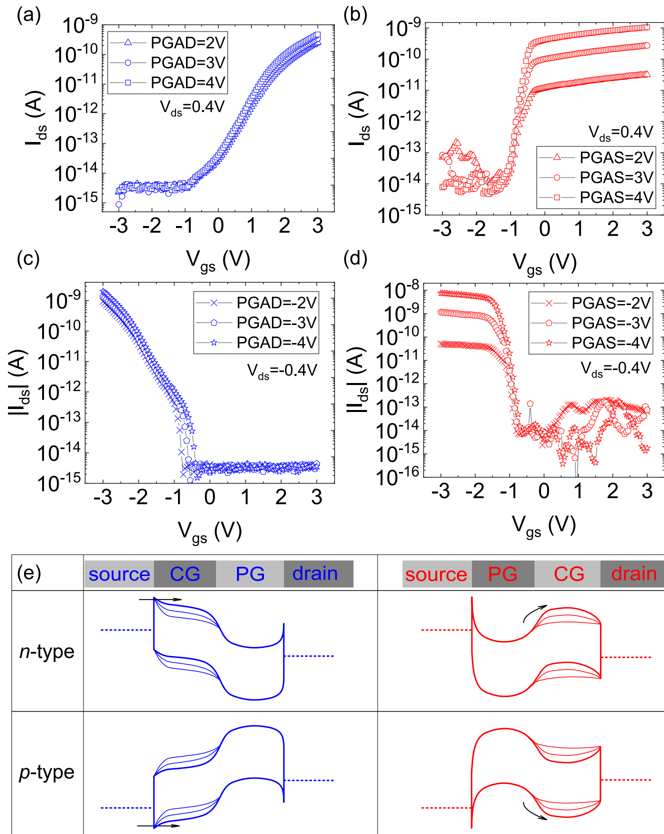

Fig. 2. Transfer characteristics of an RFET for different program gate voltages in (a) PGAD mode for *n*-type configuration, (b) PGAS mode for *n*-type configuration, (c) PGAD mode for *p*-type configuration, and (d) PGAS mode for *p*-type configuration and (e) their corresponding band diagrams. Gate leakage currents (I_{CG} and I_{PG}) are below $\sim 5 \times 10^{-15}$ A and are not plotted for clarity.

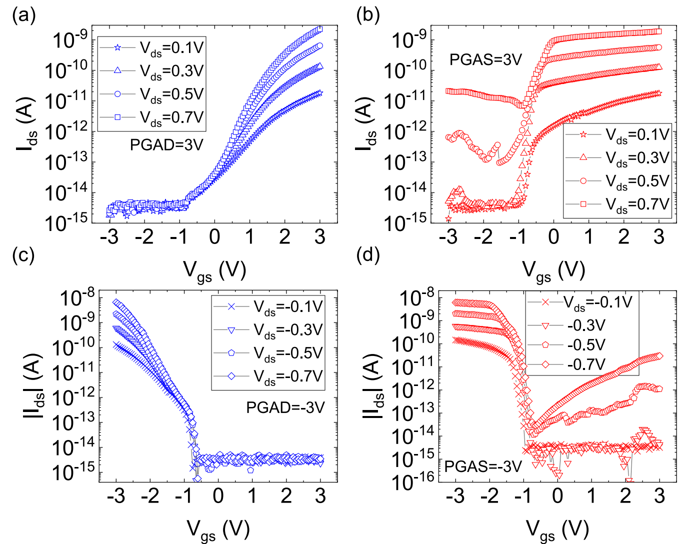

Fig. 3. Transfer characteristics of the same device for different drain–source voltages in (a) PGAD mode for *n*-type configuration, (b) PGAS mode for *n*-type configuration, (c) PGAD mode for *p*-type configuration, and (d) PGAS mode for *p*-type configuration.

configurations with increasing V_{ds} values. A current increase enabled by the modulation of the exit resistance at the drain side is observed for all cases. However, while in PGAD mode, the leakage remains below the measurable threshold due to the particular potential profile throughout the device, larger V_{ds} values lead to an exponential increase in leakage current in the PGAS mode. The reason for this is that in PGAS mode, the ambipolar operation due to an increased carrier injection at the drain-side Schottky junction with increasing V_{ds} is not suppressed. Interestingly, a more or less pronounced kink is observable in the PGAS [see right of Figs. 2 and 3]. While in PGAD, a kink may appear when the carrier injection at source changes from thermionic emission to tunneling with increasing V_{CG} values [see Fig. 2(c)], the kink in the PGAS mode is due to the charge-mediated impact of V_{CG} on the potential distribution of the source-side Schottky barrier. For a large positive (negative) V_{PG}, an almost equilibrium distribution of electrons (holes) is induced in the virtual *n*-type (*p*-type) source contact. When the CG moves the conduction (valence) band down (up), this gives rise to the steep switching of PGAS. However, if the band under the drain-side CG is moved toward the source Fermi level [indicated with three consecutive V_{CG} values in Fig. 2(e) (right)], the carrier density within the virtual source contact is reduced due to the current flow into drain. As a result, the carrier density drops and the band in the virtual source can be moved further downward (upward) giving rise to increased tunneling through the source-side Schottky barrier (see [17, Ch. 7]). Since this further increase of I_d is due to tunneling, a kink occurs. A larger V_{ds} will lead to a larger V_{CG} range of the kink as is indeed observed experimentally [see Fig. 3(d)]. However, it is important to mention that the kink only sets in, when the bands under drain-side CG are moved close to the Fermi level of the source, and hence, a close to ideal inverse subthreshold slope is obtained over several orders of magnitude in the PGAS mode.

It was mentioned above that in a recent publication, the impact of process variability has been investigated in reconfigurable devices in the PGAD mode [9]. In essence, it was found that the variability of V_{th} and I_{ON} is due to work function variation of the source and source-side CG. This is consistent with earlier findings on variability of V_{th} and I_{ON} in Schottky-barrier MOSFETs [18], reconfirming that the PGAD mode basically behaves as a Schottky-barrier MOSFET. Since V_{th} in the PGAS mode does not depend on the source-side Schottky-barrier height, we expect a smaller V_{th} variability (only due to the work function variation of the drain-side CG) compared to the PGAD mode. On the other hand, I_{ON} is limited by tunneling through the source-side Schottky barrier, and hence, it is expected that PGAS and PGAD show a similar I_{ON} variability.

Fig. 4 shows the output curves of the same device in PGAD and PGAS operation modes for both *n*- and *p*-type configurations with increasing V_{CG} values. In the case of PGAD [i.e., control gate at source (CGAS)], a nonlinear current increase in the triode regime is observed, typical of a Schottky-barrier MOSFET. In the PGAS mode, a nonlinear current increase for small bias is also observed. However, in contrast to PGAD, an exponential increase is obtained that is almost the same for all CG voltages shown in Fig. 4(b) and (d);

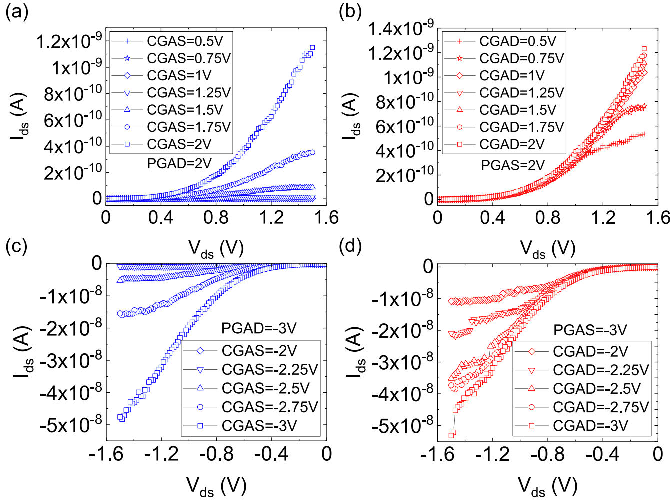

Fig. 4. Output characteristics of the same device for different control gate voltages in (a) PGAD mode for *n*-type configuration, (b) PGAS mode for *n*-type configuration, (c) PGAD mode for *p*-type configuration, and (d) PGAS mode for *p*-type configuration.

a saturation of the current at different levels occurs only for V_{ds} larger than ∼1 V. Both nonlinearities, i.e., in PGAD and PGAS, might deteriorate the functionality of logic inverters built from those devices. This is particularly detrimental to the PGAS mode, leading to a complete loss of noise margin. However, concerning the PGAD mode, it has been shown that highly scaled devices with a short screening length λ (representing the characteristic length on which potential variations are being screened [19], [20]) can also exhibit a linear output characteristic at room temperature due to the strongly increased tunneling probability through the Schottky barrier [8], [21].

The different behavior of the output characteristics of the two device operation modes may at first be surprising since it is generally argued that the nonlinearity of the I_d–V_{ds} curves stems from the forward-biased drain-side Schottky junction. However, this is not the case as we will analyze in the following; while the nonlinearity of the PGAS mode is indeed due to a forward-biased drain-side Schottky junction, the nonlinearity of the PGAD mode is due to an increased tunneling through the source-side Schottky barrier.

IV. Device Simulations

In order to elaborate further on the behavior of RFETs and in particular to understand the difference in the nonlinear behavior of the PGAD and PGAS operation modes, self-consistent device simulations using the nonequilibrium Green's function (NEGF) approach on a finite-difference grid have been carried out [22]. An effective mass approximation with symmetric conduction and valence band is assumed; the complex band structure within the bandgap is considered with Flietner's dispersion relation [23]. To reduce the computational burden, a nanowire FET with 1-D electronic transport is considered. Furthermore, the electrostatics are described by a 1-D modified Poisson's equation where the device architecture is accounted for with a proper choice of the screening length λ.

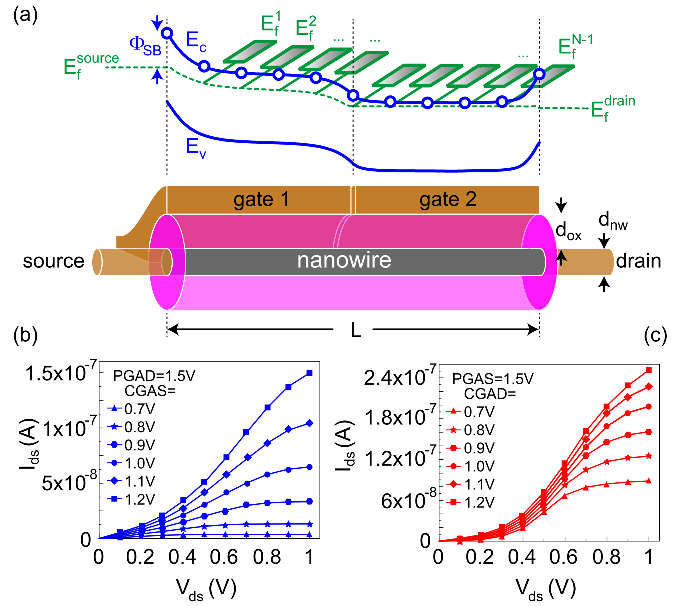

Fig. 5. (a) Schematic of the simulated dual-gate nanowire device. Top: conduction and valence bands (blue lines) on a finite-difference grid. Buettiker probes are connected to each finite-difference site with E_f^i representing the quasi-Fermi level (green dashed line) through the device. Simulated *n*-type output characteristics using the NEGF approach for both (b) PGAD and (c) PGAS operation modes. For the simulation a device with $L = 100$ nm, $d_{nw} = 1$ nm, $d_{ox} = 10$ nm, $E_g = 1$ eV, $m^*_{c,v} = 0.1m_e$, and a scattering mean free path of 15 nm are assumed.

It is important to note that these assumptions will certainly not allow a quantitative comparison between experiment and simulation. However, qualitatively they replicate the experimental situation rather well and the approach has been used successfully to reproduce and explain the device behavior of conventional as well as Schottky-barrier field-effect transistors (see [24], [25]).

An important ingredient here is the inclusion of Buettiker probes [see Fig. 5(a)], i.e., virtual contacts attached to the channel of the RFET that mimics inelastic scattering [26]; the Fermi levels of all Buettiker probes are determined to ensure a net zero current from/into each Buettiker probe, thus representing the quasi-Fermi level within the device. Fermi-level pinning with a midgap position of the source/drain Fermi level yielding a Schottky barrier of $\Phi_{SB} = E_g/2$ is assumed at the interface between source/drain and the channel; all other device parameters are stated in Fig. 5.

Fig. 5 shows simulated output characteristics in (b) PGAD and (c) PGAS operation modes for *n*-type configuration, qualitatively reproducing the experimental results shown in Fig. 4. In particular, the strong nonlinear current increase for small bias in the PGAS mode compared to PGAD is observed.

Fig. 6 shows a single I_d-V_{ds} curve for PGAD = 1.7 V and CGAS = 0.8 V and PGAS = 1.7 V and CGAD = 0.8 V, showing clearly the different behavior of the two device operation modes; while PGAD exhibits an almost linear behavior in the region of small bias,[1] PGAS shows a strong nonlinearity.

[1]Note that this is the case due to the large difference in V_{PG} and V_{CG}. For larger CG voltages as shown in Fig. 5(b), the output characteristics also become nonlinear in the PGAD mode.

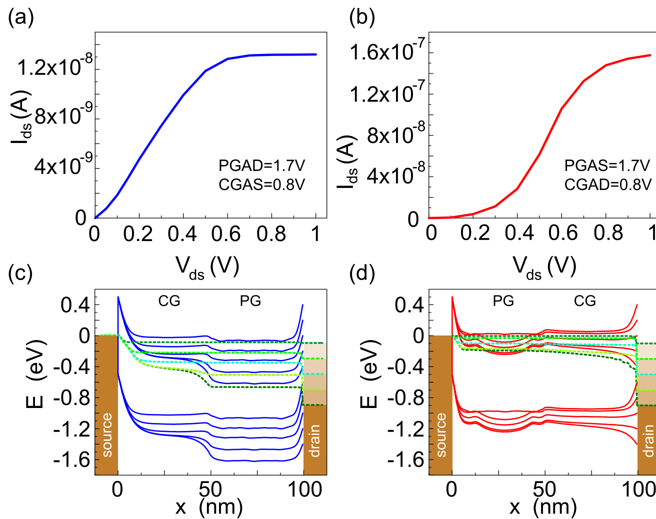

Fig. 6. Output characteristic for (a) PGAD = 1.7 V and CGAS = 0.8 V and (b) PGAS = 1.7 V and CGAD = 0.8 V. Bottom: conduction/valence band profiles for V_{ds} = 0.1, 0.3, 0.5, 0.7, 0.9 V together with the quasi-Fermi level in (c) PGAD device operation mode [same gate voltages as in (a)] as well as (d) in the PGAS mode [same gate voltages as in (b)].

The reason for this different behavior becomes obvious when comparing Fig. 6(c) and (d); in PGAD, the quasi-Fermi level (green dashed lines) at the drain end, i.e., underneath gate 2, drops substantially with increasing bias. This is due to a loss of carrier injection from the drain such that the conduction/valence bands are moved to lower energies because of the large V_{PG} at gate 2. As a result, the device does not behave like a forward-biased Schottky junction. Opposed to this, the small nonlinearity observed in PGAD [see Fig. 6(a)] stems from an increased tunneling through the source-side Schottky diode with increasing V_{ds} due to a significant reduction of the carrier density underneath the control gate [see Fig. 6(c)]. Note that the same is true in conventional, single-gate Schottky-barrier MOSFETs [17]. In contrast, in the case of PGAS [Fig. 6(b) and (d)] the quasi-Fermi level remains rather fixed by the source contact and increasing the bias yields a forward-biased Schottky junction with an exponential increase of the current. This rather undesirable behavior strongly deteriorates, e.g., the performance of inverters made of RFETs operated in the PGAS mode.

In conclusion, with only two individually controllable gates, the PGAS mode yields an almost ideal switching behavior, while its output characteristics are deteriorated when compared to PGAD, which exhibits improved output but deteriorated transfer characteristics.

V. Conclusion

Reconfigurable FETs with wet chemically etched SiNWs and Ni silicidation are fabricated and characterized for both PGAD and PGAS operation modes. The top-down fabrication approach yields localized SiNWs with atomically flat surfaces and minimal plasma damage manufacturable with conventional h-line contact lithography. The one-step silicidation process at 450 °C creates a silicide composition that has a Fermi level close to the valance band of silicon. In the PGAD mode, the dual-gate RFET is a Schottky-barrier MOSFET with suppressed ambipolar behavior. The price paid for a lower OFF-state leakage current and more unipolar device behavior is a larger inverse subthreshold slope. In the PGAS mode, the RFET demonstrates a steeper inverse subthreshold slope comparable to a state-of-the-art conventional MOSFET. However, V_{ds} should be kept low to prevent leakage increase induced by the other carrier type. The quasi-Fermi level through the device, as simulated with Buettiker probes mimicking scattering, explains the difference in output characteristics for both PGAD and PGAS operation modes.

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