# Threshold Switching Enabled Sub-pW-Leakage, Hysteresis-Free Circuits

Bojun Cheng, *Member, IEEE*, Alexandros Emboras, Elias Passerini, Mila Lewerenz, Ueli Koch, Lianbo Wu, Jiawei Liao, *Graduate Student Member, IEEE*, Fabian Ducry, *Member, IEEE*, Jan Aeschlimann, Taekwang Jang, Mathieu Luisier, and Juerg Leuthold, *Fellow, IEEE*

***Abstract*— In this article, we present ultralow leakage logic circuits by combining 3-D memristors with CMOS transistors. Significant leakage current reductions of up to 99% are found by experiments and simulation for a memristive hybrid-inverter if compared with a conventional inverter. Likewise, circuit simulations of memristive hybrid ring oscillators, NAND, or full adders show more than 100% gain in energy efficiency per cycle over state-of-the-art circuits. Importantly, the memristive circuits offer hysteresis-free operation. The hysteresis-free operation is due to properly engineered properties—such as the threshold voltage—of the memristors to match the circuit, as well as the self-adaptive filament diameter of our memristor during operation. Lastly, the memristors feature a $10^8$ ON–OFF ratio, enabling both high speed and low leakage (~10 fA) when integrated with a transistor. They also come with a well-controlled filament formation on a ~10-nm footprint, making them ideal to integrate with modern CMOS technology transistors.**

***Index Terms*— Digital circuits, FETs, hybrid FET, leakage currents, memristor, near-threshold computing, steep slope transistor.**

## I. Introduction

LOWEST power consumption is of critical importance in all electronic applications where the power supply is limited. This is more and more common in edge computing for Internet of Things (IoT) devices [1] and portable embedded systems [2], where reduction of power consumption can increase battery charge intervals. In the former case (IoT), chips composed of a sensor and a CMOS control circuit often operate at sampling rates below 1 kHz [3]. Consequently, the leakage (static) power between two consecutive events can be significant compared to the dynamic power consumption. In the latter case (portable systems), circuits operate at a sub- or near-threshold supply voltage ($V_{DD}$), which improves the energy efficiency of FETs in a quadratic way at the cost of increased delay and lowered speed. In both types of application, lowering the leakage power of CMOS circuits can further reduce the power consumption and increase the lifetime of the battery. However, the Boltzmann tail of the electron distribution in conventional CMOS logic imposes a fundamental limit of 60 mV/decade to the subthreshold swing (SS) of the drain current at room temperature [4]. As a result, maintaining a high dynamic current requires either to increase the leakage current or the supply voltage and dynamic power.

To overcome the 60-mV/decade limit, steep-slope transistors are getting a lot of attention. Among many approaches, the so-called hyper-FET (or hybrid-FET) in combination with a resistive switching (RS) device is a very attractive candidate [5]. So for instance, hybrid-FETs with sub 60-mV/decade SS have been demonstrated by connecting a phase change material (PCM) to the source terminal of an FET [6]. The PCM-FET utilizes metal–insulator transitions to achieve steep switching.

As an alternative to PCMs, filament-based threshold switching (TS), also known as conductive bridging random access memory (CBRAM)-type memristors [7], [8], offer steep switching, low switching voltage, low energy consumption, high ON/OFF ratios, and small footprint. Hybrid-FETs with filament-based TS have been demonstrated with an SS below 5 mV/decade [9], [10].

Circuits with steep-slope hyper-FETs have been proposed. For example, simulation with PCM-FETs predicts an improvement of speed and power consumption for various circuits comparing to conventional CMOS implementations [11]–[13]. We note that the PCM switchings are current or temperature-induced. This may pose some additional challenges to conventional circuit design as the current and temperature have a strong dependence on the load capacitance and transistor variations. A steep-slope circuit concept that eliminates the hysteresis regardless of its load capacitance and transistor variation is therefore of high relevance.

In this work, we combine a filament-based, voltage-controlled TS device (or volatile memristor) with FETs to form a hybrid memristive circuit technology with ultralow leakage and no hysteresis. We have recently

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Bojun Cheng, Elias Passerini, Mila Lewerenz, Ueli Koch, and Juerg Leuthold are with the Institute of Electromagnetic Fields (IEF), ETH Zurich, 8092 Zurich, Switzerland (e-mail: bojun.cheng@ief.ee.ethz.ch).

Alexandros Emboras, Lianbo Wu, Jiawei Liao, Fabian Ducry, Jan Aeschlimann, Taekwang Jang, and Mathieu Luisier are with the Integrated Systems Laboratory (IIS), ETH Zurich, 8092 Zurich, Switzerland.

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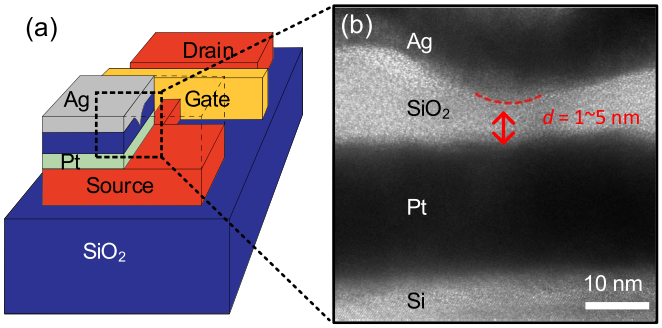


Fig. 1. Concept of our memristive FET circuits. (a) Schematic drawing of a 3-D TS device integrated onto a FinFET. (b) HRTEM image of the 3-D TS device. A clear tip shape of the Ag electrode can be seen.

reported TS memristive devices [14] with currents below 10 fA in the high-resistance state (HRS) and low switching voltage of 0.4 V. Here, we experimentally demonstrate a hysteresis-free operation of memristive circuit blocks using TS with a static power reduction of ∼99% as compared to a CMOS reference. Also, based on our experimental results, a doubling of energy efficiency over state-of-the-art transistors can be achieved in near-threshold computing applications.

## II. Low-Leakage Threshold Switch

The TS memristive-circuit element to be subsequently used is depicted in Fig. 1(a). A 3-D TS device is put in series with the pull-down path of the nFET. It acts as a basic low-leakage circuit element and constitutes a memristive nFET. The TS device features a top electrode that has a unique 3-D tip to confine the memristive operation and limit the leakage current to the tip apex [10]. Fig. 1(b) shows a fabricated TS device in a cross-sectional high-resolution transmission electron microscopy (HRTEM) image. The TS device has an active device area of less than 20 × 20 nm$^2$, therefore it can be easily integrated on the source (drain) contact of any FET. The distance $d$ between Ag and Pt at the apex of the tip can be accurately controlled to adjust the switching-threshold voltage ($V_{\text{th}}$) [14]. The small footprint is particularly beneficial for cointegration with advanced MOSFET technology nodes. The CMOS-compatible $SiO_2$ matrix within the TS device allows for a fabrication in the back end of line (BEOL) process.

Fig. 2 shows the switching cycle of the memristor. First, the applied voltage ($V_m$) is swept at a rate of 10 mV/s. The measured current is plotted against the applied voltage in Fig. 2(a). A current compliance limit of 1 $\mu$A is applied during voltage sweep, which is then drawn as the gray dashed line. When compliance current is reached, the applied $V_m$ differs from the actual voltage on the TS device and therefore does not determine the LRS resistance. The LRS resistance is determined in Fig. 2(b) and (c) in the next paragraph. The measured average HRS current is around 10 fA. This is among the lowest of its kind and will be the reason for the significant reduction of leakage power consumption in our memristive circuits. The ultralow HRS current stems from the device design, which keeps the area of the active surface minimal. The switching voltage to a low-resistance state (LRS) of the TS device is $V_{\text{th}} \approx 0.4$ V. Note, $V_{\text{th}}$ can be tuned through the

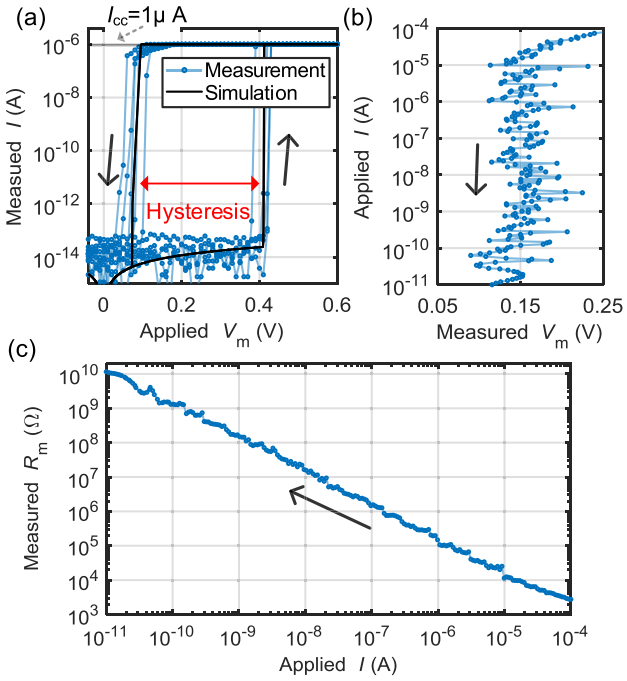


Fig. 2. Experimental characterization of our TS device. (a) Measured $I$–$V$ hysteresis during voltage sweep, five consecutive cycles (blue). The respective simulated $I$–$V$ curve based on a Verilog-A model is given in black. (b) Measured voltage during the current sweep. The steep transition indicates an almost-infinite transconductance $g_m = \Delta I/\Delta V_m$. (c) Measured TS resistance of the LRS during the current sweep of (b). The resistance is approximately inversely proportional to the current. This indicates a self-adaptive feature of the filament's diameter to accommodate the external current.

fabrication method from ∼0.15 to 1 V [14], [15], which allows for flexible matching to the range of valid threshold voltages ($V_{\text{th}}$) of each circuit, which in turn depends on the $V_{\text{DD}}$. At the switching point, the current abruptly increases by a factor of $10^8$. The device switches back to HRS at $V \approx 0.08$ V. This volatile behavior makes it suitable for circuit integration as no memristive reset at negative voltages is needed.

In addition, starting from the LRS, we sweep down the compliance current logarithmically from 100 $\mu$A to 10 pA in ∼10 s and measure the voltage ($V_m$) on the device. The result is plotted in Fig. 2(b). The voltage is almost constant at $V_{m,\text{hold}} \approx 0.15$ V through most of the current range. This is a consequence of the volatile nature of the metallic filament. We also plot the resistance of LRS as a function of the compliance current in Fig. 2(c). As one can see, the LRS resistance is approximately inversely proportional to the current. In summary, the filament adapts its diameter, and thus its conductance, to the current to retain a constant voltage. This self-adaptive characteristic drastically reduces the hysteresis and is discussed in Section III.

For subsequent circuit design, the $I$–$V$ characteristics of the 3-D TS device have been simulated with Verilog-A using a linear hypothesis [16], [17] to describe the filament expansion and dissolution. The simulated characteristics of the atomic switch are shown by the black line in Fig. 2(a). The threshold voltages, as well as the leakage current, agree very well with the experimental data.

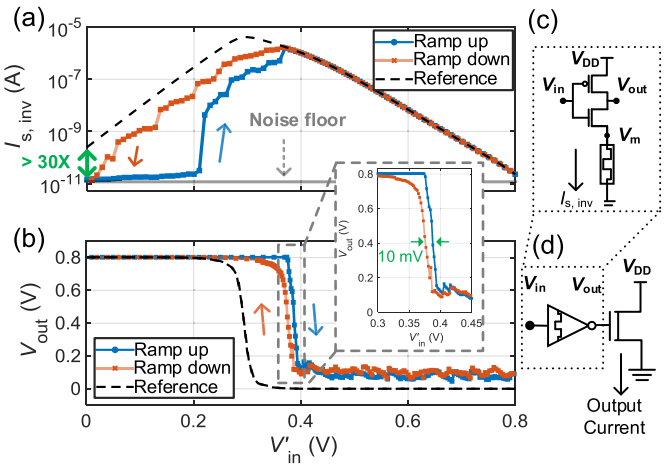


Fig. 3. Experimental characterization of the memristive inverter. For better readability, we use $V'_{\text{in}} = V_{\text{in}} + 0.55$ V as the $x$-axis. (a) Typical $I_{s,\text{Inv}} - V_{\text{in}}$ measurement of the memristive inverter with ramp up (blue) and ramp down (red). The noise floor is indicated in dashed gray. The measurement of the reference inverter without a memristor is shown in black. (b) $V_{\text{out}} - V_{\text{in}}$ plot of the same device. A zoomed-in view of the transition is shown in the inset. (c) Circuit diagram of the memristive inverter. (d) Circuit to derive the inverter $V_{\text{out}}$ by measuring the nFET output current.

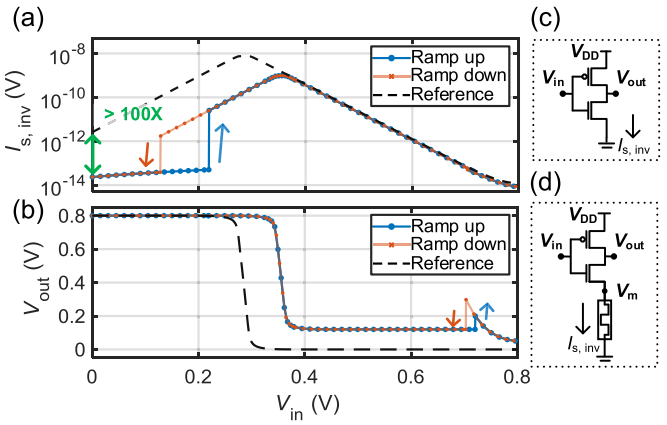


Fig. 4. Simulation of a memristive inverter. (a) Simulation of $I_{s,\text{Inv}} - V_{\text{in}}$ with ramp up (blue) and ramp down (red). Reference inverter without memristor is plotted in black. (b) Simulation of $V_{\text{out}} - V_{\text{in}}$. Inset: circuit diagram. The circuit is similar to the experimental circuit used in Fig. 3(a). (c) Circuit diagram of reference inverter. (d) Circuit diagram of the memristive inverter.

## III. Hysteresis-Free Memristive Inverter

The fabricated low-leakage, hysteresis-free memristive inverter consists of a 3-D filamentary TS device connected to the source of the nFET of an ordinary inverter. Fig. 3(c) shows the circuit diagram.

### A. Experimental Verification

The static current of the memristive inverter as a function of the input voltage, swept at a rate of ∼20 mV/s, is plotted in Fig. 3(a). We keep $V_{\text{DD}} = 0.8$ V throughout the whole experiment. Additionally, the same inverter without the TS device is measured as a reference (black dashed line). A leakage reduction by more than 30 times is obtained with the TS device, which is only limited by the noise floor of ∼10 pA of the measurement setup. In our demonstration, due to the challenge of finding a matching nFET with a leakage of ∼0.1 nA at $V_{\text{in}} = 0$ V, we use a depletion mode nFET with leakage of ∼0.1 nA at $V_{\text{in}} = -0.55$ V, which results in an inverter with a negative logic threshold voltage. If the TS device would be paired with an accumulation mode nFET, the logic threshold voltage of the memristive inverter would be positive. To mimic the matching nFET, we shift the $x$-axis by 0.55 V for better readability, i.e., $V'_{\text{in}} = V_{\text{in}} + 0.55$ V.

$V_{\text{out}}$ in Fig. 3(b) indicates a hysteresis-free switching behavior. More precisely, at $V'_{\text{in}} = 0.39$ V, one can see a small difference of approximately 10 mV between the ramp up and ramp down phases, which is magnified in the inset of Fig. 3(b). The hysteresis is much smaller than the 40-mV switching slope of the reference inverter (0.27∼0.31 V). We, therefore, consider our memristive circuit hysteresis-free. Here, the output voltage ($V_{\text{out}}$) is extracted from the measured output-current and $I$–$V$-characteristics of an additional nFET [see inset of Fig. 3(d)]. In the range from $V'_{\text{in}} = 0.4$ V to $V'_{\text{in}} = 0.8$ V, we can see that $V_{\text{out}} \approx 0.12$ V. This value is approximately equal to the voltage $V_m$ dropping off across the TS device. Its magnitude can be attributed to the fact that the TS device adapts its filament diameter and resistance based on the current to keep a voltage of $V_{m,\text{hold}} \approx 0.12$ V, similar to what is observed in Fig. 2(b).

### B. Leakage Current and Output Voltage Simulation

To accompany the experimental demonstration and characterize the proposed memristive-FET technology, circuit modeling is used.

Fig. 4(a) shows the simulated static current $I_{s,\text{inv}}$ of the memristive inverter and compared to a reference structure without memristor (black dashed line). Note that this is the static current (short-circuit current) at a given voltage. The dynamic current to charge and discharge the capacitors can be much higher and is discussed in the next section. The leakage current is confirmed to be lowered by a factor in the order of 100 compared to a reference inverter without memristor (black dashed line).

The simulated output voltage of the memristive inverter is given in Fig. 4(b). During ramp up, the TS switches to LRS and back to HRS at $V_{\text{in}} = 0.22$, 0.72 V respectively, marked by the blue arrows. During ramp down, the TS switch to LRS and back to HRS at $V_{\text{in}} = 0.7$, 0.14 V, respectively, marked by the red arrows. At LRS, the self-adaptive characteristics of the TS filament result in a constant voltage across the TS as $V_m = V_{m,\text{hold}} = 0.12$ V. The TS is in LRS from 0.22 to 0.7 V during both ramp up and ramp down, therefore $V_{\text{out}}$ is not hit by any hysteresis in this range. This also implies a hysteresis-free operation around $V_{\text{in}} = 0.35$ V where the inverter switches its logic state.

Instead, the hysteresis of the memristive device occurs between $V_{\text{in}} = 0.72$ V during ramp up and $V_{\text{in}} = 0.7$ V during ramp down. Even though the memristive-nFET exhibits a small hysteresis at ∼0.7 V, in practice, this hysteresis has little impact on the $V_{\text{in}} - V_{\text{out}}$ characteristic of the inverter as its range is outside of the voltage range where the inverter flips.

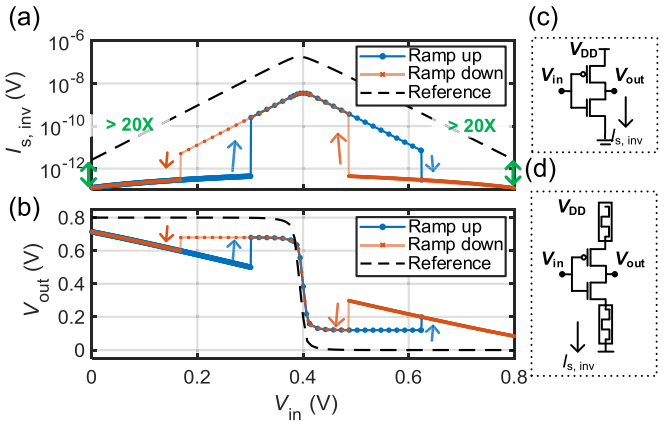


Fig. 5. Simulation of a double-sided memristive inverter. (a) $I_{s,\mathrm{Inv}} - V_{\mathrm{in}}$ with ramp up (blue) and ramp down (red). Reference inverter without memristors plotted in black. (b) Simulation of $V_{\mathrm{out}} - V_{\mathrm{in}}$. (c) Circuit diagram of reference inverter. (d) Circuit diagram of the double-sided memristive inverter.

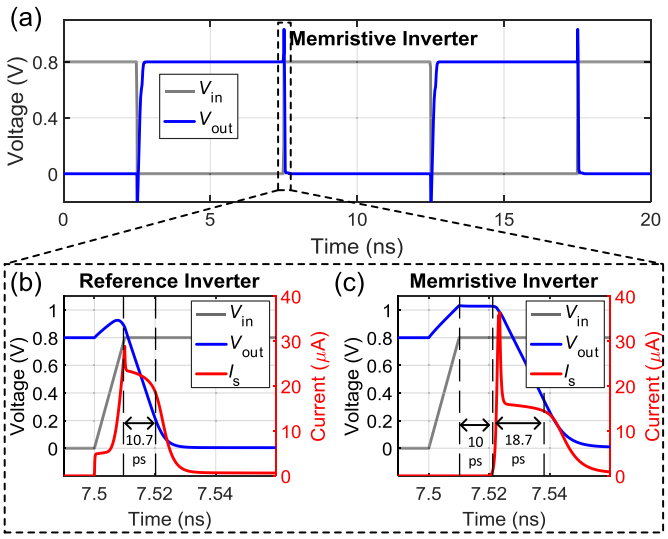


Fig. 6. Dynamic simulation results of the memristive inverter on the 22-nm SOI platform. (a) $V_{\mathrm{in}} - V_{\mathrm{out}}$ sequence. The memristive inverter returns the expected inverted output. (b) and (c) Zoomed-in view of the output falling edge of the reference and the memristive inverter. An extra delay of 10 ps from switching and a prolonged transition time can be seen.

By engineering the TS and FET parameters, the remaining hysteresis window does not interfere with the static operation points at 0.05 and 0.8 V.

### C. Double-Sided Memristive Inverter

A leakage reduction on both the nFET and pFET can be obtained by attaching the TS devices to both the nFET and pFET. The corresponding circuit diagram is shown in Fig. 5(d). The leakage reduction occurs at the cost of degradation of the output voltage swing. The stronger the leakage reduction, the higher the voltage swing degradation. In the case of a double-sided memristive inverter, the output voltage swing degradation is two times larger than for a single-sided memristive inverter, as each TS will contribute to the degradation. To maintain a voltage swing between 0.085 and 0.715 V (~80% of the $V_{\mathrm{DD}}$), the leakage cannot be reduced by a factor much larger than 20, instead of a factor above 100 (Fig. 4), as shown in Fig. 5(a). As in Fig. 5(b), we also observe a hysteresis-free switching at $V_{\mathrm{in}} = 0.40$ V. The two TS devices introduce two small hysteresis windows at $V_{\mathrm{in}} = 0.3$ V and $V_{\mathrm{in}} = 0.62$ V during ramp up and $V_{\mathrm{in}} = 0.17$ V and $V_{\mathrm{in}} = 0.49$ V during ramp down. Both hysteresis windows (0.170.3, 0.490.62 V) are again outside the voltage range of relevance.

Since the double-sided memristive circuit has the same working principle as a single-sided memristive circuit, for the sake of simplicity, we restrict the subsequent discussion on the power consumption to the single-sided memristive inverter (Fig. 4). Although for double-sided memristive circuits, the leakage reduction, as well as the potential energy-saving might be less significant compared to the single-sided memristive circuit, it is still beneficial compared to the standard CMOS circuits. There is a similar trade-off between energy-efficiency and output voltage swing in both cases, and the operation point can be tuned to the intended application, such as IoT or near-threshold computing.

## IV. Memristive Circuits for IoT Devices

To predict the power consumption of our memristive circuit approach in realistic applications in IoT devices, we replaced the original transistor model in Verilog-A with a model corresponding to the 22-nm silicon-on-insulator (SOI) process with a channel length of ~20 nm, close to the state-of-the-art. The switching speed of the memristor was also adapted to 10 ps, according to indications of switching dynamics found in similar devices [18]. The test circuit consists of a fan-out-of-4 (FO4) memristive inverters.

The simulated input and output voltages of the resulting memristive inverter are plotted in Fig. 6(a). When $V_{\mathrm{in}}$ switches from $V_{\mathrm{DD}}$ to 0 V, $V_{\mathrm{out}}$ goes from 0 V to $V_{\mathrm{DD}}$. During this process, the memristor remains in its HRS and there is little difference with the behavior of a reference inverter without memristor. Yet, when $V_{\mathrm{in}}$ switches from 0 V to $V_{\mathrm{DD}}$, the switching processes of the reference and memristive inverter differ, as illustrated in Fig. 6(b) and (c). The memristor switches to its LRS of 5 kΩ after a delay of 10 ps, which is indicated by the rise of $I_s$. As a result, the transition time increases from 10.7 to 18.7 ps with a memristor.

The dynamic and static power consumption per cycle, as well as their ratio, are shown in Fig. 7 as a function of the switching frequency. Due to the presence of a TS device in the memristive circuit, the static power of the memristive inverter (blue straight line) is reduced by a factor of 150 over the static power consumption of the reference inverter (black straight line), while the dynamic power only increases by approximately 5% (dashed plots around 1 fJ). The energy savings are plotted in green in Fig. 7 as a function of the operation frequency. Below 100 kHz the static power consumption dominates over the dynamic and the memristive inverter features a lower total power consumption than the reference inverter. This favorable power consumption performance makes the memristive inverter suitable for sensor applications where low sampling rates suffice. The memristive inverter saves more than 50% energy at 1 kHz and even more at lower frequencies.

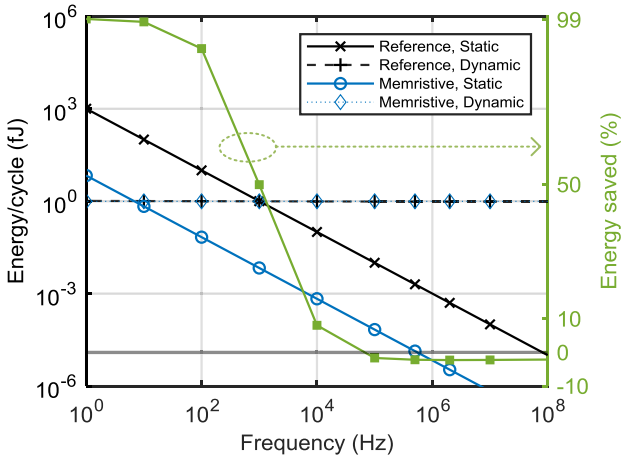


Fig. 7. Static and dynamic energy for memristive and reference inverters as a function of frequency. The total energy saved when we use the memristive inverter is shown in green on the right axis. The memristive inverter saves more than 50% energy at a frequency of 1 kHz and much more at lower frequencies.

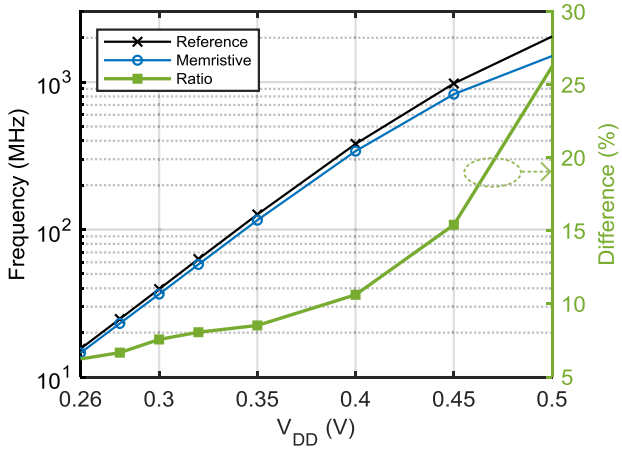


Fig. 8. Frequency (black, left axis) for memristive and reference RO as a function of $V_{DD}$ and the frequency difference in percentage (green, right axis).

TABLE I
TS MODEL PARAMETERS

| Parameters | IoT Sensing | Near-threshold computing |
|---|---|---|
| $V_{DD}$ | 0.8 V | 0.26~0.45 V |
| $V_{th}$ | 0.4 V | 0.17~0.26 V |
| HRS | 17 TΩ | 8 GΩ |
| LRS | 5 kΩ | 5 kΩ |

This demonstrates that the proposed memristive-FET circuit is advantageous for low-frequency IoT devices in terms of power consumption.

## V. Memristive Circuits for Near-Threshold Computing

Following the same approach as for low leakage IoT circuits, we now focus on near-threshold computing. As we lower the $V_{DD}$ from 0.8 V by more than a half, for the best performance-energy balance, we also select transistors with lower threshold voltage and higher leakage. Moreover, to ensure an output voltage swing larger than 80% of the $V_{DD}$, the leakage reduction is set to 20×. As a consequence, we exchange the TS by a lower switching-threshold voltage ($V_{th}$) device to match the transistor characteristics. The parameters of the standard and lower-switching threshold TS are given in Table I. It is worth noting that both models are based on experimentally demonstrated TS devices we fabricated [10], [14]. In addition, $V_{th}$ is adjusted to best match $V_{DD}$.

However, process variations and random telegraph noise do not scale well with $V_{DD}$. When the $V_{DD}$ is too low, these factors will limit the reliability and makes circuits impractical [19], [20]. For this reason, we constrain our $V_{DD}$ range to $V_{DD} \geq 0.26$ V.

### A. Voltage-Delay Analysis

To determine the performance in terms of delay and speed, we have performed extensive memristive inverter simulations. We have used an 11-stage ring oscillator (RO) constructed using CMOS inverters without TS devices attached to the pull-down path as a reference. The simulation results are depicted in Fig. 8. With the introduction of the TS devices in the RO, a slight reduction of the RO's fundamental frequency can be seen. However, the frequency difference remains below 10% for the operation regime at $V_{DD} < 0.38$ V. This is the $V_{DD}$ regime with a lower dynamic energy per cycle, which is of high interest for low power applications, as discussed in the following.

We have run additional simulations where device variability is accounted for. We used the 11-stage RO and at $V_{DD} = 0.45$ V and a TS switching voltage $V_{th} = 0.26$ V. As shown in Table II, for typical–typical (tt), slow–slow (ss), fast–slow (fs), the frequency difference between the memristive and reference RO is within 20%. For fast–fast (ff) and slow–fast (sf), as the frequency is above 1 GHz, the TS device further limits the RO's operating speed. Moreover, for the variability of the TS, we considered a broad range of $V_{th}$ TS at all corners with $V_{DD} = 0.45$ V. The RO at all corners works with $V_{th}$ values from 0.21 to 0.33 V. When $V_{th} > 0.33$ V, the TS will not easily switch on during the $V_{in} = 0 \rightarrow V_{DD}$ transition for the sf corner. Then, when $V_{th} < 0.21$ V, it may switch to the LRS at undesired voltage swing for the fs corner.

### B. Energy Analysis

We now evaluate the potential energy saving of logic circuits employing the TS devices. For this, we use the simulations from Fig. 8 to extrapolate the delay performance of a typical logic circuit. Without loss of generality, we assume that our model circuits are able to operate at 5% of the fundamental frequency of the 11-stage RO. These operation frequencies are much lower than what the 11-stage RO would permit. Operation at 5% of the maximum frequency of a simple RO is reasonable. The maximum operation frequency would depend on actual implementations and applications though. The chosen ratio yields realistic optimum operation points for the technology in question below.

TABLE II
CORNER SIMULATION OF RO FREQUENCY

| Corner | Reference RO | Memristive RO |
|---|---|---|
| tt | 979.3 MHz | 796.5 MHz |
| ff | 3641 MHz | 2020 MHz |
| sf | 1901 MHz | 1372 MHz |
| fs | 375.7 MHz | 319.5 MHz |
| ss | 138 MHz | 125.7 MHz |

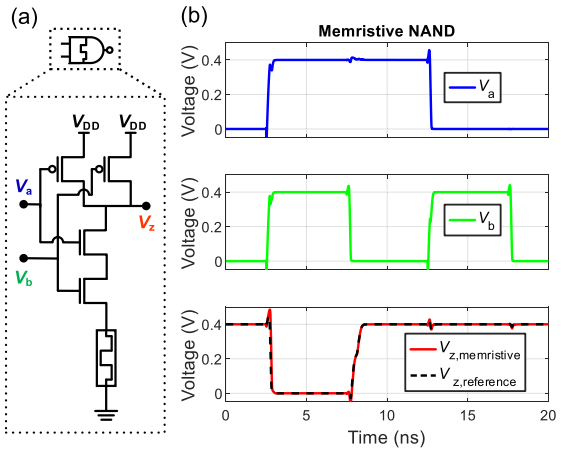


Fig. 9. Demonstration of NAND logic. (a) Circuit diagram of the memristive NAND. (b) Input and output voltage sequences. The output of memristive and reference NAND are given in red and black, respectively. Only when both $V_a$ and $V_b$ are high (between 2.5 and 7.5 ns), $V_z$ is low.

Fig. 9(a) shows the circuit diagram of a memristive NAND, which is considered among the fundamental building blocks for a digital circuit. We use the same nFET and pFET as we used for the RO. A sequence of voltage inputs $V_a$, $V_b$, and output $V_z$ is reported in Fig. 9(b), with $V_{DD} = 0.4$ V, demonstrating its proper functionality.

The energy consumption result as a function of $V_{DD}$ is given in Fig. 10. Fig. 10(a) shows the static and dynamic energy per cycle for both the memristive and reference NAND. The energy is defined as the average over all transitions from each of the four input states to another state. The static power is the average over four static states. With the memristive NAND, the leakage energy is reduced by ∼95%. In addition, the TS switching delay also eliminates the short-circuit current [21]. As a result, the dynamic power of the memristive NAND at $V_{DD} < 0.4$ V is lower than that of the reference NAND.

Fig. 10(b) shows the total energy per cycle as a function of $V_{DD}$. For the reference NAND, the total energy per cycle reaches its minimum of 33.4 aJ (highest efficiency) at $V_{DD} =$ 0.4 V. The lowest total energy per cycle of the memristive NAND is 15.8 aJ at $V_{DD} = 0.26$ V, where it is more than 52% smaller than the minimum energy of the reference NAND. This corresponds to an efficiency gain of 111%. Note that we restrict $V_{DD}$ to be higher than 0.26 V. Lower values would not be practical, though it can be inferred that the performance gain could be even higher at lower $V_{DD}$.

The memristive NAND lowers the leakage current significantly (∼20×) and therefore effectively shifts the energy optimal operation voltage of a circuit to a lower value. Like most design parameters, this effect can be exploited by a designer to achieve different energy-delay trade-offs. As an

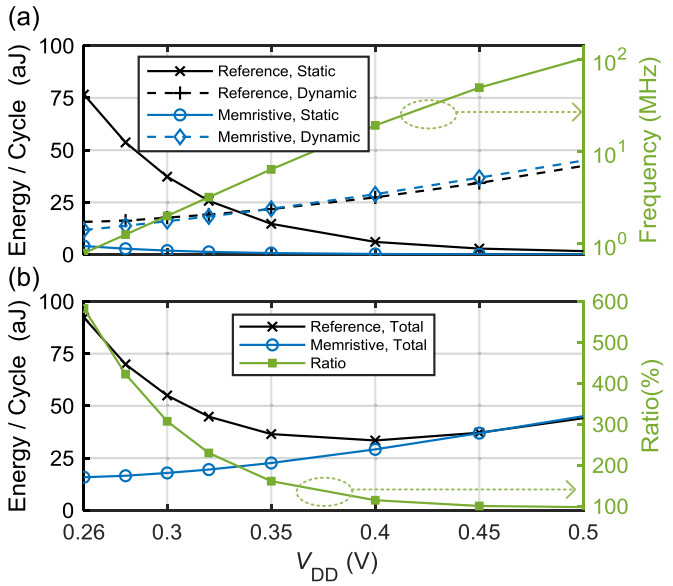


Fig. 10. (a) Static and dynamic energy per cycle for memristive and reference NANDs as a function of $V_{DD}$. Right axis: frequency of the NAND. (b) Total energy per cycle for memristive and reference NAND as a function of $V_{DD}$. Right axis: the ratio of the reference and memristive total energy.

TABLE III
FULL ADDER PERFORMANCE COMPARISON. $V_{DD} = 0.4$ V

| Full Adder | Static Power | Dynamic Power | Efficiency Gain |
|---|---|---|---|
| Reference | 1.12 nW | 6.54 nW | |
| Memristive | 0.059 nW | 6.67 nW | +13.9% |

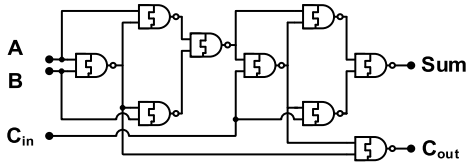


Fig. 11. Circuit diagram of the memristive full adder. It consists of nine memristive NAND, as depicted in Fig. 9.

example, the nFET threshold voltage could be further reduced, increasing the operation speed at the expense of increased leakage. In fact, for the result of the memristive NAND reported in Fig. 10, a 10% increase in leakage (0.4 aJ at $V_{DD} = 0.26$ V) would completely compensate for the performance loss of the TS device at $V_{DD} = 0.26$ V, while still maintaining an overall 106% efficiency gain. This way, the memristive circuit offers an additional tuning parameter to allow designers to adapt their circuits over a broader range.

### C. Memristive Full Adder

As the last illustration, we constructed a memristive full adder with nine memristive NAND gates (see Fig. 11). We simulated its characteristics at $V_{DD} = 0.4$ V, $f = 20$ MHz, which is the optimal operation point of the reference circuit. The corresponding static and dynamic powers, as well as efficiency gain, can be found in Table III. The dynamic power is the average over all transitions from each of the eight input states to one of the four output combinations, whereas the static power is the average over the eight possible input

combinations. It is found that the static power of this adder is reduced by 94.7% and the total efficiency is increased by 13.9%. Note that the reference full adder is already operating at the optimum $V_{DD}$ with the highest efficiency, while more gain in efficiency could be expected if we lower the $V_{DD}$ to the most efficient operation point of the memristive full adder.

## VI. Summary

A 3-D TS device with around 10-fA leakage has been combined with CMOS transistors to build low-power memristive inverter element. A leakage current reduction by a factor of 100 was found in the experiment. Also, a hysteresis-free operation was demonstrated. Based on these findings, the power consumption of other interesting memristive circuits was derived based on calibrated simulations. Using the proposed memristive circuit approach, we find significant reductions of the total power consumption at operation speeds up to 100 kHz. Additionally, an improvement of the power efficiency by a factor of 2 is demonstrated for near-threshold computing. All of these findings make the proposed approach ideal for low-power applications and IoT sensing.

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