Improved Correlated Multiple Sampling by Using Interleaved Pixel Source Follower for High-Resolution and High-Framerate CMOS Image Sensor

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***Abstract*— This article describes an improvement in the noise reduction performance of a column correlated multiple sampling (CMS) readout circuit using interleaved pixel source follower for high-resolution and high-framerate CMOS image sensors (CISs). In this architecture, the time-interleaved operation of the two pixel source followers reduces the restrictions imposed by the settling time of the pixel source followers and extends the time for multiple sampling. The noise analysis indicates that this method has an advantage of enhanced noise reduction not only for thermal noise but also for 1/*f* noise when a high-speed readout operation is required. The measurement of the noise performance of the 8K image sensor using the CMS with the interleaved pixel source follower method exhibits a low input-referred noise of 3.2 e^- at 8K 120 frames per second, while 4.6 e^- with the conventional single-source follower readout method. The measurement results match reasonably well with the analysis presented in this article, demonstrating the effectiveness of the interleaved pixel source follower method for high-resolution and high-framerate CISs.**

***Index Terms*— 8K, CMOS image sensor (CIS), correlated multiple sampling (CMS), high resolution, noise reduction.**

I. Introduction

THE recent trends in video applications have tended toward increasing spatial resolutions, such as 4K, 8K, and high framerates. The video parameters of an ultrahigh-definition television (UHDTV) are standardized in recommendations ITU-R BT.2020 and ITU-R BT.2100 [1], [2], which specify spatial resolutions of up to 8K and frame frequencies of up to 120 frames per second (fps). One of the most challenging tasks for such high-resolution and high-framerate image sensors is to achieve high-speed readout and low-noise performance. For example, the single-row time of an 8K 120 fps progressive-scan image sensor, which corresponds to the readout time for a single row in a column-parallel readout circuit architecture, is 1.85 μs (including vertical blanking interval), which is much shorter than that of a high-definition television (HDTV) 1080i (29.6 μs) [3]. In addition, a large number of pixels require a small pixel pitch, which leads to degradation of the signal-to-noise ratio.

The correlated multiple sampling (CMS) technique has been studied as a promising noise reduction technique for achieving low-noise performance characteristics in CMOS image sensors (CISs) [4]–[6]. CMS is advantageous owing to its ability to efficiently reduce both thermal and $1/f$ noise of the pixel source follower amplifiers, which are known to be one of the major noise components in well-designed low-noise CISs [7]. In the past few years, the CMS column-parallel analog-to-digital converters (ADCs) have been implemented with the CMS technique in various ways. These include a digital implementation with multiple A/D conversions based on a single slope (SS) [8], [9] and successive approximation register (SAR) [10] ADC and an analog implementation with a passive switched capacitor (SC) [11], [12] and an SC integrator circuit [13], [14].

However, achieving both high-speed readout and low noise, which are required in high-resolution and high-framerate CISs, is difficult for the CMS readout circuit. Indeed, they have not been used in CISs that meet both the pixel count of >8 Mpixel and framerate of >60 fps. One of the reasons for this is the restriction imposed by the settling time of the pixel source follower. Since multiple sampling must be performed after the pixel source follower output has settled, a part of the readout time is devoted to the settling of the pixel source follower. In particular, for high-resolution and high-framerate CISs, the readout time is limited to a short period and the settling time of the pixel source follower tends to be long because of the parasitic capacitance due to a large number of

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vertical pixels. These factors make it difficult to secure the time required for multiple sampling.

To overcome this difficulty, we previously implemented a circuit topology with interleaved pixel source followers in a column CMS readout circuit [15]. In this architecture, the two-pixel source followers work in parallel at different phases: the output of one is multiple sampled while settling the output of the other. This time-interleaved operation reduces the restriction imposed by the settling time of the pixel source followers and extends the time for multiple sampling. We applied this method to a column-parallel readout circuit in an 8K image sensor and achieved random noise of 3.2 e^- at a readout time of 0.93 μs [8K 120 fps operation with digital correlated double sampling (CDS)] [15].

However, the precise contribution of the interleaved pixel source follower method has not been evaluated. This method enhances the reduction effect, especially for thermal noise, as thermal noise is known to be reduced by a factor equal to the square root of the sampling number [16]. In contrast, the reduction effect for $1/f$ noise could be degraded even when the sampling number is increased. This is because increasing the sampling number certainly reduces the $1/f$ noise, but simultaneously the parallel operation of pixel source followers increases the interval of the reset and signal sampling, which is known to limit the reduction effect for $1/f$ noise [5]. These conflicting effects are affected by the readout speed because increasing the sampling number and the interval of the reset and signal sampling are strongly dependent on the readout speed. Therefore, to clarify the precise contribution of the interleaved pixel source follower method, we need to discuss further both the thermal and $1/f$ noise reduction effects considering its dependence on the readout speed.

In this article, the impact of the interleaved pixel source follower method on both thermal and $1/f$ noise is theoretically analyzed. Moreover, its dependence on the operation speed is discussed. To verify the theoretical analysis, we measured and compared the theoretical calculations with the noise performance of an 8K image sensor implemented with the interleaved pixel source follower method. The contribution of the interleaved pixel source follower method for the noise performance in high-resolution and high-framerate CISs is demonstrated.

II. Theoretical Noise Analysis

In this section, the noise reduction effect of the interleaved pixel source follower method for both the thermal and $1/f$ noise is theoretically analyzed and compared with that of the conventional method regarding their dependencies on the operation speed. In the following discussion, a column CMS readout circuit is implemented with an SC integrator, column ADC, and digital CDS circuit as a typical example of the architecture.

A. Architecture

The schematic and timing diagrams of a conventional CMS readout circuit are shown in Fig. 1. The reset and signal levels of the source follower output (V_R and V_S, respectively)

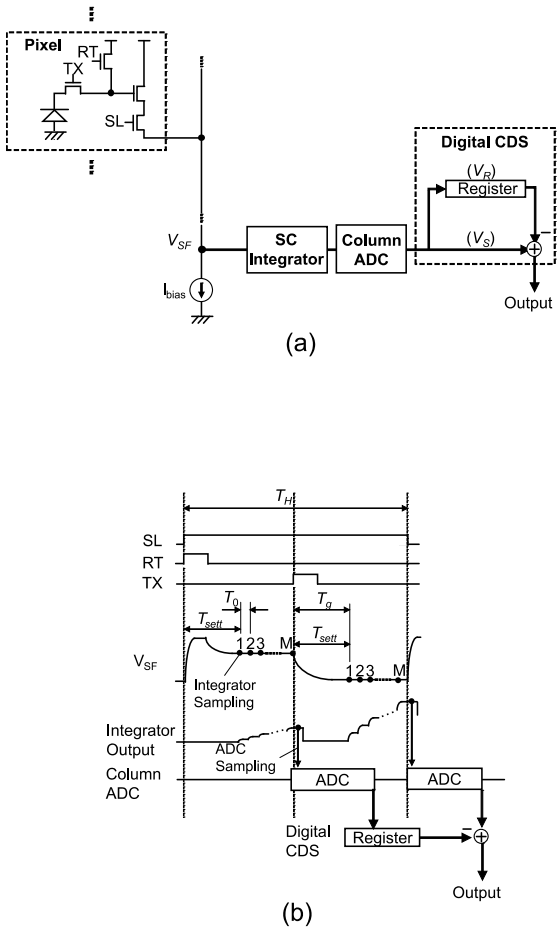

Fig. 1. (a) Schematic and (b) timing diagram of the conventional column readout circuit using CMS with single-pixel source follower.

are sampled and integrated M times by the SC integrator. The column ADC converts the output voltages of the SC integrator into the digital code. The digital CDS circuit takes the difference between the digital code of V_R and V_S. T_H, T_0, and T_{sett} are the readout time for a single row, the sampling period of the multiple sampling, and the settling time of the pixel source follower, respectively. For simplicity, T_{sett} and $T_H/2$ are assumed to be integral multiples of T_0. Subsequently, considering the time constraint, the sampling number M and the interval of the reset and signal multiple sampling T_g can be expressed as

$$M = \frac{T_H/2 - T_{sett}}{T_0} + 1 \quad (1)$$

$$T_g = T_{sett}. \quad (2)$$

As shown in (1), a part of the readout time is devoted to the settling of the pixel source follower. Therefore, shorter T_H and longer T_{sett}, which are required for higher resolution and framerate CISs, result in a smaller M. This relationship makes it difficult to implement the CMS technique for high-resolution and high-framerate CISs.

Fig. 2 shows a schematic and a timing diagram of a readout circuit using the interleaved pixel source follower method. Each pixel column has two source followers (SFA and SFB). Column vertical pixels are divided line by line into

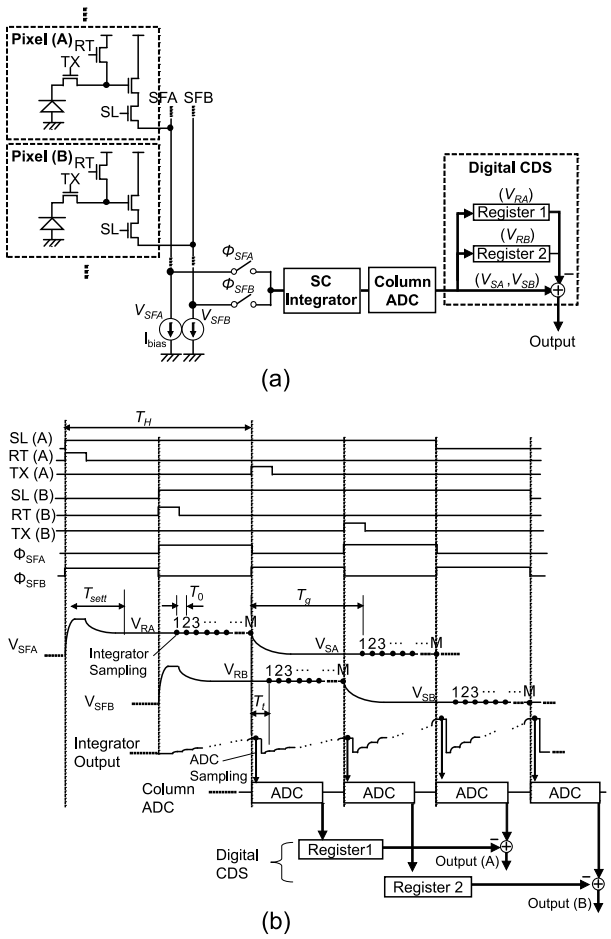

Fig. 2. (a) Schematic and (b) timing diagram of the column readout circuit using CMS with interleaved pixel source followers.

pixels A and B, and they are alternately connected to the two source followers. The two source followers work in parallel, and the phase of their operation differs by $T_{\mathrm{H}}/2$. The outputs of the source followers are connected to the SC integrator via selector switches (Φ_{SFA} and Φ_{SFB}). Subsequently, the SC integrator receives the reset levels of pixels A and B (V_{RA} and V_{RB}), followed by their signal levels (V_{SA} and V_{SB}). The digital CDS circuit takes the difference between the digital code of V_{SA} and V_{RA} and between that of V_{SB} and V_{RB} using a set of two registers. In this architecture, the input voltages of the SC integrator have already been settled before connecting to the SC integrator, which reduces the waiting time for settling. We call this topology the "interleaved pixel source follower method." T_t is the minimum time interval between the last Mth sampling point and the first sampling point of the next multiple sampling of the SC integrator. This is the time that is required to operate the following operations: integrating the Mth sampled signal, column ADC sampling, resetting the SC integrator output, and charging the input capacitor for the first sampling of the next multiple sampling. Notably, $T_t < T_{\mathrm{sett}}/2$ is required to achieve $M = 1$.

When $T_{\mathrm{H}}/2 < T_{\mathrm{sett}} - T_t$

$$M = \frac{T_{\mathrm{H}} - T_{\mathrm{sett}}}{T_0} + 1 \tag{3}$$

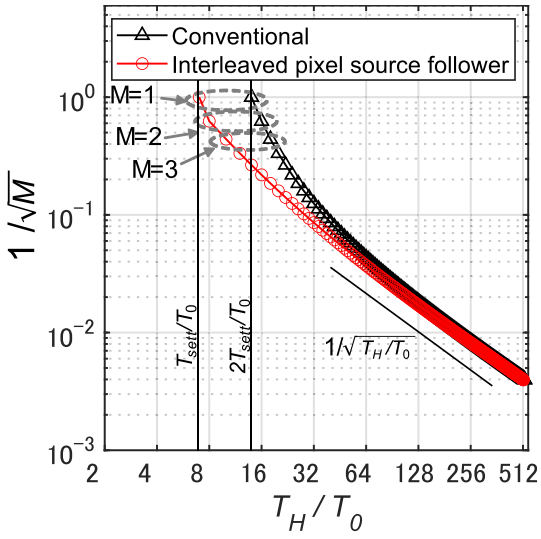

Fig. 3. Noise reduction effect for thermal noise as a function of T_{H}/T_0, comparing the conventional and the interleaved pixel source follower methods. Here, $T_t = 3T_0$ and $T_{\mathrm{sett}} = 7T_0$ are assumed as example parameters.

$$T_{\mathrm{g}} = T_{\mathrm{sett}} \tag{4}$$

and when $T_{\mathrm{H}}/2 \geq T_{\mathrm{sett}} - T_t$

$$M = \frac{T_{\mathrm{H}}/2 - T_t}{T_0} + 1 \tag{5}$$

$$T_{\mathrm{g}} = T_{\mathrm{H}}/2 + T_t. \tag{6}$$

Note that T_t is assumed to be an integral multiple of T_0 for simplicity.

B. Thermal Noise Reduction Effect

In the CMS readout circuit, the thermal noise is reduced by a factor equal to the square root of the sampling number owing to the averaging effect of multiple sampling [16]. Therefore, the enhancement of the noise reduction effect caused by the interleaved source follower can be calculated by the increase in M from the conventional method. In the conventional method, because a part of the readout time is devoted to the settling of the pixel source follower, M decreases as T_{sett} increases, as shown in (1). In the interleaved pixel source follower method, T_t has the same relationship with M as T_{sett} has in the conventional method when $T_{\mathrm{H}}/2 \geq T_{\mathrm{sett}} - T_t$, as shown in (5). In high-resolution CISs, $T_t < T_{\mathrm{sett}}$ is supposed to be because of the large parasitic capacitance as a large number of vertical pixels strongly limits the bandwidth of the pixel source follower, which results in a large T_{sett}. However, T_t can be optimized by the SC integrator design regardless of the number of vertical pixels. The amount of increase in M from the conventional method to the interleaved pixel source follower method, that is, ΔM, is obtained using (1) and (5) and is expressed as

$$\Delta M = \frac{T_{\mathrm{sett}} T_t}{T_0}. \tag{7}$$

Here, $T_{\mathrm{H}}/2 \geq T_{\mathrm{sett}} - T_t$ is assumed. Fig. 3 compares the thermal noise reduction effect of the conventional and interleaved

pixel source follower methods. The term $1/\sqrt{M}$ is plotted as a function of T_H/T_0 to discuss their dependence on the readout time. Here, T_0, T_{sett}, and T_t are treated as constants, and T_H is treated as a variable. $T_{sett} = 7T_0$ and $T_t = 3T_0$ are assumed as examples, which correspond to the actual value designed for the 8K image sensor described in Section III-A. T_{sett}, T_t, and T_0 strongly depend on the pixel rate and various design constraints, such as power consumption and circuit area. ΔM is calculated as (4) from (7). The markers in Fig. 3 correspond to an increase in the sampling number ($M = 1, 2, 3, \ldots, n$), as depicted in the figure. $M = 1$ is attained at the point $T_H/T_0 = T_{sett}/T_0$ (=7) for the interleaved pixel source follower method. At $T_H/T_0 = 2T_{sett}/T_0$ (=14), $M = 1$ is attained for the conventional method, while $M = 1 + \Delta M = 5$ is attained for the interleaved pixel source follower method. A higher noise reduction effect can be obtained for the interleaved pixel source follower method regardless of T_H/T_0, and the difference between the two methods decreases with increasing T_H/T_0. For a large T_H/T_0 ($M \gg 1$), $1/\sqrt{M}$ in both methods approaches a line proportional to $1/(TH/T0)^{1/2}$.

C. 1/f Noise Reduction Effect

T_g is constant (=T_{sett}) regardless of T_H in the conventional method, while it increases with T_H in the interleaved pixel source follower method. This can lead to the degradation of the noise reduction effect for the $1/f$ noise component in the interleaved pixel source follower method. The noise reduction effect of the CMS for $1/f$ noise can be expressed by the noise reduction factor F_{CMS} defined by [5]

$$F_{CMS}(M, M_g, x_c) = \int_0^\infty \frac{4\sin^2(Mx/2)\sin^2\left((M + M_g - 1)x/2\right)}{M^2 x\left(1 + (x/x_c)^2\right)\sin^2(x/2)} dx \quad (8)$$

with the definition of $x_c = \omega_c T_0$ and $x = \omega T_0$, where ω_c is the cutoff angular frequency determining the bandwidth of the noise components, and M_g is an integer defined by $M_g = T_g/T_0$. F_{CMS} can be approximated by a noise reduction factor of the differential averager F_{DA} expressed by [17]

$$F_{DA}(R_G) = {R_G}^2 \ln R_G + (2 + R_G)^2 \ln(2 + R_G) - 2(1 + R_G)^2 \ln(1 + R_G) \quad (9)$$

where R_G is the ratio of M_g to M ($R_G = M_g/M$). This approximation is useful for calculating F_{CMS} as a function of only R_G without numerical calculation of (8). For a large M, F_{CMS} can be exactly approximated by F_{DA}. R_G of the conventional and interleaved pixel source follower methods ($R_{G,S}$ and $R_{G,D}$, respectively) can be obtained from (1), (2), (5), and (6) as expressed by

$$R_{G,S} = \frac{T_{sett}}{T_H/2 - T_{sett} + T_0} \quad (10)$$

$$R_{G,D} = \frac{T_H/2 + T_t}{T_H/2 - T_t + T_0}. \quad (11)$$

Here, $T_H/2 \geq T_{sett} - T_t$ is assumed. At the point of T_H satisfying $R_{G,S} = R_{G,D}$, F_{CMS} of the two methods can be approximated as roughly equal using (9). For $T_H/T_0 \gg 1$ ($M \gg 1$), it is supposed that $R_{G,S} \cong 0$ and $R_{G,D} \cong 1$; thus, the saturation value of F_{CMS} of the conventional and interleaved pixel source follower methods can be approximated as $F_{DA}(0) \cong 4\ln(2) \cong 2.77$ and $F_{DA}(1) \cong 9\ln(3) - 8\ln(2) \cong 4.34$, respectively. Fig. 4 compares the values of F_{CMS} for the conventional and interleaved pixel source follower methods. F_{CMS}, derived from the numerical calculation with (8), is plotted as a function of T_H/T_0. $T_{sett} = 7T_0$, $T_t = 3T_0$ (the same as in Fig. 3), and $x_c = 16$ are assumed as an example. T_H that meets $R_{G,S} = R_{G,D}$ (denoted as T_{HX}) is plotted as the vertical line of T_{HX}/T_0(≅27). The point of intersection of the two lines approaches the line of T_{HX}/T_0. When $T_H/T_0 < T_{HX}/T_0$, a higher noise reduction effect can be obtained for the interleaved pixel source follower method. In contrast, when $T_H/T_0 > T_{HX}/T_0$, the interleaved pixel source follower method shows an inferior reduction effect for the $1/f$ noise compared with the conventional method. These are caused by the improvement effect by ΔM that becomes smaller while the degradation caused by T_g increases with increasing T_H/T_0. For $T_H/T_0 \gg 1$, F_{CMS} of the conventional and interleaved pixel source follower methods saturates to $4\ln(2) \cong 2.77$ and $9\ln(3) - 8\ln(2) \cong 4.34$, respectively, which are equal to the saturation values approximated above using (9).

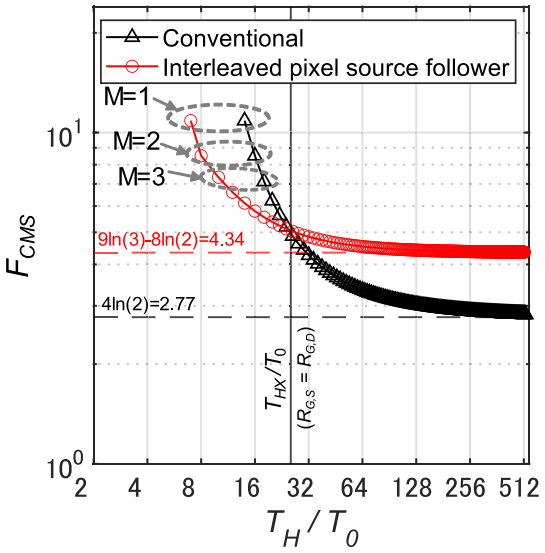

Fig. 4. Noise reduction effect for $1/f$ noise components as a function of T_H/T_0: comparison between the conventional and the interleaved pixel source follower methods. Here, $T_t = 3T_0$ and $T_{sett} = 7T_0$ are assumed as example parameters.

D. Applicability

An overall noise reduction effect can be obtained by applying the reduction factors $1/\sqrt{M}$ and F_{CMS} for thermal and $1/f$ noise components, respectively, and summing them. For low-speed CISs, where the thermal noise can be effectively suppressed by an efficient sampling number of the CMS or the bandwidth limitation effect of the low-speed readout circuit, the $1/f$ noise could become a major noise component [18]. Under this condition, the interleaved pixel source follower method does not work effectively because the enhancement, owing to ΔM, is small, and the degradation in $1/f$ noise reduction that is caused by the increase in T_g becomes large.

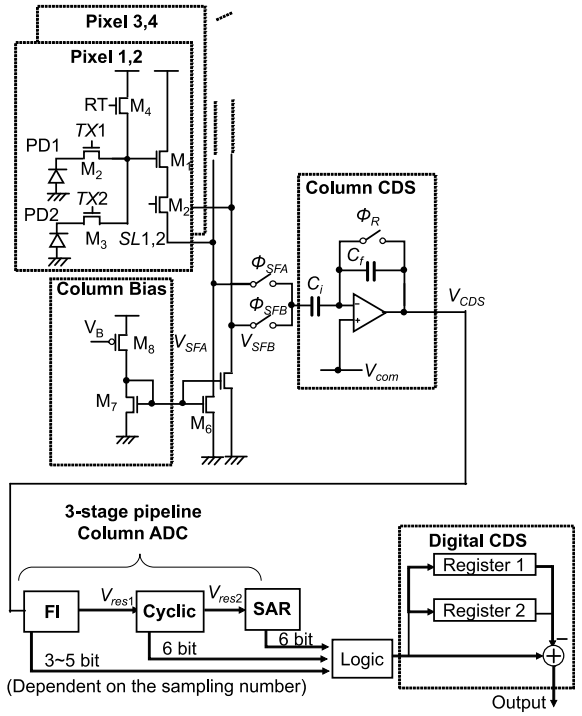

Fig. 5. Schematic of the image sensor's pixel and readout circuit.

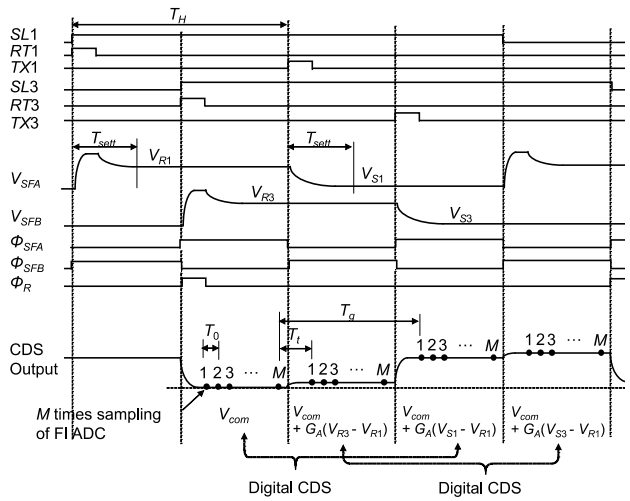

Fig. 6. Timing diagram of the image sensor's pixel and readout circuit. The same operation is conducted for pixels 2 and 4.

In contrast, for high-speed CISs, only a few sampling numbers can be obtained, and high bandwidth is required for the readout circuit, which leads to large thermal noise components. Under this condition, the interleaved pixel source follower method is effective because the thermal noise reduction effects are effectively enhanced by ΔM. Especially for high-resolution CIS, as shown in (7), ΔM tends to be large because of the large difference between T_{sett} and T_t, which results in a large enhancement of the noise reduction effect. In addition, from the discussion on the $1/f$ noise reduction effect, if T_{H} is shorter than T_{HX}, the interleaved pixel source follower method enhances the noise reduction effect even for $1/f$ noise components. Therefore, ΔM and T_{HX} provide clear indications of the applicability. We conclude that the interleaved pixel source follower method effectively reduces noise at high-resolution and high-framerate CISs.

III. Comparison With Experimental Measurements

A. Implementation of 8K Image Sensor

The schematic and timing diagrams of an 8K image sensor readout circuit with an implemented interleaved pixel source follower method are shown in Figs. 5 and 6, respectively. The image sensor has a pixel array with 2.1-μm pixel pitch (effective area: 4.320 pixels $\times$ 7.680 pixels). The vertically aligned two-shared pixels are connected alternately to the two source followers. The outputs of the source followers are connected to an analog column CDS circuit via two switches, which is for level adjustment and amplification of the pixel source follower output. Subsequently, the CDS circuit receives the reset levels of pixels 1 and 3 (V_{R1} and V_{R3}), followed by their signal levels (V_{S1} and V_{S3}). Once V_{R1} is received, capacitor C_f is reset by Φ_{R}, and the output voltage of the CDS (V_{CDS}) is set to a common voltage V_{com}. Thus, the output order of V_{CDS} is V_{com}, $V_{\text{com}} + G_{\text{A}}(V_{\text{R3}}-V_{\text{R1}})$, $V_{\text{com}} + G_{\text{A}}(V_{\text{S1}}-V_{\text{R1}})$, and $V_{\text{com}} + G_{\text{A}}(V_{\text{S3}}-V_{\text{R1}})$, where G_{A} is the gain of the column CDS ($G_{\text{A}} = C_i/C_f = 2$). These voltages are sampled and integrated M times and converted into digital code by the three-stage pipelined ADC, consisting of folding integration (FI) and cyclic, SAR ADC. The FI ADC has an SC integrator that executes multiple sampling. The digital CDS circuit takes the difference between the first and third outputs and between the second and fourth outputs using two sets of registers. Then, the final CMS output codes of $G_{\text{A}}(V_{\text{S1}}-V_{\text{R1}})$ and $G_{\text{A}}(V_{\text{S3}}-V_{\text{R3}})$ are obtained. In this implementation, a margin, corresponding to the maximum difference between V_{R1} and V_{R3}, is needed for the lower limit of the column ADC input voltage range. This is required because if $V_{\text{R3}}-V_{\text{R1}}$ is negative, then $V_{\text{com}} + G_{\text{A}}(V_{\text{R3}}-V_{\text{R1}})$ is lower than the reference level of the CDS output (V_{com}). Output voltage clipping circuits are used in the pixel source followers to avoid abnormal voltage fluctuations in V_{R1} and V_{R3}. The difference between the two pixel source followers' gains or linearity error of the column ADC can cause horizontal striped artifacts, which can be reduced by applying signal corrections in the digital domain.

Fig. 7 shows (a) circuit diagram and (b) timing diagram of the FI ADC. The FI ADC consists of an SC integrator, comparator, counter, and negative feedback path with a 1-bit digital to analog converter (DAC). This ADC works as a first-order incremental delta–sigma modulator. The counter output is treated as higher bits, and the residue voltage of the SC integrator is converted into lower bits by the following ADC. This type of A/D conversion is also known as an extended counting ADC [19], [20]. Duplicated sampling capacitors ($C_{1\text{A}}$ and $C_{1\text{B}}$) are implemented to obtain high-speed operation. In the first sampling phase, $C_{1\text{A}}$ and C_2 are charged by the input voltage, and the voltage across C_2 and V_{RC} is compared by the comparator. The sampled charge of $C_{1\text{A}}$ is transferred to C_2 so that the integration gain is

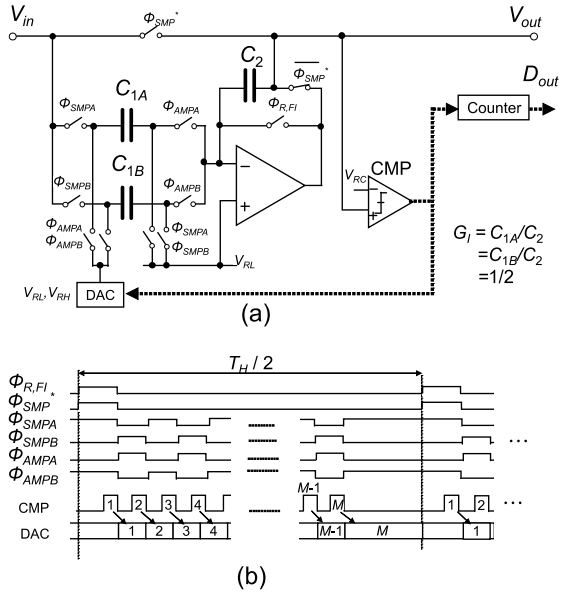

Fig. 7. (a) Circuit diagram and (b) timing diagram of the FI ADC.

$G_I + 1$, where $G_I = C_{1A}/C_2 = C_{1B}/C_2 = 1/2$. In the second sampling phase, the charge sampled in C_{1A} is transferred to C_2, and a reference voltage (V_{RL} or V_{RH}) for the 1-bit DAC is subtracted. Moreover, C_{1B} simultaneously samples the input voltage. In the following phases, the ADC works similarly as in the second sampling phase. However, the roles of C_{1A} and C_{1B} are switched. The input voltage is amplified by the gain of $G_I M + 1$, and the output voltage is maintained to a limited range from V_{RL} to V_{RH}.

B. Noise Component Analysis in the Readout Circuit

The noise components of the 8K image sensor are clarified in this section. For this, the noise characteristics of the signal readout circuit from the pixel-to-column ADC were analyzed based on the model presented in [5] with some modifications. The noise power referred to at the CMS output can be expressed as the sum of the noise components described as follows: $P_{n,rst}$ is the reset noise component of the integrator; $P_{nT,smpl}$ and $P_{nF,smpl}$ are the thermal and $1/f$ noise components in the sampling phase, respectively; $P_{nT,trns}$ and $P_{nF,trns}$ are the thermal and $1/f$ noise components in the signal charge transfer phase, respectively; and $P_{nT,ADC}$ is the thermal noise component of the column ADC sampling. $P_{n,rst}$, $P_{nT,trns}$, $P_{nF,trns}$, and $P_{nT,ADC}$ can be calculated using the same model presented in [5]. In this analysis, $P_{nF,trns}$ and $1/f$ noise due to the amplifier of the FI ADC are ignored because the amplifier uses relatively large transistors with low $1/f$ noise. $P_{nT,smpl}$ and $P_{nF,smpl}$ must be modified to include the effect of the first sampling and the noise component of the column CDS and column bias circuit. $P_{nT,smpl}$ is modified as

$$P^*_{nT,smpl} = P_{nT,SF} + P_{nT,Bias} + P_{nT,CDS} \tag{12}$$

where $P_{nT,SF}$, $P_{nT,Bias}$, and $P_{nT,CDS}$ are the noise components generated by the source follower, column bias circuit, and column CDS, respectively. The noise bandwidth limitation of the source follower and column bias circuit are assumed independent of the FI ADC sampling capacitor because the cutoff frequencies of the source follower ω_{cSF} and the column bias circuit ω_{cB} are lower than that of the CDS circuit. Thus, $P_{nT,SF}$, and $P_{nT,Bias}$ can be calculated by

$$P_{nT,SF} = \int_0^\infty G_A^2 G_{nSF}^2 \frac{4k_B T \xi_{SF}}{g_{mSF}} \frac{1}{1+(\omega/\omega_{cSF})^2} \left|H^*_{CMS}(\omega)\right|^2 df \tag{13}$$

$$P_{nT,Bias} = \int_0^\infty G_A^2 G_{nSF}^2 \frac{4k_B T \xi_B}{g_{mSF}^2} \frac{g_{mCS}^2}{g_{mBias}} \frac{1}{1+\left(\omega/\omega_{cB}\right)^2} \times \left|H^*_{CMS}(\omega)\right|^2 df \tag{14}$$

where G_{nSF} is the noise gain factor of the source follower [5], ξ_{SF} and ξ_B are the excess thermal noise factor of the source follower and the column bias circuit, respectively; g_{mSF}, g_{mCS}, and g_{mBias} are the transconductance values of transistors M1, M6, and M7, respectively, as shown in Fig. 5, and $H^*_{CMS}(\omega)$ is the CMS transfer function. From the sampling timing and integration gain of the FI ADC, H^*_{CMS} is obtained with the z transform and is expressed in the z domain as

$$H^*_{CMS}(z) = G_I\left(1 - z^{(M+M_g-1)}\right)\left\{\frac{1-z^{-M}}{1-z^{-1}} + \frac{1}{G_I} z^{-(M-1)}\right\} \tag{15}$$

where M_g is an integer defined by $M_g = T_g/T_0$. T_g and T_0 are the intervals of the reset and signal multiple sampling and the sampling period, respectively. With $z = \exp(j\omega T_0)$, the noise power transfer function for the CMS $H^*_{CMS}(\omega)$ is given by

$$\begin{aligned}\left|H^*_{CMS}(\omega)\right|^2 &= 4\, G_I^2 \sin^2\left\{\omega\left(M + M_g - 1\right)T_0/2\right\} \\ &\cdot \left\{\frac{\sin^2(\omega M T_0/2)}{\sin^2(\omega T_0/2)} + \frac{2}{G_I} \right. \\ &\left. \times \frac{\sin(\omega M T_0/2)\cos\{\omega(M-1)T_0/2\}}{\sin(\omega T_0/2)} + \frac{1}{G_I^2}\right\}.\end{aligned} \tag{16}$$

Similar calculations cannot be applied to $P_{nT,CDS}$ because the CDS cutoff frequency is affected by the sampling capacitance of the FI ADC. However, each sampled noise of the first sampling ($P_{n,CDS1}$) and second to Mth samplings ($P_{n,CDS2}$) can be calculated separately, and $P_{nT,CDS}$ can be obtained by summing them

$$P_{nT,CDS} = 2P_{n,CDS1} + 2(M-1)P_{n,CDS2} \tag{17}$$

where

$$P_{n,CDS1} = \frac{(G_I+1)^2 \xi_{CA} k_B T}{\beta_A (C_L + C_2)} \tag{18}$$

and

$$P_{n,CDS2} = \frac{G_I{}^2 \xi_{CA} k_B T}{\beta_A C_L} \tag{19}$$

where ξ_{CA}, β_A, and C_L are the excess thermal noise factor, feedback factor, and load capacitance of the amplifier, respectively, which are used for the CDS circuit in the Mth sampling phase. $P_{nF,smpl}$ is modified as follows:

$$P^*_{nF,smpl} = \int_0^\infty G_A^2 G_{nSF}^2 \frac{K_{fSF}\varsigma_{SF}}{f} \frac{1}{1+(\omega/\omega_{cSF})^2} \left|H^*_{CMS}(\omega)\right|^2 df \tag{20}$$

TABLE I
SAMPLING TIMINGS USED FOR MEASUREMENTS

Readout method	Interleaved pixel source follower			Conventional		
T_H [μs] (frame rate [fps])	1.85 (120)	3.70 (60)	7.41 (30)	1.85 (120)	3.70 (60)	7.41 (30)
T_0 [μs]	0.11					
T_{sett} [μs]	0.81					
T_t [μs]	0.27					
M	6	14	30	2	10	26
T_g [μs]	1.29	2.19	3.96	0.81	0.81	0.81

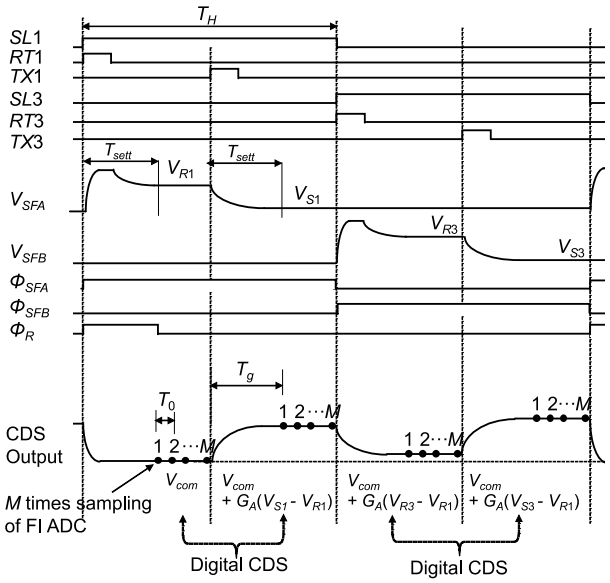

Fig. 8. Timing diagram of the readout circuit used for emulating the conventional readout timing. The same operation is conducted for pixels 2 and 4.

where K_{fSF} is the flicker noise coefficient, and ς_{SF} is the flicker noise factor of the source follower. The total noise power referred to at the output of the readout circuit $P_{\mathrm{nC,total}}$ is given by

$$P_{\mathrm{n,total}} = P_{\mathrm{n,rst}} + P^*_{\mathrm{nT,smpl}} + P^*_{\mathrm{nF,smpl}} + P_{\mathrm{nT,trns}} + P_{\mathrm{nT,ADC}}. \tag{21}$$

The gain from the charge generated in the photodiode to the output is given by $G_{\mathrm{cSF}}G_{\mathrm{A}}(G_{\mathrm{I}}M+1)$, where G_{cSF} is the conversion gain of the pixel source follower. The input referred noise is given by

$$N_{\mathrm{n,total}} = \frac{\sqrt{P}_{\mathrm{n,total}}}{G_{\mathrm{cSF}}G_{\mathrm{A}}(G_{\mathrm{I}}M+1)}. \tag{22}$$

C. Experimental Setup

The sampling timings used for the measurement are shown in Table I. The readout time for a single row T_{H} of 1.85, 3.70, and 7.41 μs, corresponding to framerates of 120, 60, and 30, respectively, is used for the measurement. The conventional readout operation was emulated using the same readout circuit to compare with the conventional method. Fig. 8 shows the readout timing used for emulating the conventional readout operation. The two pixel source followers were operated one by one. The select switches (Φ_{SFA} and Φ_{SFB}) select the SFA, and the reset and signal levels of pixel 1 were readout in the period of T_{H}. Subsequently, the select switches select SFB, and the reset and signal levels of pixel 3 were readout in the next period of T_{H}. The column CDS circuit receives the reset and signal level of the pixels subsequently, and the digital CDS circuit takes the difference between the two consecutive codes. Note that the same readout operation can be performed by a single-pixel source follower and a single register in the digital-CDS circuit used for the conventional readout circuit. T_0, T_t, and T_{sett} were 0.11, 0.81, and 0.27 μs, respectively. These parameters were determined by the bandwidth of the pixel source follower and SC integrator in the FI ADC. M obtained in the interleaved pixel source follower method is ΔM (=4) larger than that of the conventional method for the same T_{H}. T_{g} is equal to T_{sett} (=0.81 μs) regardless of T_{H} in the conventional readout method; however, it increases in proportion to T_{H} in the interleaved pixel source follower method. To measure dark noise for the 8K image sensor, the extracted 100 × 100 pixels were used to analyze the random noise; the root-mean-square noise values were calculated for each pixel, and the median value of the pixels was treated as random noise.

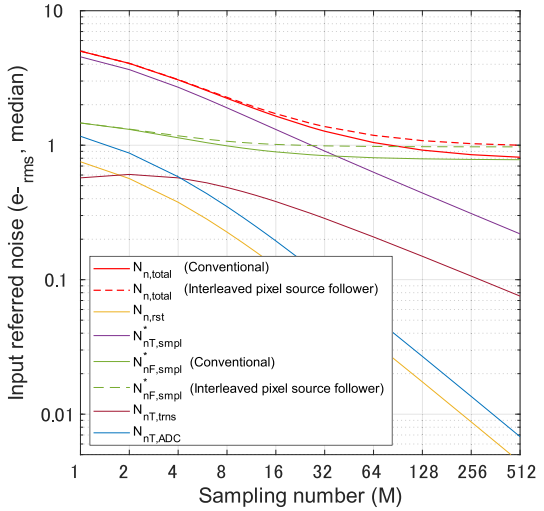

Fig. 9. Calculated noise components as functions of M.

D. Results and Discussion

Fig. 9 shows the calculated noise components as a function of M, where $N_{\mathrm{n,rst}}$, $N^*_{\mathrm{nT,smpl}}$, $N^*_{\mathrm{nF,smpl}}$, $N_{\mathrm{nT,trns}}$, and $N_{\mathrm{nT,ADC}}$ are the input-referred noise components of $P_{\mathrm{n,rst}}$, $P^*_{\mathrm{nT,smpl}}$, $P^*_{\mathrm{nF,smpl}}$, $P_{\mathrm{nT,trns}}$, and $P_{\mathrm{nT,ADC}}$, respectively. Moreover, the sum of them is plotted as $N_{\mathrm{n,total}}$. Because $N_{\mathrm{n,rst}}$, $N^*_{\mathrm{nT,smpl}}$, $N_{\mathrm{nT,trns}}$, and $N_{\mathrm{nT,ADC}}$ showed the same behavior for both the conventional and interleaved pixel source follower methods, they are plotted using similar lines for both the methods. This is because these components are dependent on M but are independent of T_{g} [5]. In contrast, $N^*_{\mathrm{nF,smpl}}$ that originates from the $1/f$ noise of the source follower amplifier shows a different tendency when

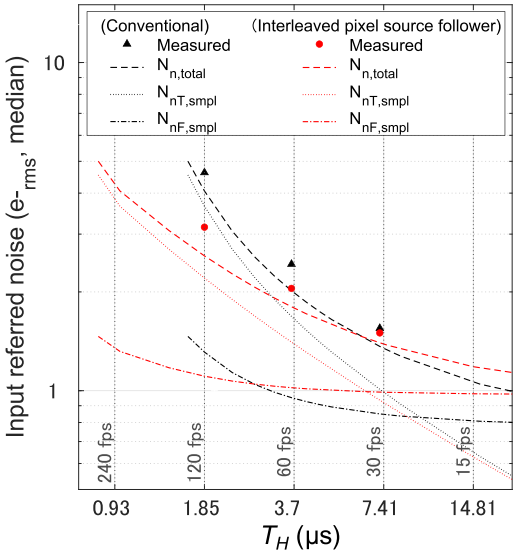

Fig. 10. Comparison of the measured input-referred noise with the calculated noise $N_{\mathrm{n,total}}$ as functions of T_{H}. $N^{*}_{\mathrm{nT,smpl}}$ and $N^{*}_{\mathrm{nF,smpl}}$ are plotted as the main noise components of $N_{\mathrm{n,total}}$.

comparing the two methods. This is because the $1/f$ noise reduction effect is affected by T_{g}, as discussed in Section II. When the sampling number is small, $N^{*}_{\mathrm{nT,smpl}}$ is a dominant component; however, it is suppressed with an increase in M. For large M, $N^{*}_{\mathrm{nF,smpl}}$ becomes dominant, which is because the noise reduction effect for $1/f$ noise is saturated for a large M. The saturation value of the interleaved pixel source follower method is higher than that of the conventional method, which corresponds to the degradation of the $1/f$ noise reduction effect caused by the interleaved pixel source follower method, as presented in Section II. The noise components $N_{\mathrm{n,rst}}$, $N_{\mathrm{nT,trns}}$, $N_{\mathrm{nT,ADC}}$, and $N_{\mathrm{nT,smpl}}$ are smaller than $N^{*}_{\mathrm{nT,smpl}}$ and effectively suppressed with an increase in M. From these results, $N^{*}_{\mathrm{nT,smpl}}$ and $N^{*}_{\mathrm{nF,smpl}}$ can be regarded as the main noise components that can explain the behavior of the overall noise performance of the image sensor.

Fig. 10 compares the measured input-referred noise of the conventional and interleaved pixel source follower methods as a function of T_{H}. The calculated noise of $N_{\mathrm{n,total}}$ is plotted to compare with the calculation results. $N^{*}_{\mathrm{nT,smpl}}$ and $N^{*}_{\mathrm{nF,smpl}}$ are plotted as the main noise components of $N_{\mathrm{n,total}}$. At $T_{\mathrm{H}} = 1.85$ μs, corresponding to 8K 120 fps operation, a low input-referred noise of 3.2 e^{-} with $M = 6$ is obtained for the interleaved pixel source follower method, while that for the conventional method is 4.6 e^{-} with $M = 2$. The difference in the input referred-noise between the two methods decreases with an increase in T_{H}. At $T_{\mathrm{H}} = 7.41$ μs, corresponding to 8K 30 fps operation, 1.5 e^{-} with $M = 30$ and 1.6 e^{-} with $M = 26$ are obtained for the interleaved pixel source follower method and the conventional method, respectively. These results can be explained by the analysis presented in Section II as follows. For high-speed readout operation (at $T_{\mathrm{H}} = 1.85$ μs), because T_{H} is shorter than T_{HX}, ΔM (=4) strongly enhances the noise reduction performance for both the thermal and $1/f$ noise, which results in the low input-referred noise of the interleaved pixel source follower method. For a relatively low-speed readout operation (at $T_{\mathrm{H}} = 7.41$ μs), the improvement effect by ΔM becomes small, and the degradation of $1/f$ noise reduction effect caused by T_{g} becomes larger. Therefore, the difference in the input-referred noise between the two methods becomes small. $N^{*}_{\mathrm{nT,smpl}}$, $N^{*}_{\mathrm{nF,smpl}}$, and thermal and $1/f$ noise components in the sampling phase, respectively, show the behavior mentioned above, and $N_{\mathrm{n,total}}$, whose main component can be regarded as $N^{*}_{\mathrm{nT,smpl}}$ and $N^{*}_{\mathrm{nF,smpl}}$, agrees reasonably well with the measured results. Thus, these results clearly demonstrate the contribution of the interleaved pixel source follower method for the improvement of noise performance in the high-resolution and high-framerate CIS.

IV. Conclusion

This article describes the noise reduction effect of a column CMS readout circuit with interleaved two pixel source followers and discusses its effectiveness for high-resolution and high-framerate CISs. The noise reduction effect analysis indicated that the increase in the sampling number, owing to the interleaved pixel source followers, tends to be large in the high-resolution CISs, resulting in a large enhancement in noise reduction. Furthermore, the interleaved pixel source follower method has the advantage of enhanced noise reduction performance not only for thermal noise but also for $1/f$ noise when a high-speed readout operation is required. The measurement of the noise performance for the 8K image sensor implemented with the interleaved pixel source follower method showed the low input-referred noise of 3.2 e^{-} at 8K 120 fps operation while 4.6 e^{-} for the conventional readout method. Furthermore, their dependence on the readout speed and the difference between the two methods agreed reasonably well with the analysis presented in this article. These results demonstrated the effectiveness of the interleaved pixel source follower method and clarified its effect on the noise performance at high-resolution and high-framerate CIS.

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References

[1] *Parameter Values for Ultra-High Definition Television Systems for Production and International Programme Exchange*, document Rec. ITU-R BT.2020-1, 2015. [Online]. Available: https://www.itu.int/dms_pubrec/itu-r/rec/bt/R-REC-BT.2020-2-201510-I!!PDF-E.pdf

[2] *Image Parameter Values for High Dynamic Range Television for Use in Production and International Programme Exchange*, document Rec. ITU-R BT.2100-2, 2016. [Online]. Available: https://www.itu.int/dms_pubrec/itu-r/rec/bt/R-REC-BT.2100-2-201807-I!!PDF-E.pdf

[3] I. Takayanagi and J. Nakamura, "High-resolution CMOS video image sensors," *Proc. IEEE*, vol. 101, no. 1, pp. 61–73, Jan. 2013, Accessed on: Jan, 25, 2020, doi: 10.1109/JPROC.2011.2178569.

[4] S. Kawahito, S. Suh, T. Shirei, S. Itoh, and S. Aoyama, "Noise reduction effects of column-parallel correlated multiple sampling and source-follower driving current switching for CMOS image sensors," in *Proc. Int. Image Sensor Workshop*, 2009, pp. 320–323. [Online]. Available: http://www.imagesensors.org/Past%20Workshops/2009%20Workshop/2009%20Papers/075_paper_kawahito_shizuoka_colpar.pdf

[5] S. Kawahito and M.-W. Seo, "Noise reduction effect of Multiple-Sampling-Based signal-readout circuits for ultra-low noise CMOS image sensors," *Sensors*, vol. 16, no. 11, p. 1867, Nov. 2016, doi: 10.3390/s16111867.

[6] A. Boukhayma, A. Peizerat, and C. Enz, "Temporal readout noise analysis and reduction techniques for low-light CMOS image sensors," *IEEE Trans. Electron Devices*, vol. 63, no. 1, pp. 72–78, Jan. 2016, doi: 10.1109/TED.2015.2434799.

[7] C. Enz and A. Boukhayma, "Recent trends in low-frequency noise reduction techniques for integrated circuits," in *Proc. Int. Conf. Noise Fluctuations (ICNF)*, Xian, China, Jun. 2015, pp. 1–6, doi: 10.1109/ICNF.2015.7288622.

[8] M. Sato *et al.*, "A 0.50e$^-$rms noise 1.45μm-pitch CMOS image sensor with reference-shared in-pixel differential amplifier at 8.3Mpixel 35fps," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2020, pp. 108–110, doi: 10.1109/ISSCC19947.2020.9063017.

[9] S.-F. Yeh, K.-Y. Chou, H.-Y. Tu, C. Y.-P. Chao, and F.-L. Hsueh, "A 0.66e_{rms}^- temporal-readout-noise 3-D-stacked CMOS image sensor with conditional correlated multiple sampling technique," *IEEE J. Solid-State Circuits*, vol. 53, no. 2, pp. 527–537, Feb. 2018, doi: 10.1109/JSSC.2017.2765927.

[10] M.-K. Kim, S.-K. Hong, and O.-K. Kwon, "A fast multiple sampling method for low-noise CMOS image sensors with column-parallel 12-bit SAR ADCs," *Sensors*, vol. 16, no. 1, p. 27, Dec. 2015, doi: 10.3390/s16010027.

[11] A. Boukhayma and A. Peizerat, "A correlated multiple sampling passive switched capacitor circuit for low light CMOS image sensors," in *Proc. Int. Conf. Noise Fluctuations (ICNF)*, Xian, China, Jun. 2015, pp. 1–4, doi: 10.1109/ICNF.2015.7288563.

[12] R. Capoccia, A. Boukhayma, and C. Enz, "Experimental verification of the impact of analog CMS on CIS readout noise," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 3, pp. 774–784, Mar. 2020, doi: 10.1109/TCSI.2019.2951663.

[13] S. Suh, S. Itoh, S. Aoyama, and S. Kawahito, "Column-parallel correlated multiple sampling circuits for CMOS image sensors and their noise reduction effects," *Sensors*, vol. 10, no. 10, pp. 9139–9154, Oct. 2010, doi: 10.3390/s101009139.

[14] T. Wang, M.-W. Seo, K. Yasutomi, and S. Kawahito, "A 19-bit column-parallel folding-integration/cyclic cascaded ADC with a pre-charging technique for CMOS image sensors," *IEICE Electron. Exp.*, vol. 14, no. 2, Jan. 2017, Art. no. 20161199, doi: 10.1587/elex.14.20161199.

[15] T. Yasue *et al.*, "A 33Mpixel CMOS imager with multi-functional 3-stage pipeline ADC for 480fps high-speed mode and 120fps low-noise mode," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2018, pp. 90–92, doi: 10.1109/ISSCC.2018.8310198.

[16] R. Capoccia, A. Boukhayma, and C. Enz, "A kTC noise analysis in a passive switched-capacitor CMS circuit for CIS," in *Proc. 25th Int. Conf. Noise Fluctuations (ICNF)*, 2019, pp. 1–4, doi: 10.5075/EPFL-ICLAB-ICNF-269305.

[17] G. R. Hopkinson and D. H. Lumb, "Noise reduction techniques for CCD image sensors," *J. Phys. E. Sci. Instrum.*, vol. 15, no. 11, p. 1214, 1982, doi: 10.1088/0022-3735/15/11/020.

[18] M.-W. Seo, S. Kawahito, K. Kagawa, and K. Yasutomi, "A 0.27e-rms read noise 220-μV/e-conversion gain reset-gate-less CMOS image sensor with 0.11-μm CIS process," *IEEE Electron Device Lett.*, vol. 36, no. 12, pp. 1344–1347, Dec. 2015, doi: 10.1109/LED.2015.2496359.

[19] P. Rombouts, W. De Wilde, and L. Weyten, "A 13.5-b 1.2-V micropower extended counting A/D converter," *IEEE J. Solid-State Circuits*, vol. 36, no. 2, pp. 176–183, Feb. 2001, doi: 10.1109/4.902758.

[20] J.-H. Kim *et al.*, "A 14b extended counting ADC implemented in a 24Mpixel APS-C CMOS image sensor," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, USA, vol. 45, Feb. 2012, pp. 390–392, doi: 10.1109/ISSCC.2012.6177060.