The Impact of Holding Voltage of Transient Voltage Suppressor (TVS) on Signal Integrity of Microelectronics System With CMOS ICs Under System-Level ESD and EFT/Burst Tests

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***Abstract*— Transient voltage suppressor (TVS) has been widely used on the printed circuit board (PCB) to protect the microelectronics system against the system-level electrostatic discharge (ESD) and electrical fast transient/burst (EFT/B) events. However, the signal integrity of the system operations may be destroyed after the system-level ESD and EFT/B immunity test, if the TVS were designed with a holding voltage of lower than the operating voltage of the CMOS ICs equipped in the system. In this work, the signal integrity of microelectronics system protected by the TVS with different holding voltages was studied under the system-level ESD and EFT/B immunity test. By monitoring the transient voltage waveforms in the time domain during system-level ESD and EFT/B immunity test, the system malfunction has been found when the TVS is with a lower holding voltage. Therefore, the holding voltage of the TVS must be greater than the system operating voltage to maintain the signal integrity in the field applications.**

***Index Terms*— Electrical fast transient (EFT)/burst test, holding voltage, signal integrity, system-level electrostatic discharge (ESD), transient voltage suppressor (TVS).**

I. Introduction

IN ORDER to protect against the damages from electrostatic discharge (ESD), on-chip ESD protection circuits or devices must be integrated into the CMOS ICs to meet the component-level ESD specification [1]. Besides, the microelectronics system equipped with the CMOS ICs needs to meet the system-level ESD and electrical fast transient/burst (EFT/B) specification [2], [3]. The microelectronics system must sustain the ESD level of 8 kV under contact-discharge mode to achieve the immunity requirement of “level 4” in the system-level ESD standard [2]. The signal, data, and control ports of microelectronics system also must sustain the 2-kV EFT test to achieve the immunity requirement of “level 4” in the EFT/B standard [3]. The transient current and the zapping voltage of the system-level ESD and EFT/B immunity test are much larger than those in the component-level ESD test. The on-chip ESD protection circuits with limited device dimensions in silicon chip were hard to sustain the overstress of the system-level ESD and EFT immunity test. Therefore, the discrete transient voltage suppressors (TVSs) were added on the printed circuit board (PCB) of the microelectronics system to protect the CMOS ICs against the overstress of the system-level ESD and EFT test. Such TVSs were often placed near to the I/O ports of CMOS ICs and also near to the power pins, on the PCB layout.

The TVS with a lower holding voltage (after it was turned on) can sustain much higher ESD and EFT/B energy, due to the lower heat generated on itself when the transient current is discharging through it. Some commercial TVS products were therefore designed with lower holding voltages to provide high ESD and EFT/B specification. But the on-chip ESD protection devices with their holding voltages lower than the operating voltage of circuits had been reported to suffer the latchup-like failure [4]–[6].

The signal integrity issue of integrated circuits (ICs) was traditionally estimated by measuring the insertion loss, cross talk, or even eye diagram of the I/O signals. The signal integrity in a microelectronics product may be affected by many aspects such as the trace layout on the PCB, the location of the ICs on the PCB, and the function of IC used in the system [7]. The I/O ports of microelectronics systems protected by TVS should be improved with high immunity against the system-level ESD/EFT events. But if the holding voltage of the TVS is lower than the voltage level of the I/O signals, the unexpected turned-on TVS (due to the over-shooting and/or under-shooting transient voltages during

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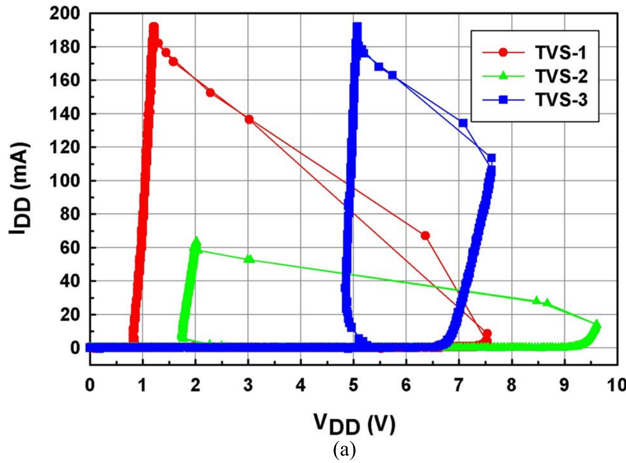
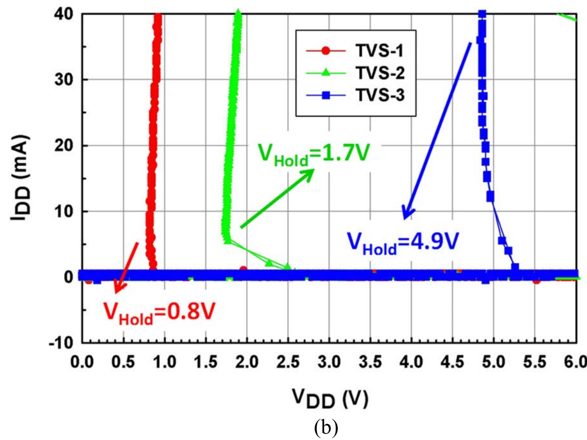


(a)



(b)

Fig. 1. (a) Measured dc *I*–*V* characteristics and (b) zoomed-in plots to show the holding voltage of three commercial TVSs (TVS-1, TVS-2, and TVS-3), which performed with different holding voltages.

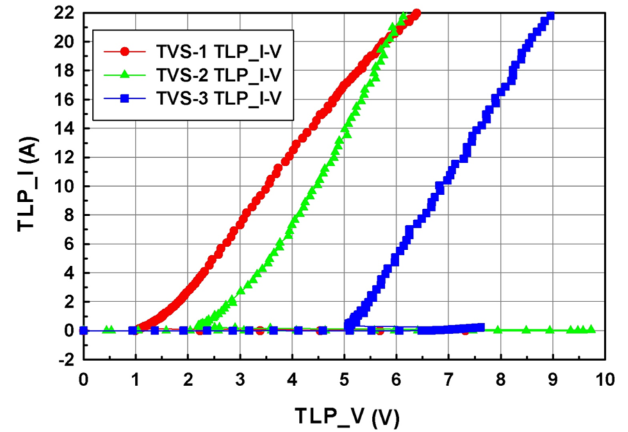


Fig. 2. 100-ns TLP-measured *I*–*V* curves of three TVSs.

the ESD/EFT tests) may cause the I/O signal failure after the ESD/EFT tests. Such a failure was not included into the traditional signal integrity issue. Recently, the signal integrity of microelectronics system protected by TVSs with different holding voltages under the system-level ESD test has been investigated [8]. In addition, further study has been investigated in this work, whether the on-board TVS with its holding voltage lower than the system operating voltage did cause any negative impact to the microelectronics system under ESD/EFT test.

II. TVS Characteristics

In order to investigate the impact to the microelectronics system, three commercial TVS products with different holding voltages are selected to be tested in this experiment. All these TVS products have been declared that it can be used as 3.3-V I/O port protection device.

A. DC I–V Characteristics of TVS

The dc I–V characteristics of three commercial TVSs are measured by the curve tracer (Tek370B), and the results are shown in Fig. 1(a) and (b). From Fig. 1(a), the trigger voltage (V_{Trig}) of TVS-1, TVS-2, and TVS-3 are 7.6, 9.7, and 7.6 V, respectively. And the trigger current (I_{Trig}) of TVS-1, TVS-2, and TVS-3 are 10, 14, and 110 mA, respectively. With a lower trigger voltage, the TVS can be triggered on earlier to protect the CMOS ICs in the microelectronics system when the overstress voltage is zapping on it.

The holding voltage (V_{Hold}) and the holding current (I_{Hold}) of TVS-1, TVS-2, and TVS-3 are shown in Fig. 1(b). From Fig. 1(b), the TVS-1 has the lowest holding voltage of 0.8 V, and the holding voltage of TVS-2 is 1.7 V. Only the TVS-3 has the holding voltage bigger than the operating voltage of 3.3 V, and the holding voltage of TVS-3 is 4.9 V. With a lower holding voltage, the overstress voltage to microelectronics system can be clamped down lower by the TVS. From Fig. 1(b), the holding currents (at the point of minimum voltage in the holding region) of TVS-1, TVS-2, and TVS-3 are 3, 7, and 35 mA, respectively.

B. 100-ns TLP I–V Characteristics

To investigate the ESD robustness of each TVS, the 100-ns transmission line pulsing system (TLP) is used to measure the corresponding I–V curve [9], [10]. Fig. 2 shows the 100-ns TLP-measured I–V curves of these three TVSs. The second breakdown current (It2) of these three TVSs are all greater than 22 A (limited by the equipment), which can sustain the ESD level greater than 8 kV under direct contact-discharge test mode by the ESD gun. From the TLP-measured I–V curves, the lower holding voltage always brings the lower clamping voltage. The TVS with lower clamping voltage can provide the CMOS ICs with more efficient protection. Hence, some commercial TVS products were designed with lower holding voltage to provide better system-level ESD protection for CMOS ICs. But the TVS with a holding voltage lower than the system operation voltage will cause signal integrity issue to the microelectronics system.

III. System-Level ESD Immunity Test

A. Test Setup for System-Level ESD Immunity Test

Fig. 3 shows the test setup with two CMOS ICs (IC-1 and IC-2) protected by a TVS on one signal trace on the PCB. In order to emulate the output port in the microelectronic system, a CMOS inverter (IC-1) is used as a transmission

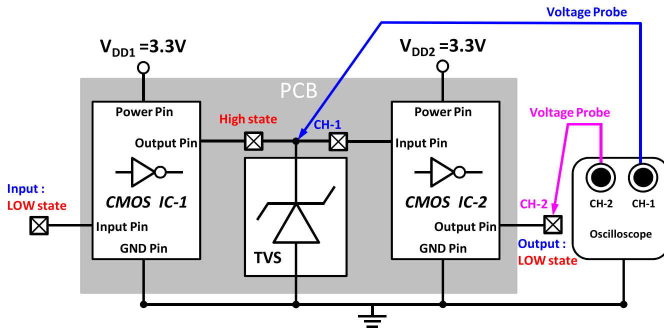


Fig. 3. Test setup with two CMOS ICs (IC-1 and IC-2) protected by a TVS on one signal trace on the PCB.

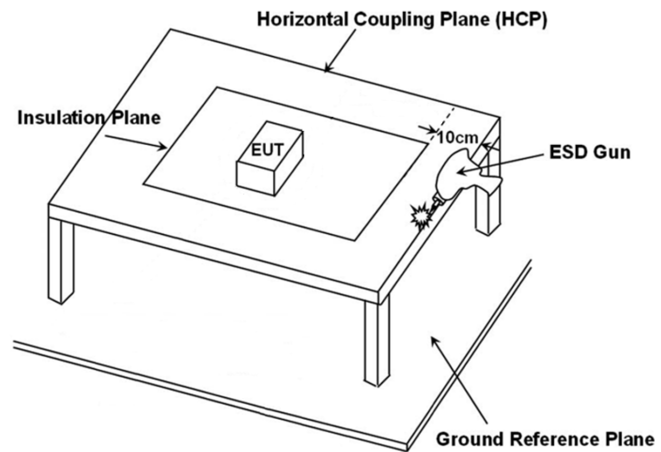


Fig. 4. Measurement setup of the system-level ESD test with the indirect contact-discharge test mode, as specified in the IEC 61000-4-2 standard [2].

port to transmit the signal. Another CMOS inverter (IC-2) is a reception port which is used to emulate the input port in the microelectronic system. The power pin of IC-1 is connected to V_{DD1} of 3.3 V, and the power pin of IC-2 is connected to V_{DD2} of 3.3 V. The input signal applied to the IC-1 is logic "low." Therefore, the signal received by the input pin of IC-2 is logic "high," and the output of IC-2 is kept at "low" state. The maximum output currents of CMOS IC-1 and CMOS IC-2 are 100 mA, which are larger than the holding currents of TVS-1, TVS-2, and TVS-3.

To emulate the ESD protection with TVS on the PCB of microelectronics system, a TVS is placed from the signal trace (that connecting the output pin of IC-1 and the input pin of IC-2) to ground. All these three devices (IC-1, IC-2, and TVS) are soldered to the PCB to form the equipment under test (EUT) for system-level ESD test. The transient voltage waveforms at the output pins of IC-1 and IC-2 during system-level ESD immunity test are monitored and recorded through separate voltage probes of the oscilloscope at the channel 1 (CH-1) and the channel 2 (CH-2), as illustrated in Fig. 3. Three commercial TVSs with different holding voltages will be tested. These three TVSs are all declared that it can be used as 3.3-V I/O port protection device. The EUT without TVS also will be tested as a reference. With the system-level ESD immunity test to these EUTs, we can investigate the impact of different holding voltages of TVS to the input or output ports of the microelectronics system.

Fig. 4 shows the measurement setup of the system-level ESD immunity test with the indirect contact-discharge test mode, as specified in the IEC 61000-4-2 standard [2]. The EUT in Fig. 4 is the whole PCB with power supplies (3.3 V) shown in Fig. 3. The system-level ESD gun with specified ESD voltage is zapping to the horizontal coupling plane (HCP), and the ESD energy will be coupled to the EUT [11]. The tested ESD level will start from 1000 V, and the increased step of ESD level is 1000 V.

B. Transient Response Under System-Level ESD Test

Under the system-level ESD immunity test (as illustrated in Fig. 4), the measured voltage waveforms at the output pin of IC-1 and the output pin of IC-2 with TVS-1 protection during the system-level ESD test of +1000 V zapping are shown in Fig. 5. Before the ESD zapping, the initial states

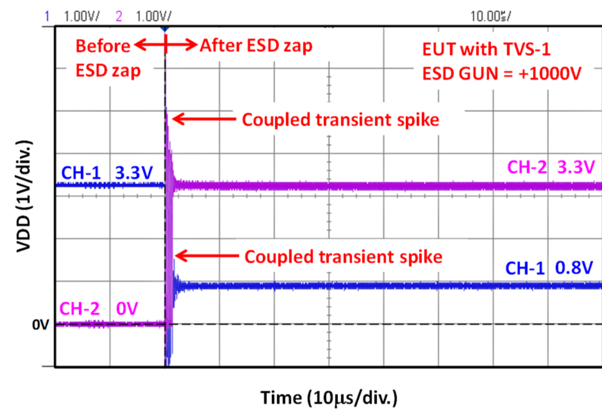


Fig. 5. Measured transient voltage waveforms at the output pin of IC-1 (voltage probe CH-1), and the output pin of IC-2 (voltage probe CH-2), with **TVS-1** protection during the system-level ESD test of +1000 V zapping.

at the output pins of IC-1 and IC-2 are kept at logic "high (3.3 V)" and logic "low (0 V)," respectively, as the CH-1 and CH-2 waveforms shown in Fig. 5. During the system-level ESD zapping, the transient voltage injected from the ESD gun will be coupling to the trace lines on the PCB, as the transient spikes observed in the CH-1 and CH-2 voltage waveforms.

After the ESD zapping of +1000 V, the voltage at the output pin of IC-1 is dropping to 0.8 V, even if the input signal at the input pin of IC-1 is still kept at logic low (0 V). The voltage at CH-1 is dropping from 3.3 to 0.8 V just after the transient spikes induced by ESD zapping. This clamping down voltage of 0.8 V is exactly the same as the holding voltage of TVS-1 in Fig. 1(b). The transient spikes during the system-level ESD test can trigger TVS-1 into its holding state, therefore, the signal voltage level at the output pin of IC-1 is clamping down to 0.8 V. The TVS-1 indeed turns on to clamp the transient spikes, and therefore, to well protect the ICs on the PCB against electrical overstress. But the signal voltage level at the output pin of IC-1 is locked by the lower holding voltage (0.8 V) of TVS-1, and it in turn causes the wrong logic state at the output pin of IC-2 to become logic high (3.3 V).

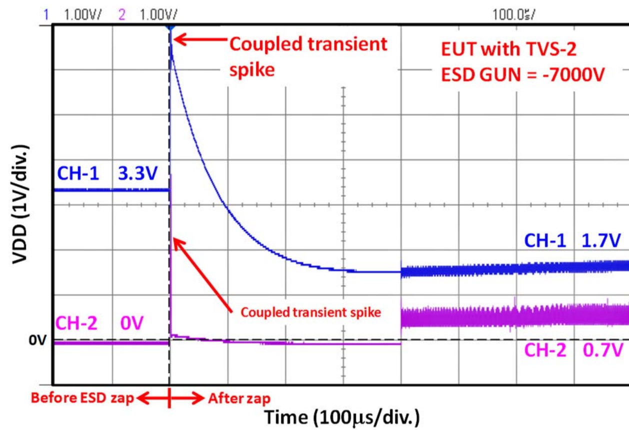


Fig. 6. Measured transient voltage waveforms at the output pin of IC-1 (voltage probe CH-1), and the output pin of IC-2 (voltage probe CH-2), with **TVS-2** protection during the system-level ESD test of −7000 V zapping.

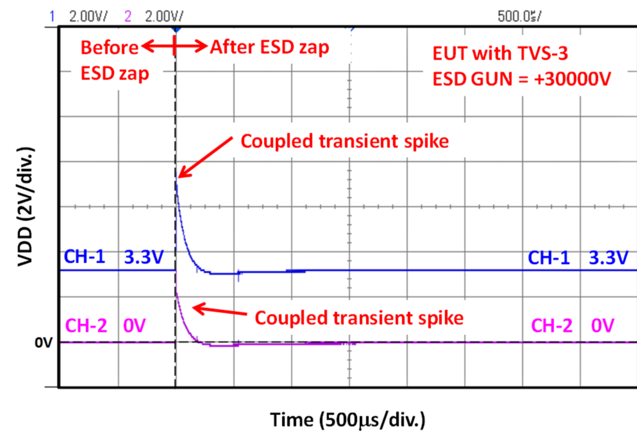


Fig. 7. Measured transient voltage waveforms at the output pin of IC-1 (voltage probe CH-1), and the output pin of IC-2 (voltage probe CH-2), with **TVS-3** protection during the system-level ESD test of +30 000 V zapping.

Such a wrong logic state induced by TVS-1 after system-level ESD immunity test will cause some mistake (soft error) or malfunction to the system operation, even if the hardware (CMOS ICs) was not damaged by the ESD stress. When the ESD voltage is higher (typically 8 kV in the most system-level applications), such signal-integrity issue will become even worse in the microelectronics system protected by this TVS-1.

The measured voltage waveforms at the output pins of IC-1 and IC-2 with TVS-2 protection during the system-level ESD immunity test of −7000 V zapping are shown in Fig. 6. After the ESD zapping of −7000 V, the voltage level at the output pin of IC-1 is dropping down and clamping at ∼1.7 V, which is near to the holding voltage of TVS-2 [as that measured in Fig. 1(b)]. Due to the voltage level clamped by TVS-2 at CH-1, the voltage level at the output pin of IC-2 (CH-2) is totally wrong (∼0.7 V). The output logic state at CH-2 changes from the logic "low" to an ambiguous state, which will cause serious malfunction to the system operation, after the system-level ESD zapping of −7000 V.

In Fig. 6, the long decay time on the voltage waveform at the output node of IC-1 is caused by the competition between the pull-up pMOS in the inverter of IC-1 (it is turned on to pull up the output node to VDD of 3.3 V) and the TVS-2 (it is triggered on to pull down the output node to GND of 0 V). The drain current of pMOS under such a voltage/bias condition is not so strong to compete the pull-down current of TVS-2, but it still can supply some current to pull up the output node. When the current difference between the pull-up current (by pMOS of IC-1) and the pull-down current (by TVS-2) is small, the time to cause the voltage dropping from 3.3 to 1.7 V at the output node of IC-1 will become longer, as shown in Fig. 6.

The measured voltage waveforms at the output pins of IC-1 and IC-2 with TVS-3 protection during the system-level ESD zapping of up to ±30 000 V are shown in Fig. 7. The ESD spike coupling to the output pin of IC-1 causes an overshooting voltage into the microelectronics system. Although the overshooting voltage can trigger on the TVS-3, the TVS-3 is turned off after the overstress voltage is released to ground. Due to the holding voltage of TVS-3 greater than the system operating voltage, the TVS-3 can turn off automatically after the coupled ESD energy is released. With a correct logic state (3.3 V) kept at the output pin of IC-1, the output logic state at CH-2 is also kept at its right state (0 V), after the system-level ESD zapping of up to ±30 000 V. Therefore, the TVS-3 can provide efficient system-level ESD protection to the PCB and also well keep the signal integrity of the microelectronics system.

TABLE I
SUMMARY OF SYSTEM-LEVEL ESD IMMUNITY TEST

	TVS-1	*TVS-2*	*TVS-3*	*Without TVS*
Failed ESD Voltage (V)	+1000	-7000	N.A.	-20000
Passed ESD Voltage (V)	N.A.	±6000	±30000	±19000
Voltage Probe CH1 before ESD ZAP (V)	3.3V (HIGH STATE)			
Voltage Probe CH2 before ESD ZAP (V)	0V (LOW STATE)			
Voltage Probe CH1 after ESD ZAP (V)	0.8	1.7	3.3	2.2
Voltage Probe CH2 after ESD ZAP (V)	3.3	0.7	0	0
Fail Mode	Signal Integrity Issue	Signal Integrity Issue	NO Fail	CMOS IC Permanent Damage

The EUT without TVS protection (control group) can pass the system-level ESD immunity test of ±19 000 V without any signal integrity issue. After the system-level ESD zapping of −20 000 V, the voltage at CH-1 is dropping down to 2.2 V. The voltage at CH-1 is always kept at 2.2 V after rebooting the EUT, thus the EUT is permanently damaged due to the −20 000-V system-level ESD immunity test [8]. The figure of the measured transient waveform of EUT without TVS during the system-level test is not shown here. The logic change and signal integrity issues are not observed and recorded by the oscilloscope during the system-level ESD test of the EUT without TVS. From the measurement result of the control group, all the test and measurement setups of the EUT without TVS will not influence the signal integrity.

The measurement results of the transient responses on the PCB protected by the TVSs under system-level ESD immunity test are summarized in Table I. The EUT without TVS protection can pass the system-level ESD test up to ±19 000 V. However, the passed ESD voltage of EUT with

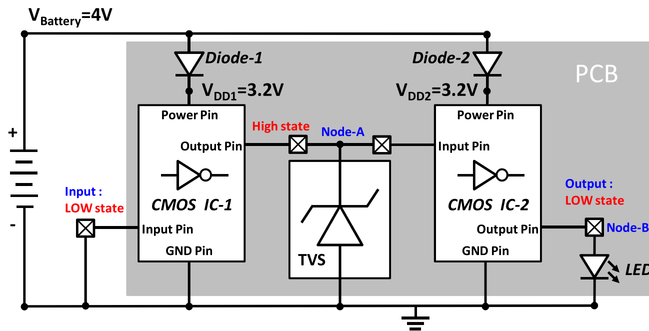


Fig. 8. Additional test setup without transient coupling path caused by the cables of voltage probe and power supply to the EUT.

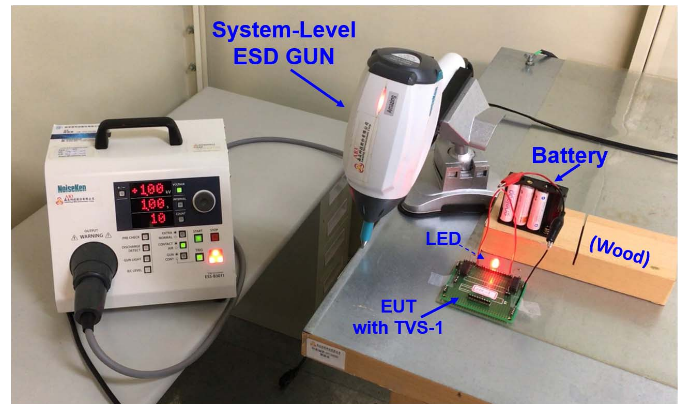


Fig. 9. LED was lit up on the new EUT with TVS-1 device after +1000-V system-level ESD test.

TVS-1 and TVS-2 protection are decreased to lower than 7000 V. Because the holding voltages of TVS-1 and TVS-2 are lower than the system operation voltage, the EUTs protected with these two TVSs cannot meet the immunity requirement of "level 4," due to the signal-integrity issue. To safely protect the microelectronics system against the system-level ESD overstress as well as to keep the signal integrity correct in the field applications, the holding voltage of TVS should be slightly higher than the maximum voltage level of signals in the microelectronics system.

C. Additional Verification on Transient Response

As the aforementioned test setup shown in Fig. 3, the voltage waveforms at the output nodes of IC-1 and IC-2 were monitored by voltage probes with probe cables, and the 3.3-V power sources to the IC-1 and IC-2 were from power supply with connection cables. The coupled transient spikes, which are measured by the voltage probes, may be disturbed by the probe cables. Even though all the voltage probe cables and the power supply cables were fully suspended in midair (with a distance of ~15 cm from the surface of HCP table) to prevent the ESD-induced transient coupling into these cables, someone would still wonder such possible coupling transients into the test board through the cable connections.

In order to completely remove the possible coupling path caused by the cables of voltage probe and the power supply, a new EUT setup without any cable connection is developed to repeat the system-level ESD test, which is shown in Fig. 8. The signal level at the output of IC-2 is now monitored by a light-emitting diode (LED) without any voltage probe, and a standalone 4-V battery is used as a power source rather than the power supply. The diode-1 and diode-2 are used to reduce the voltage levels at V_{DD1} and V_{DD2} from 4 V of battery to ~3.2 V for the 3.3-V CMOS IC-1 and IC-2, respectively. The input pin of CMOS IC-1 is connected to the ground (logic "low"). Therefore, the node-A in Fig. 8 will be 3.2 V (logic "high"), and the node-B at the output will be 0 V (logic "low"). The LED is connected from the node-B to ground, which is used as a logic-state detector. At the original state, the voltage of node-B is 0 V. Thus, the LED is kept at OFF-state without light emission. If the logic state of node-B is changed from logic "low" to logic "high" (3.2 V), the LED will be lit up. The TVS is placed from the node-A (that connecting the output pin of IC-1 and the input pin of IC-2) to ground. All these devices are soldered to the PCB to form the new EUT for system-level ESD test. The tested ESD level will start from 1000 V, and the increased step of ESD level is 1000 V. In addition to the logic-state detector, the voltage levels at node-A and node-B will be rechecked by digital multimeter after the system-level ESD test.

The new EUT with TVS-1 device cannot pass the first test level. As soon as a +1000-V ESD pulse is zapped to the HCP, the LED is lit up immediately, as shown in Fig. 9. Obviously, there is a logic error at the node-B. Measuring the voltage level by digital multimeter, the voltages at node-A and node-B are ~0.9 and ~2.0 V, respectively. The measured voltage of node-A is almost the same as the holding voltage of TVS-1 in Fig. 1(b). The voltage level at the node-A is locked by the lower holding voltage of TVS-1, and it in turn causes the wrong logic state at the node-B. The voltage of the node-B should be pulled up by CMOS IC-2 to 3.2 V (logic "high"), but the LED is lit up to pull down the voltage level at node-B to ~2.0 V.

After the +5000-V system-level ESD test to the new EUT with TVS-2 device, the voltage at node-A is dropped to ~1.8 V which is almost the same as the holding voltage of TVS-2 in Fig. 1(b). The TVS-3 device with its holding voltage higher than 3.2 V did not cause any failure on this new test setup, even if the ESD test voltage level was raised up to ±30 000 V (limited by the ESD gun). Table II shows the summary of the system-level ESD test results of the new EUT. The new EUT without any TVS device placed at the node-A can pass the system-level ESD test higher than ±16 000 V. During the system-level ESD test, neither signal integrity issue nor logic change of node-A and node-B were observed.

From the measurement results listed in Tables I and II, the logic error caused by the TVS-1 or TVS-2 devices cannot be restored automatically after the TVS was triggered on by the ESD-induced overshooting/undershooting transient voltage. The TVS-1 or TVS-2 device was kept at its holding state to pull down the output voltage (at node-A) of IC-1 to its holding voltage. Thus, the signal integrity of the system operations was destroyed after the system-level ESD test. From this additional verification on transient response, the holding

TABLE II
SUMMARY OF SYSTEM-LEVEL ESD IMMUNITY TEST OF THE NEW EUT SETUP

	TVS-1	TVS-2	TVS-3	Without TVS
Failed ESD Voltage (V)	+1000	+5000	N.A.	N.A.
Passed ESD Voltage (V)	N.A.	±4000	±30000	>|±16000|
Node-A before ESD ZAP (V)	3.2V (HIGH STATE)			
Node-B before ESD ZAP (V)	0V (LOW STATE)			
Node-A after ESD ZAP (V)	0.9	1.8	3.2	3.2
Node-B after ESD ZAP (V)	2.0	0	0	0
LED	ON	OFF	OFF	OFF
Fail Mode	Signal Integrity Issue	Signal Integrity Issue	NO Fail	NO Fail

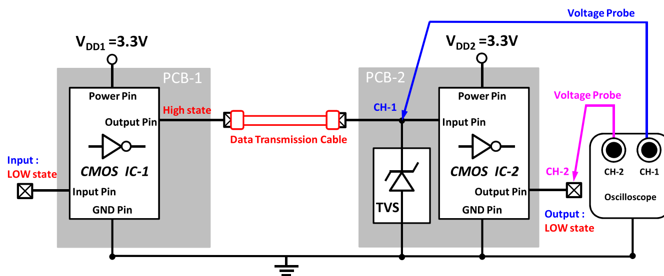


Fig. 10. Test setup with two CMOS ICs (IC-1 and IC-2) connected by the data transmission cable and protected by a TVS.

voltage of TVS should be slightly higher than the maximum voltage level of signals in the microelectronics system to keep the correct signal integrity in the field applications.

The battery wiring and the absence of a good return plane in the EUT may increase the sensitivity of the circuit toward disturbances by ESD. A decoupling capacitance between the VDD and GND can be a good choice to stabilize the voltage and to reduce the ESD-induced transient noise into the microelectronics system.

IV. EFT/B Immunity Test

The EFT/B immunity test is a test with bursts consisting of a number of fast pulses, coupled into the power supply, control, signal, and ground ports of microelectronic equipment. The characteristics of EFT/B immunity tests are high amplitude, short rise time, high repetition rate, and low energy of the transient. The EFT/B immunity test is intended to demonstrate the immunity of electronic equipment to transient disturbances such as those originating from switching transient.

A. Test Setup for EFT/B immunity Test

Fig. 10 shows the test setup for the EFT/B immunity test. The CMOS inverter (IC-1) is used to emulate a transmission port to transmit the signal, and the IC-1 will be soldered to a PCB-1. Another CMOS inverter (IC-2) is used to emulate a reception port to receive the digital data from the transmission port IC-1. A protection device TVS will be placed from input pin of CMOS inverter (IC-2) to ground. The CMOS inverter (IC-2) and the protection device TVS will be soldered to another PCB-2. A data transmission cable will be connected to the output pin of IC-1 and the input pin of IC-2. All these three devices (IC-1, IC-2, and TVS) and the data transmission cable form the EUT for EFT/B immunity test.

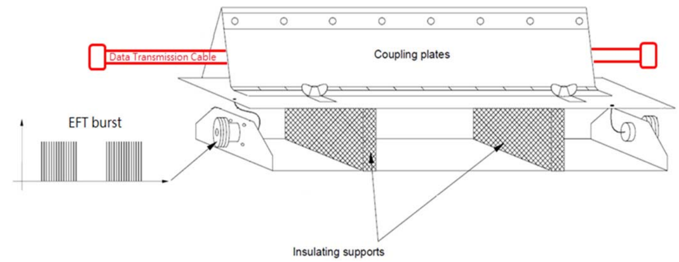


Fig. 11. Capacitive coupling clamp for the EFT/B immunity test [3].

The power pin of IC-1 is connected to V_{DD1} of 3.3 V, and the power pin of IC-2 is connected to V_{DD2} of 3.3 V. The input signal applied to the IC-1 is logic "low." Therefore, the signal received by the input pin of IC-2 is logic "high," and the output of IC-2 is kept at "low" state. The transient voltage waveforms at the input pin and output pin of IC-2 during EFT/B immunity test are monitored and recorded through separate voltage probes of the oscilloscope at the channel 1 (CH-1) and the channel 2 (CH-2), as illustrated in Fig. 10. Three commercial TVSs, as mentioned previously, with different holding voltages will be tested. With the EFT/B immunity test to these EUTs, we can investigate the impact of different holding voltages of TVS to the input or output ports of the microelectronics system.

Fig. 11 shows the capacitive coupling clamp for the EFT/B immunity test [3]. The data transmission cable (as shown in Fig. 10) will be placed into the coupling plates of the capacitive coupling clamp, as shown in Fig. 11. And the EFT/B is zapping to the coupling plates. Therefore, the EFT pulse will couple to the data transmission cable and the EUT. The EFT/B test voltage will start from 200 V for both positive and negative pulse, and the increased step of EFT/B test voltage is 200 V. The repetition frequency of EFT burst will be 5 kHz, thus, there are 75 pulses in each burst. And the burst duration time is 15 ms. Therefore, the time interval between two adjacent EFT pulse is 0.2 ms. The duration of the EFT/B immunity test will be 1 min.

B. Transient Response Under EFT/B Immunity Test

Under the 200-V EFT/B voltage zapping to the coupling clamp (as illustrated in Fig. 11), the transient waveform of the input pin and the output pin of IC-2 with protection device TVS-1 are measured and shown in Fig. 12. Before the EFT/B zapping, the initial states at the input pin and the output pin of IC-2 are kept at logic "high (3.3 V)" and logic "low (0 V)," respectively, as the CH-1 and CH-2 waveforms shown in Fig. 12. During the EFT/B zapping to the coupling clamp, the EFT pulse will couple to the data transmission line and couple into the CMOS IC-1 and IC-2. After the 200-V EFT/B zapping, the voltage at the input pin of IC-2 is dropping from 3.3 to 0.8 V, even if the input signal at the input pin of IC-1

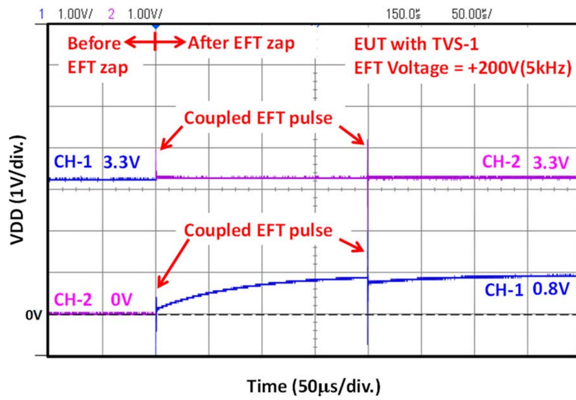


Fig. 12. Measured transient voltage waveforms at the input pin of IC-2 (voltage probe CH-1), and the output pin of IC-2 (voltage probe CH-2), with **TVS-1** protection during the EFT/B test of +200 V zapping.

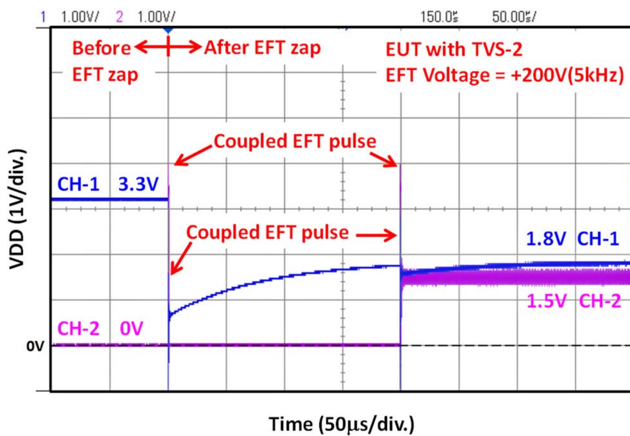


Fig. 13. Measured transient voltage waveforms at the input pin of IC-2 (voltage probe CH-1), and the output pin of IC-2 (voltage probe CH-2), with **TVS-2** protection during the EFT/B test of +200 V zapping.

is still kept at logic low (0 V). This clamping down voltage of 0.8 V is exactly the same as the holding voltage of TVS-1 in Fig. 1(b). The coupled EFT pulse can trigger TVS-1 into its holding state, therefore, the signal voltage level at the input pin of IC-2 is clamping down to 0.8 V. The TVS-1 indeed turns on to clamp the coupled EFT pulse, and therefore, to well-protect the ICs on the PCB against electrical overstress. But the signal voltage level at the input pin of IC-2 is locked by the lower holding voltage (0.8 V) of TVS-1, and it in turn causes the wrong logic state at the output pin of IC-2 to become logic high (3.3 V). Such a wrong logic state induced by TVS-1 after EFT/B immunity test will cause some mistake (soft error) or malfunction to the system operation, even if the hardware (CMOS ICs) was not damaged by the EFT/B immunity test. When the EFT/B voltage is higher (typically 2000 V in the I/O and communication ports), such signal integrity issue will become even worse in the microelectronics system protected by this TVS-1.

Fig. 13 shows the measured transient waveform of input pin and output pin of IC-2 with protection device TVS-2 during the 200-V EFT/B immunity test. After the EFT/B test of +200 V, the voltage level at the input pin of IC-2 is dropping down and clamping at ∼1.8 V, which is near to the holding voltage of TVS-2 [as shown in Fig. 1(b)]. The voltage level of the received data of IC-2 (CH-1) was clamped by TVS-2. Thus, the output voltage (1.5 V) of IC-2 (CH-2) is totally wrong. The output logic state at CH-2 changes from the logic "low" to an ambiguous state, which will cause serious malfunction to the system operation, after the EFT/B test of +200 V.

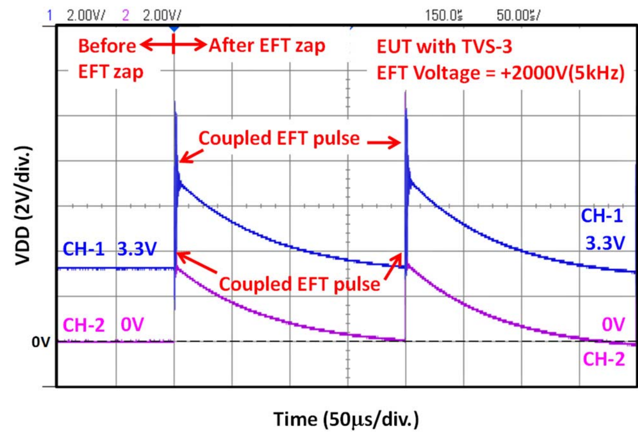


Fig. 14. Measured transient voltage waveforms at the input pin of IC-2 (voltage probe CH-1), and the output pin of IC-2 (voltage probe CH-2), with **TVS-3** protection during the EFT/B test of +200 V zapping.

TABLE III
SUMMARY OF EFT IMMUNITY TEST

	TVS-1	*TVS-2*	*TVS-3*
Failed EFT Test Voltage (V)	+200	+200	N.A.
Passed EFT Test Voltage (V)	N.A.	N.A.	>±2000
Voltage Probe CH1 before EFT Test (V)	3.3V (HIGH STATE)		
Voltage Probe CH2 before EFT Test (V)	0V (LOW STATE)		
Voltage Probe CH1 after EFT Test (V)	0.8	1.8	3.3
Voltage Probe CH2 after EFT Test (V)	3.3	1.5	0
Fail Mode	Signal Integrity Issue	Signal Integrity Issue	NO Fail

The measured transient voltage waveforms at the input pin and the output pin of IC-2 with TVS-3 protection during the EFT/B zapping of +2000 V are shown in Fig. 14. The EFT pulse coupling to the input pin of IC-2 causes an overshooting voltage into the microelectronics system. The overshooting voltage can trigger on the TVS-3. Because the holding voltage of TVS-3 is greater than the system operating voltage, the TVS-3 can turn off after the coupled EFT pulse is released to ground. With a correct logic state (3.3 V) kept at the input pin of IC-2, the output logic state of IC-2 is also kept at its right state (0 V), after the EFT/B test of up to ±2000 V. Therefore, the TVS-3 can provide efficient EFT/B protection to the PCB, and also well keep the signal integrity of the microelectronics system.

The measurement results of the transient responses on the PCB protected by the TVSs under EFT/B immunity test are summarized in Table III. Only the EUT with TVS-3 can pass the ±2000 V EFT/B immunity test to achieve the immunity

requirement of "level 4" in the EFT/B standard [3]. The EUTs protected with TVS-1 and TVS-2 cannot pass the 200-V EFT/B immunity test. And the fail-mode of these two EUTs is not CMOS IC damage but signal integrity issue. This is because the holding voltages of TVS-1 and TVS-2 are lower than the system operation voltage. As soon as these TVSs were triggered by the coupled EFT pulse, the voltage levels of input pin of IC-2 are locked at the holding voltage of these TVSs and cause the signal integrity issue. To safely protect the microelectronics system against the EFT/B overstress as well as to keep the signal integrity correct in the field applications, the holding voltage of TVS should be slightly higher than the maximum voltage level of signals in the microelectronics system.

V. Conclusion

The signal integrity of microelectronics system protected by three commercial TVSs with different holding voltages has been investigated in detail under the system-level ESD test and EFT/B test. From the measurement result, the EUTs with the TVS which have the holding voltages lower than the operation voltage cannot achieve the immunity requirement of "level 4" in both system-level ESD and EFT/B standards. The failure modes of these failed EUTs do not cause permanent damage on CMOS ICs but the signal-integrity issue is caused by the TVS. From the experimental results of this work, only the EUT with TVS-3 in which its holding voltage is greater than the system operation voltage can pass the system-level ESD test up to ±30 000 V and EFT/B test up to ±2000 V. To keep the correct signal integrity in microelectronics system, the TVS with holding voltage greater than the system operation voltage is strongly recommended.

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