A Global Shutter Wide Dynamic Range Soft X-Ray CMOS Image Sensor With Backside-Illuminated Pinned Photodiode, Two-Stage Lateral Overflow Integration Capacitor, and Voltage Domain Memory Bank

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***Abstract*— This article presents a prototype 22.4 μm pixel pitch global shutter (GS) wide dynamic range (WDR) soft X-ray CMOS image sensor (sxCMOS). Backside-illuminated (BSI) pinned photodiodes with a 45-μm thick Si substrate were introduced for low noise and high radiation hardness to high energy photons. Two-stage lateral overflow integration capacitor (LOFIC) and voltage domain memory bank with high-density Si trench capacitors were introduced for WDR and for GS. The developed sxCMOS achieved maximum 21.9 Me$^-$ full well capacity with a single exposure 129 dB dynamic range by GS operation. Over 70% quantum efficiency (QE) toward soft X-ray was successfully achieved. The developed prototype sxCMOS is a step forward toward a 4 M pixel detector system to be utilized in next-generation synchrotron radiation facilities and X-ray free-electron lasers.**

***Index Terms*— Backside-illuminated (BSI), CMOS image sensor (CIS), coherent X-ray diffraction imaging (CDI), global shutter (GS), lateral overflow integration capacitor (LOFIC), soft X-ray, wide dynamic range (WDR).**

Manuscript received November 30, 2020; revised January 26, 2021 and February 19, 2021; accepted February 22, 2021. Date of publication March 15, 2021; date of current version March 24, 2021. This work was supported in part by the SACLA Basic Development Program 2020. This article is an extended version of a paper presented at IEDM 2020. The review of this article was arranged by Editor T. Grasser. *(Corresponding authors: Hiroya Shike; Rihito Kuroda.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2021.3062576.

Digital Object Identifier 10.1109/TED.2021.3062576

I. Introduction

SOFT X-ray imaging is an important methodology in surface and chemical science. Among various analyses, a field of coherent soft X-ray diffraction imaging has been rapidly developing for analyzing structures and chemical, electronic and magnetic states of target materials [1]. As performances of light sources are improving, a single-shot coherent diffraction imaging with short-pulsed high brilliance light is expected to be useful for analyzing dynamic reactions such as catalytic reaction, magneto-optical effect, and so on. However, the current soft X-ray imager's dynamic range that can be achieved with single-shot imaging is not sufficient, thus multiple exposures are necessary to expand the dynamic range. In addition, the framerate of current soft X-ray imagers is not sufficient for dynamic observation. Consequently, a wide dynamic range (WDR) fast readout soft X-ray imager is highly desired. Development of detectors is, therefore, actively conducted in this field [2], [3].

For CMOS image sensors (CIS), WDR, and global shutter (GS) technologies attract much attention due to their usefulness in various sensing applications such as automobile, drones, machine vision, and so on [4]–[9].

There are four major linear response WDR approaches: multiple exposure [10], dual conversion gain (CG) [5], combination of photodiodes (PDs) [11], and lateral overflow integration capacitor (LOFIC) [12]–[14]. Among various linear response WDR technologies, LOFIC, which is a single exposure single PD and scalable high full well capacity (FWC) scheme,

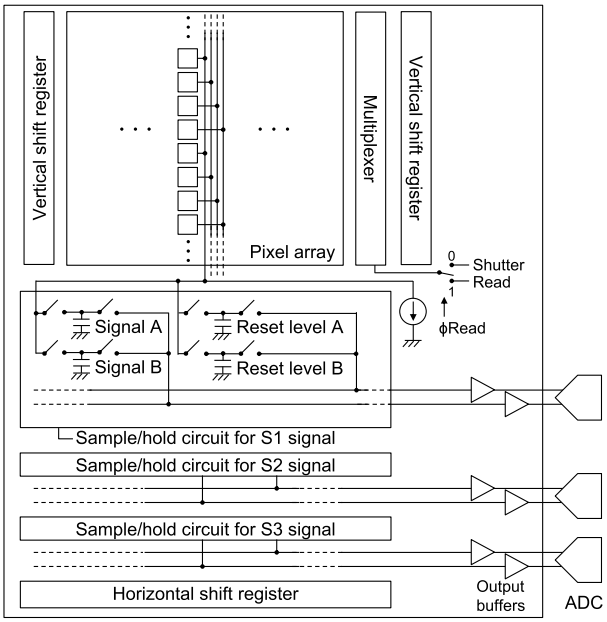

Fig. 1. Circuit block diagram of the developed sxCMOS.

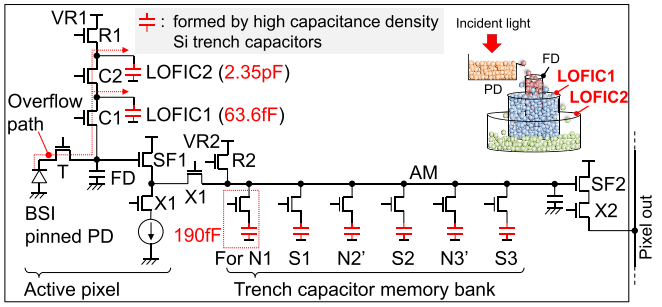

Fig. 2. Pixel circuit block diagram of the developed sxCMOS.

TABLE I
SIGNAL DEFINITIONS OF TWO-STAGE LOFIC

Signal	Photoelectron integration	Charge to voltage conversion
High sensitivity S1	PD	FD
High saturation S2	PD + FD + LOFIC1	FD + LOFIC1
Highest saturation S3	PD + FD + LOFIC1 + LOFIC2	FD + LOFIC1 + LOFIC2

is considered to be suitable for soft X-ray imaging. In addition, voltage domain GS CIS has improved their noise performance thanks to the high-density capacitor technologies employed in recent years [15]–[17].

In this work, we present a 22.4-μm pixel pitch prototype GS, single exposure WDR soft X-ray CMOS image sensor (sxCMOS) using backside-illuminated (BSI) pinned PD with a 45-μm thick fully depleted Si substrate, two-stage LOFIC, and voltage domain memory bank consists of high-density Si trench capacitors. The developed prototype sxCMOS is a step forward toward 4 M pixel detector system to be utilized in next-generation synchrotron radiation facilities and X-ray free-electron lasers [18].

II. DEVELOPED SXCMOS ARCHITECTURE AND TECHNOLOGY

A. Circuit Architecture and Operation

Fig. 1 shows the circuit block diagram of the developed sxCMOS. It consists of a pixel array, vertical and horizontal scan circuits for signal readout, column readout circuit, and output buffers. There are four vertical output lines per column in order to decrease the signal readout period. Multiplexers choosing the shutter mode or the readout mode by ϕ Read are placed in every four rows. In the shutter mode, signals of all pixels are stored in trench capacitor-based voltage domain memory banks inside pixels simultaneously. In the readout mode, signals of four rows are readout in parallel from the memory banks to the column sample/hold capacitors. A sample/hold circuit has two sampling paths; A and B. For low noise readout mode, they are combined to reduce the thermal noise, and for high-speed readout mode, they are used for a pipeline operation. In addition, toward a 1 M pixel chip, parallel signal outputs will be employed in order to maintain high-speed signal readout for an increased number of pixels. This architecture enables a 1000 frames/s operation.

Fig. 2 shows the pixel circuit block diagram of the developed sxCMOS. The pixel consists of a BSI pinned PD, a transfer gate (T), a floating diffusion (FD), a first source follower driver (SF1), a current source switch (X1), a first overflow switch (C1), a LOFIC1, a second overflow switch (C2), a LOFIC2, a reset gate (R1), a memory bank reset gate (R2), a voltage domain memory bank for six signals (N1, S1, N2', S2, N3', S3) consisting of sampling switches and capacitors, a second source follower driver (SF2), and a select switch (X2). The two-stage LOFIC architecture was employed to achieve a WDR over 120 dB while maintaining a high signal-to-noise ratio (SNR) at signal switching points and high linearity [19], [20]. Here, high capacitance density Si trench capacitors, having the same unit layout, are employed for both LOFICs and memory bank; LOFIC1 uses one unit (63.6 fF), LOFIC2 uses 37 units (2.35 pF), and each memory capacitor uses three units (190 fF). The thermal noise due to the voltage domain memory capacitors is about 220 μV_{rms} at 60 °C thanks to the high-density trench capacitors. For instance, a photon of 100 eV is converted to 27.4 electron–hole pairs in average in Si. Considering the thermal noise arising at the voltage domain memory capacitors as the main noise source, photon counting with SNR of above 6 is possible by this design for 100 eV photons. By combining the two-stage LOFIC technology with the voltage domain memory bank, a GS operation is implemented with a WDR covering single-photon detection level sensitivity to very high FWC of over 20 Me^-. Also, the signal readout is carried out during the integration period of the next frame. Subsequently, the dead time of the integration is only several microseconds which is below 1% of the frame period even at 1000 frames/s.

Table I shows the signal definitions of two-stage LOFIC. A high sensitivity signal S1 integrates photoelectrons at PD and the signal charge is converted at FD. A high saturation signal S2 integrates photoelectrons at PD + FD + LOFIC1

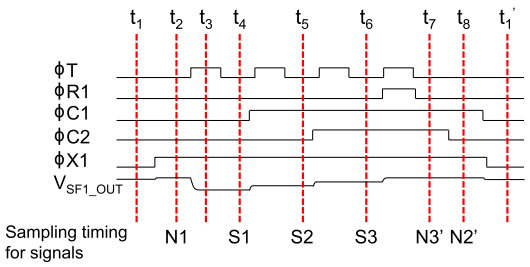

Fig. 3. Pixel operation timing diagram of the developed sxCMOS.

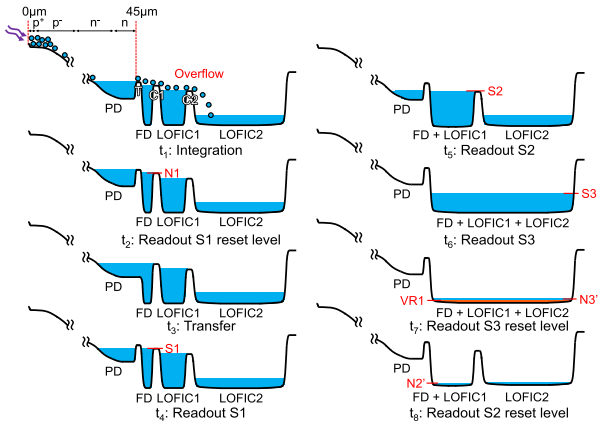

Fig. 4. Potential diagrams of the developed sxCMOS.

and signal charge is converted at FD + LOFIC1. The highest saturation signal S3 integrates photoelectrons at PD + FD + LOFIC1 + LOFIC2 and signal charge is converted at FD + LOFIC1 + LOFIC2.

Figs. 3 and 4 show the pixel operation timing and the potential diagrams of two-stage LOFIC GS operation, respectively. In order to achieve a high long-term reliability, a 45-μm thick Si was employed so that the high-energy photons do not penetrate to transistors region formed near the frontside surface. The detailed explanation will be given later. The photoelectrons generated near the backside are drifted to the PD and accumulated. An overflow path of two-stage LOFIC is formed by tuning gate voltage levels of T, C1, and C2 during the integration period [21]. The gate voltage levels were tuned so that both formation of the overflow path and sufficient saturation of each signal were achieved. When a high-intensity light is irradiated to a pixel during the integration period (t1), overflow photoelectrons from PD and FD are accumulated in the LOFIC1 and overflow photoelectrons from the LOFIC1 are accumulated in the LOFIC2. A reset signal for the high sensitivity signal S1 converted at the FD (N1) is readout and stored in the memory at t2. Photoelectrons accumulated in the PD are transferred to the FD at t3. A high sensitivity signal converted at the small capacitance FD (S1), a high saturation signal converted at FD + LOFIC1 (S2), and the highest saturation signal converted at FD+LOFIC1+LOFIC2 (S3) are readout and stored in each memory at t4, t5, and t6, respectively. After the PD reset, a reset signal for the highest saturation signal S3 converted at FD + LOFIC1 + LOFIC2 (N3') is readout and stored in the memory at t7. A reset signal

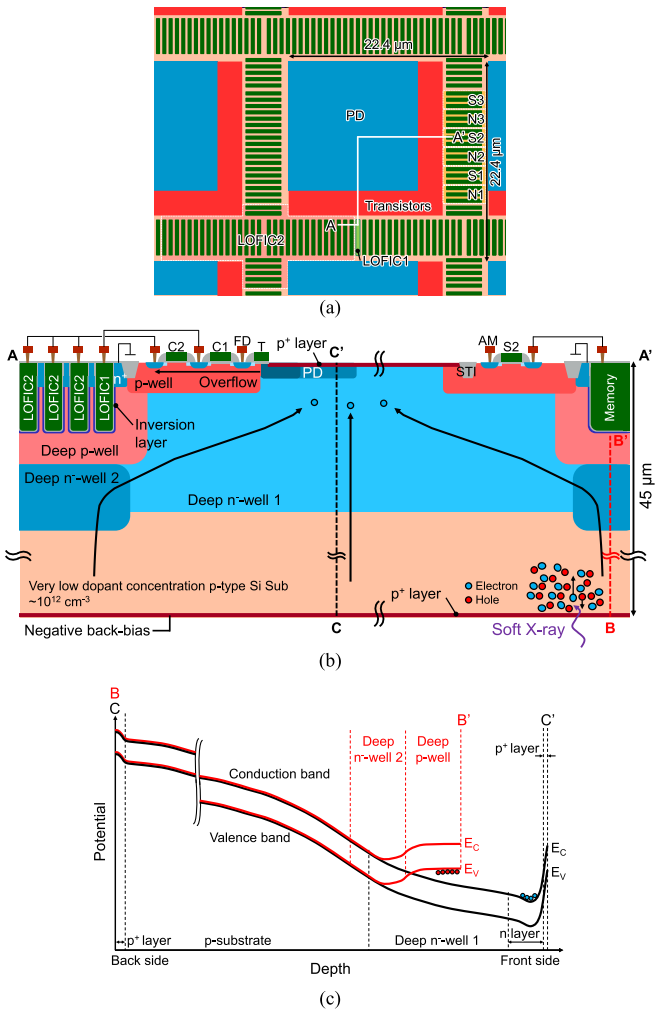

Fig. 5. (a) Pixel layout of the developed sxCMOS. (b) Pixel cross-sectional diagram of line A-A' around LOFICs, memory bank and PD. (c) 1-dimension potential diagrams of line B-B' and C-C'.

for the high saturation signal S2 converted at FD + LOFIC1 (N2') is readout and stored in the memory at t8. During the next integration period, six signals are readout sequentially from the memory bank to column sample/hold capacitors by four rows in parallel. Three pairs of each signal and its reset signal are readout by three differential analog-to-digital converters (ADCs) outside the chip. The high-sensitivity signal S1 is obtained by N1-S1 correlated double sampling. The high saturation signal S2 and the highest saturation signal S3 are obtained by N2'-S2 and N3'-S3 double samplings, respectively.

B. BSI Pinned PD With High Radiation Hardness and Soft X-Ray Sensitivity

Fig. 5(a) and (b) shows the layout and the cross-sectional diagrams of the 22.4-μm pitch pixel of the prototype sxCMOS developed in this work, respectively. LOFIC and capacitor memory bank have the same unit trench capacitor layout and are used to isolate pixels symmetrically. This layout is suitable for coherent soft X-ray diffraction imaging, which calculates real-space image from measured Fourier magnitude,

because it is important to reduce the crosstalk and count accurate number of incident photons for each pixel. The size of PD was designed to measure the characteristics of both frontside-illuminated (FSI) and BSI for testing.

In order to achieve a WDR and photon counting level sensitivity to soft X-ray photons, a direct detection sensor with high radiation hardness is required. Direct irradiation of soft X-ray to detectors can cause fluctuations in MOS transistor threshold voltages [22]. Penetration lengths of soft X-rays in Si are about 40 nm at 100 eV, and about 3 μm at 1 keV [23]. The penetration length is a length at which incident light intensity decreases to 1/e times, thus, in order to achieve sufficient radiation hardness toward high energy photons, Si substrate thickness should be much thicker than the penetration length. The developed sxCMOS employed a 45-μm thick p-type Si substrate with BSI so as to ensure 100 Gy radiation hardness of the semiconductor devices toward 1 keV soft X-ray. The developed sxCMOS aims to be tolerant for use of two years or longer for a practical usage at synchrotron facilities [24].

In the X-ray region, multiple electron–hole pairs are generated from a single photon. For example, a 100 eV photon generates 27.4 electron–hole pairs in average [25]. In addition, penetration length of Si around 100 eV soft X-ray is very short. To enhance quantum efficiency (QE) toward 100 eV soft X-ray and minimize random noise and dark current shot noise, full depletion of the 45-μm thick p-type Si substrate and full transfer of a large number of photoelectrons generated at shallow depth on the backside are needed. In order to achieve full depletion of a thick p-type Si substrate, low oxygen concentration Czochralski-grown (Cz) Si wafer with oxygen concentration in the order of 10^{17} cm^{-3} was employed. The acceptor concentration was in the order of 10^{12} cm^{-3}. In addition, a back-bias was applied to increase the depletion width [26], [27]. However, applied a negative back-bias induces a hole leakage current between backside p^+ surface and p-well regions near the frontside surface. In order to suppress the leakage current while transferring photoelectrons, deep n^--wells were formed beneath the PD and p-wells. Fig. 5(c) shows the 1-dimension potential diagrams of line B-B' and C-C', respectively. The dopant concentrations of deep n^--wells were designed so that they are also depleted when the p-type Si substrate is fully depleted. By the electric field formed near the backside and the potential gradient formed near the frontside of the Si substrate, photoelectrons are transferred from backside surface to n-type storage layer near the frontside while suppressing the leakage current. Here the width of deep n^--well 2 was designed to be narrow so that there is a potential gradient for electrons from deep n^--well 2 toward deep n^--well 1. Also, this BSI pinned PD structure reduces parasitic light sensitivity. Because of the thick Si substrate with BSI, soft X-ray rarely penetrates the diffusion layer of the memory bank switches. So the direct photoelectric conversion at the diffusion layer rarely occurs. The potential gradient for electrons is formed so that photoelectrons rarely contaminate the diffusion layer of the memory bank switches. By doing so, the BSI pinned PD structure with the 45-μm thick Si substrate that satisfies sufficient radiation hardness, high QE, and lower leakage current was formed for soft X-ray imaging.

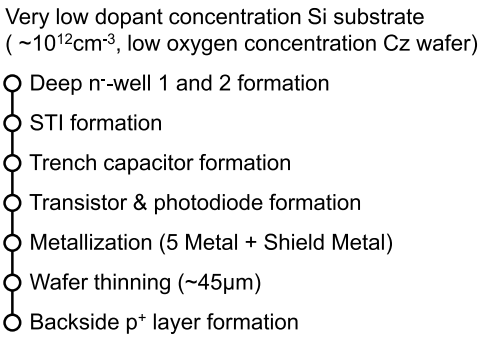

Fig. 6. Process flow of the developed sxCMOS.

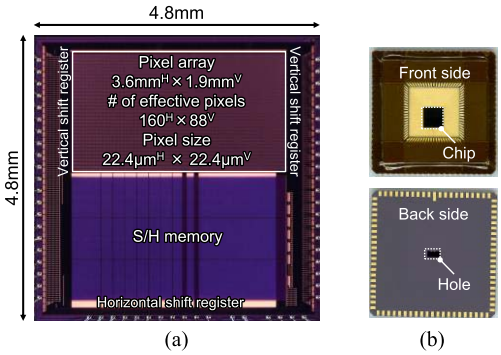

Fig. 7. Micrograph of (a) developed prototype sxCMOS chip and (b) package.

C. Chip Fabrication

Fig. 6 shows the fabrication process flow of the developed sxCMOS based on a 0.18 μm one-poly-Si five-Metal layer CMOS process technology with BSI pinned PD and trench capacitor. The diameter of the Si wafer was 200 mm. Deep n^--well 1 and 2 were formed by a high energy ion implantation and thermal diffusion due to drive-in anneal. The Si substrate of 45-μm thick was thinned by using backside grinding and chemical mechanical polishing processes. After wafer thinning, backside p^+ layer was formed by a p-type ion implantation and laser anneal to the backside surface.

Fig. 7(a) and (b) shows the micrograph of the developed prototype sxCMOS chip with $160^H \times 88^V$ effective pixels and the ceramic package, respectively [28]. Both FSI and BSI were tested using the same ceramic package with a hole under the pixel region. With the same circuit design scheme, the pixel number can be increased to $1024^H \times 1024^V$. In addition, by stitching four chips closely, an sxCMOS detector system with effective pixel number of $2048^H \times 2048^V$ is to be developed.

III. Measurement Results and Discussion

Figs. 8 and 9 show the measured chip leakage current characteristics and the cross-sectional diagram near the chip

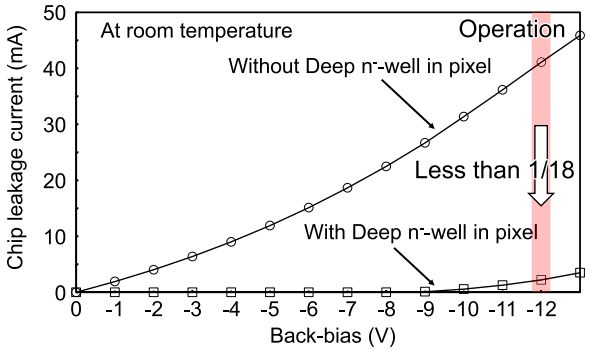

Fig. 8. Measured chip leakage current characteristics.

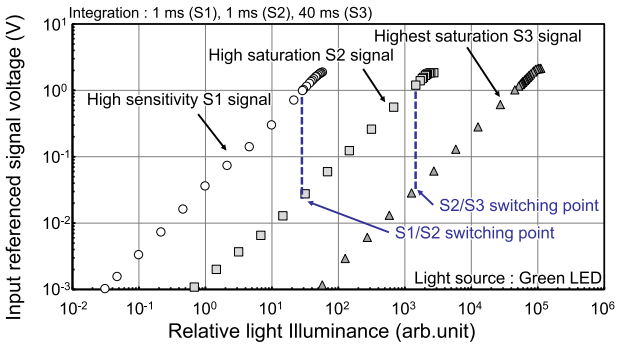

Fig. 10. Measured photoelectric conversion characteristics.

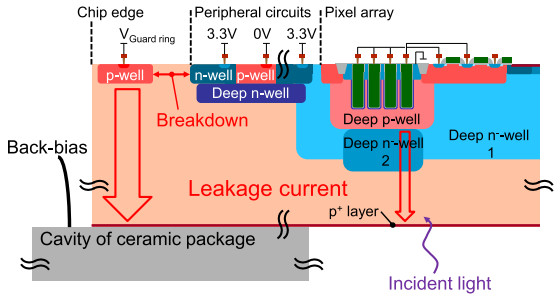

Fig. 9. Chip edge cross-sectional diagram of the developed prototype sxCMOS.

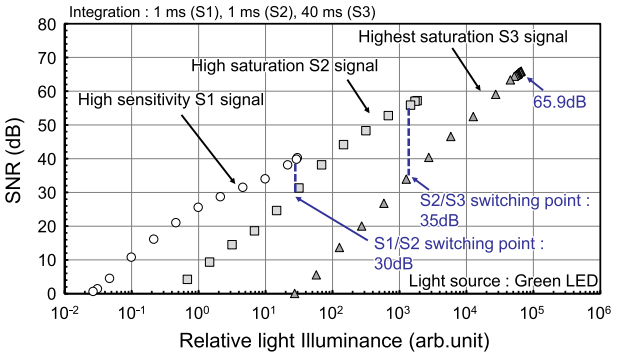

Fig. 11. Measured SNR characteristics.

edge of the developed prototype sxCMOS. The chip leakage current is mainly a hole current between backside p^+ surface and p-well regions near the frontside surface. The leakage current was suppressed by forming a potential barrier to holes using a p-n junction as shown in Fig. 5(c). A well-in-well structure in peripheral circuits and deep n^--wells in pixel were employed. In order to test both FSI and BSI using the same prototype chip, a back-bias was applied from a cavity of the ceramic package. The purpose of this measurement was to confirm the effect of deep n^--wells in pixel at room temperature by measuring two types of prototype chips with and without deep n^--wells. Deep n^--wells were effective to suppress the leakage current, but a large chip leakage current occurred near the chip edge because the applied voltage of $V_{\text{Guard ring}}$ was limited by its breakdown voltage between n-well and p-well near the chip edge. The breakdown voltage near the chip edge is to be increased and the leakage current near the chip edge will be suppressed in the next prototype development. The back-bias will be applied from $V_{\text{Guard ring}}$ in a 1 M pixel chip by optimizing the chip structure. The developed prototype sxCMOS operated at -12 V back-bias, which is expected to achieve full depletion of the 45-μm thick Si substrate by TCAD simulation.

Figs. 10 and 11 show the measured photoelectric conversion characteristics and SNR characteristics of the developed sxCMOS. The integration time of the high sensitivity S1 signal and the high saturation S2 signal was 1 ms because the sxCMOS will be operated at 1000 frames/s. The integration time of the highest saturation S3 signal was 40 ms because the illuminance of the employed light source was not enough to saturate the signal within 1 ms. A 129-dB WDR with linear response was obtained by S1, S2, and S3 signals under single exposure by GS operation. The measured CGs of the S1, S2, and S3 were 100 μV/e^-, 2.5 μV/e^-, and 68 nV/e^-. The FWCs of the S1, S2, and S3 were 10.3 ke^-, 602 ke^-, and 21.9 Me^-. The dark random noise of 8.1 e^-_{rms} was obtained by the S1 signal and the maximum SNR of 65.9 dB was obtained by the S3 signal. In addition, high SNR at the signal switching points was confirmed: 30 dB at S1-S2 and 35 dB at S2-S3, respectively, which is suitable for scientific imaging. Fig. 12 shows the synthesized signal electrons of the S1, S2, and S3 signal. Linear response was obtained in synthesized signal.

LOFIC has the advantage of single exposure, single PD, and scalable high FWC. However, variation in trench capacitors for LOFIC and a dark current at LOFIC cause nonideal characteristics. Variation in capacitance of LOFIC affects photoresponse nonuniformity (PRNU). A dark current at LOFIC affects dark signal nonuniformity (DSNU). PRNU and DSNU of LOFIC were measured by the FSI chip mounted on the ceramic package without the backside hole to remove the effect of BSI pinned PD structure. The measured PRNU and DSNU of the S2 signal in the center 3600 pixels under room temperature were 0.8% ($\pm 1\sigma$) and 113 e^-_{rms}, respectively. The measured DSNU contains a PD dark current fixed pattern noise and charge transfer noise. DSNU is smaller than the thermal noise arising at the analog memory (AM) bank, which is 144 e^-_{rms} for S2 signal (input-referred).

Figs. 13 and 14 show the breakdown of the measured dark random noise characteristics and the distribution of dark

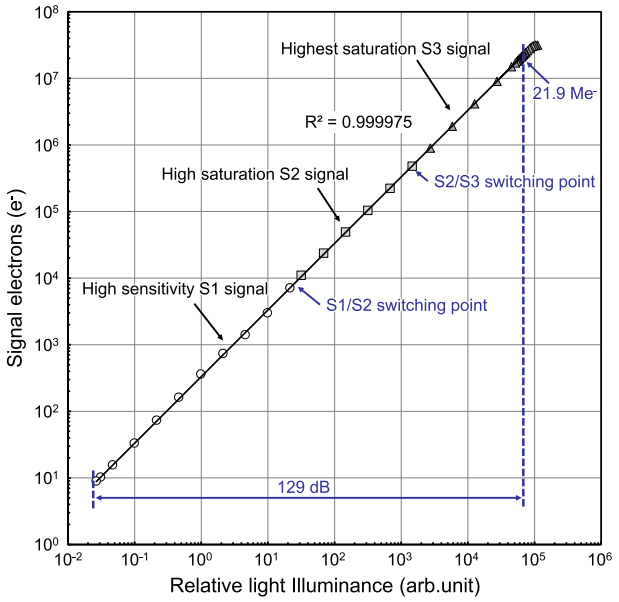

Fig. 12. Synthesized signal electrons of S1 + S2 + S3.

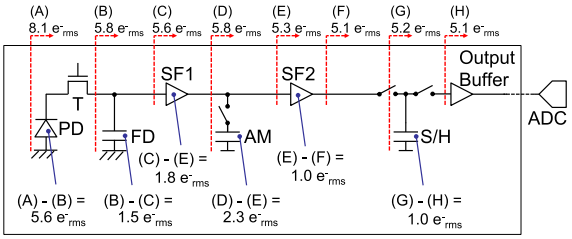

Fig. 13. Breakdown of the measured dark random noise characteristics. (A) Dark random noise, (B) dark random noise with T gate off, (C) reading out VR1 with fixed FD without using AM, (D) reading out VR2 with floating AM, (E) reading out VR2 without using AM, (F) reading out vertical line reset voltage with fixed S/H, (G) reading out vertical line reset voltage with floating S/H, and (H) reading out horizontal line reset voltage.

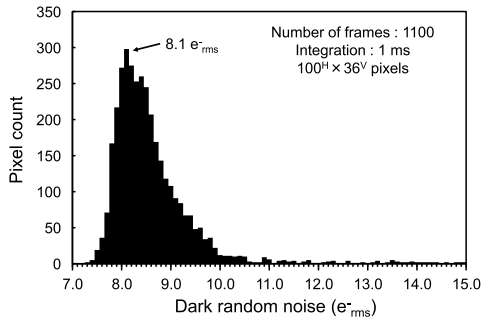

Fig. 14. Distribution of dark random noise.

random noise. The dark random noise was evaluated at the central $100^{H} \times 36^{V}$ pixels along the backside hole of the ceramic package. The mode value of dark random noise by GS operation was 8.1 e^{-}_{rms} in this work. The noise of the in-pixel AM, which is one of the main noise sources of this GS operation, was suppressed to 2.3 e^{-}_{rms} thanks to the high-density trench capacitors. The dark random noise contains, however, a temporal random noise of the measurement system which

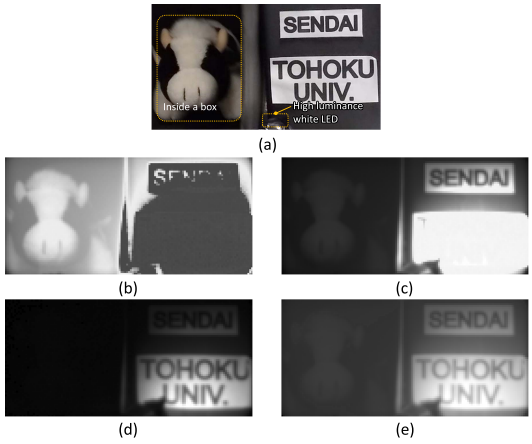

Fig. 15. (a) Image shooting samples, and sample images by (b) high sensitivity S1 signal, (c) high saturation S2 signal, (d) highest saturation S3 signal captured at 125 frames/s with F# 1.4 lens, and (e) synthesized WDR image of S1 + S2 + S3, $\gamma = 0.2$.

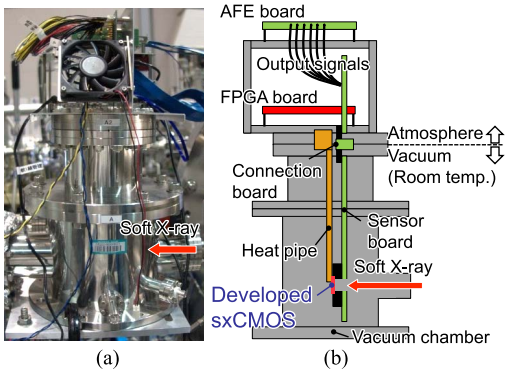

Fig. 16. (a) Photograph and (b) cross-sectional diagram of the soft X-ray measurement system.

was about 5.1 e^{-}_{rms}. This resulted in the total signal readout noise of about 5.8 e^{-}_{rms}. The PD dark current shot noise and charge transfer noise were 5.6 e^{-}_{rms} in total. The dark random noise can be further suppressed by optimizing measurement system as well as the PD and transfer gate structures, and increasing analog signal gain toward the photon counting for 100 eV soft X-ray.

Fig. 15 shows the sample images of a stuffed animal inside a dark box and printed papers with a high luminance visible light captured at 125 frames/s with F# 1.4 lens. Fig. 15(a) was the image shooting samples captured by another camera without turning on the light source. Fig. 15(b)–(d) was captured by the S1, S2, and S3 signals while the high luminance light was turned on, respectively. The sample images were cropped to $133^{H} \times 63^{V}$ pixels according to the backside hole of the ceramic package. Fig. 15(e) is synthesized of S1, S2, and S3 signals with a gamma value of 0.2. The results show that the developed sxCMOS with BSI pinned PD exhibits a single exposure WDR performance by GS operation.

Fig. 16 shows the soft X-ray measurement system. The measurements were conducted at the BL-10 beamline of the NewSUBARU synchrotron facility [29]. Here, Fig. 16(a) and (b) is the photograph and the cross-sectional

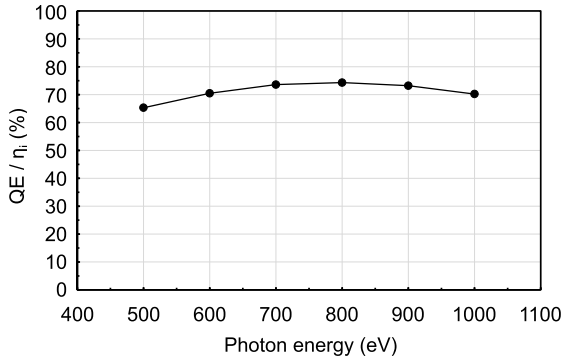

Fig. 17. Measured QE characteristics normalized by quantum yield in the soft X-ray region.

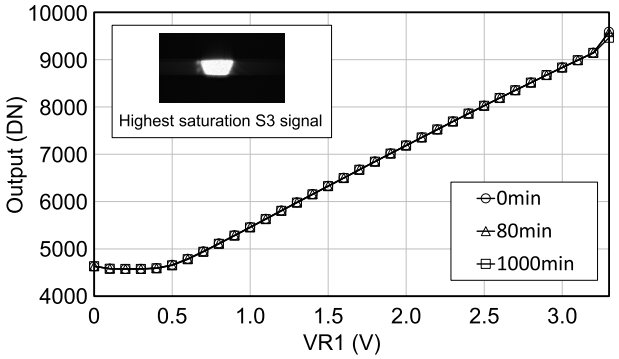

Fig. 18. Voltage readout characteristics before and after soft X-ray (1 keV) irradiation, and the S3 signal image during irradiation.

diagram of the soft X-ray measurement system, respectively. The developed sxCMOS was installed in the vacuum chamber using a sensor board and a connection board with a heat pipe to release the heat generated by the chip. The analog front-end (AFE) board and field-programmable gate array (FPGA) board were placed in the atmosphere.

Fig. 17 shows the measured QE normalized by quantum yield in the soft X-ray region, 500–1000 eV. The measurement was carried out under room temperature. The integration time was 20 ms, where the S1 signal was nearly saturated and the S2 signal was not saturated. QE is defined as the following equation [30]:

$$\mathrm{QE} = \eta_i \cdot \mathrm{QE_I} \cdot \mathrm{CCE}. \tag{1}$$

Here, CCE, charge collection efficiency is the ratio of signal photoelectrons to generated photoelectrons, maximum 1. $\mathrm{QE_I}$, interacting QE is number of interacting photons per incident photons, maximum 1. η_i, quantum yield gain defined as (2) is number of electron–hole pairs generated by an interacting photon, can be over 1

$$\eta_i = \frac{E_{\mathrm{photon}}}{E_{\mathrm{e-h}}}. \tag{2}$$

Here, E_{photon} is the energy of an incident photon, $E_{\mathrm{e-h}}$ is the energy required to generate an electron–hole pair, which for Si is approximately 3.65 eV/e^- at room temperature valid only for $E_{\mathrm{photon}} > 10$ eV. The measured characteristics in Fig. 15 was QE normalized by the quantum yield, thus the maximum is unity. The measured QE/η_i was over 70% in 600–1000 eV region. Optimization of the backside p^+ layer and back-bias in the next prototype development is expected to further improve QE.

Fig. 18 shows the measured voltage readout characteristics before and after soft X-ray irradiation and the image captured by the S3 signal during soft X-ray accelerated irradiation stress test. The measurements were conducted at the BL17SU at SPring-8 [31]. The purpose of this measurement is to confirm the transistor characteristics before and after 1 keV soft X-ray irradiation of 3.0×10^{15} photons/mm^2, which was set as the target irradiation dose for use in synchrotron radiation facilities. The beam size was about 0.42 mm × 0.37 mm. The time to reach 3.0×10^{15} photons/mm^2 is 108 min. The voltage

TABLE II
PERFORMANCE SUMMARY OF THE DEVELOPED SXCMOS

Process technology		0.18 μm 1-poly-Si 5-Metal CMOS with pinned PD
Power supply voltage		3.3 V
Die size		4.8 mm^H×4.8 mm^V
# of effective pixels		160^H×88^V
Pixel size		22.4 μm^H×22.4 μm^V
Fill factor		100 %
Shutter type		Global shutter
Standard frame rate		450 fps @ 20 MHz
Conversion gain of S1 signal		100 μV/e^-
Conversion gain of S2 signal		2.5 μV/e^-
Conversion gain of S3 signal		68 nV/e^-
Full well capacity	High sensitivity S1	10.3 ke^- (20.6 e^-/μm^2)
	High saturation S2	602 ke^- (1.20 ke^-/μm^2)
	Highest saturation S3	21.9 Me^- (43.6 ke^-/μm^2)
Dark random noise (S1 signal)		8.1 e^-_{rms}
Maximum SNR (S3 signal)		65.9 dB
Dynamic range		129 dB

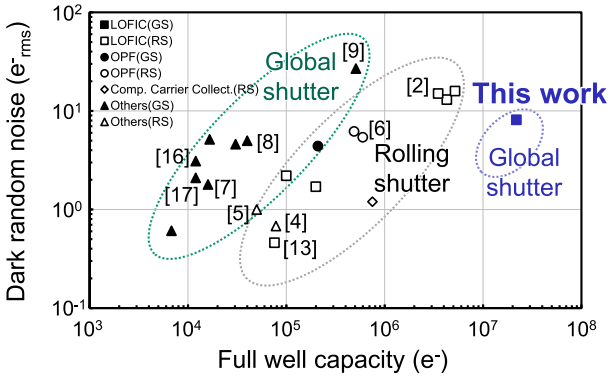

Fig. 19. Comparison of FWC and dark random noise of previously reported various CIS and this work.

transfer characteristics of the signal path were measured by reading out signal while changing VR1. The results show that the change of voltage transfer characteristics in the signal readout chain before (0 min) and after the irradiation up to 1000 min was negligible. This indicates that the transistor characteristics did not degrade for the irradiation condition in this experiment. It has been confirmed that the 45-μm thick Si substrate leads to a high radiation hardness toward

soft X-ray and enables stable measurements at synchrotron radiation facilities.

Table II shows the chip performance summary. A 1000 frames/s operation is to be available at 40 MHz pipeline operation mode with parallel signal outputs.

Fig. 19 shows the relationship of FWC and dark random noise with other linear response rolling shutter (RS) and GS CIS. A dark random noise of 8.1 e^-_{rms} with 21.9 Me^- FWC was successfully achieved in this work by GS operation.

IV. Conclusion

A 22.4-μm pixel pitch GS sxCMOS with BSI pinned PD, two-stage LOFIC, and voltage domain memory bank was developed and its performance was characterized by the fabricated prototype chip. The developed prototype chip successfully demonstrated a high QE toward soft X-ray with a single exposure 129 dB dynamic range by GS operation. This development is a step forward toward a 4 M pixel detector system for next-generation synchrotron radiation facilities and X-ray free-electron lasers.

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