Direct White Noise Characterization of Short-Channel MOSFETs

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***Abstract*— On-wafer evaluation of white thermal and shot noise in nanoscale MOSFETs is demonstrated by directly sensing the drain current under zero- and nonzero-drain-bias (V_d) conditions for the first time, without recourse to a hot noise source, commonly needed in noise figure measurement. The dependence of white noise intensity on the drain bias clearly shows thermal noise at $V_d = 0$ V and shot noise at $V_d > 0$ V with its gate-bias-dependent suppression. An empirical expression for the Fano factor (shot-noise suppression factor) that is well-behaved even at $V_d = 0$ V exactly and suitable for measurement-based evaluation is proposed. The direct measurement approach could allow more accurate and predictive noise modeling of RF MOSFETs than has conventionally been possible.**

***Index Terms*— 1/f noise, device modeling, MOSFET, shot noise, thermal noise.**

I. Introduction

MOSFETs are known to exhibit flicker (or $1/f$) noise at low frequencies (LFs) and white noise at high frequencies (HFs). Physical origins of flicker noise and white noise differ, and therefore, their power spectral densities are independent of each other. White noise can be further classified into thermal noise and shot noise, among others. Unlike the relationship between flicker noise and white noise, thermal noise and shot noise are not completely independent of each other [1]–[5].

The physics of noise in deep-submicrometer MOSFETs is much more involved than that in long-channel MOSFETs [6]–[11]. HF noise critically affects the operation of very wideband RF circuits, especially millimeter-wave circuits, because the noise integrated over a wide bandwidth contributes to the signal-to-noise ratio (SNR) of a wireless system. Recently, adverse effects of white noise from a local oscillator on wideband millimeter-wave circuits have experimentally been confirmed [12], [13]. Of course, the phase noise of oscillators and frequency synthesizers below the white noise region, too, has always been and will increasingly be a concern in RF circuit design [14]. Accurate noise measurements of transistors over a wide frequency range, including the white noise region and the transition region to that region, therefore, are essential not only for elucidating the physics behind but also for developing predictive device noise models for circuit design. Models built only from extrapolated data may well necessitate more silicon respins.

White noise in MOSFETs is typically characterized by noise figure (NF) measurement at RF, where flicker noise is negligible. In the Y-factor method of NF measurement, a known good "hot" white noise source is required to provide two ["hot" and "cold" (room temperature)] reference noise temperatures [15], [16]. The hot or cold white noise is impressed to the device under test (DUT) during the measurement. The method is typically applicable down to 10 MHz at best and usually requires a complicated de-embedding procedure, which adds to measurement uncertainty. LF (flicker) noise measurement, on the other hand, is performed by directly sensing noise generated by the DUT under "cold" dc-biased conditions. Several systems for LF noise measurement are commercially available. Although a typical maximum measurement frequency is a few tens of megahertz in product specifications, in practice, frequency roll-off due to parasitic capacitance tends to make the maximum measurable frequency considerably lower, often below 1 MHz. Noise measurement around the megahertz range is not very well covered by either method. Since typical MOSFET noise spectra become white only above 1 MHz or higher, it is difficult to apply commercial LF noise measurement systems to white-noise measurement.

There have, nevertheless, been some reports on "cold" direct noise measurement of discrete MOSFETs over frequencies ranging from flicker noise region to white noise region [17], [18]. We also chose a "cold" dc-biased approach for direct on-wafer device noise measurement. A proof-of-concept *noise probe* that extended the maximum measurable frequency to above 100 MHz was demonstrated in [19] and [20]. It has a broadband low-noise amplifier (LNA) built in the probe itself, thereby reducing the parasitic capacitance significantly. At present, an improved version of the noise probe is commercially available [21]. Measurements can be conducted even at and near zero drain bias ($V_d = 0$ V), which is not always straightforward by other means of measurement.

II. Measurements

In this study, we demonstrate the measurement of MOSFET white noise by utilizing a noise probe, shown in Fig. 1(a). Fig. 1(b) shows a schematic of the measurement system. The

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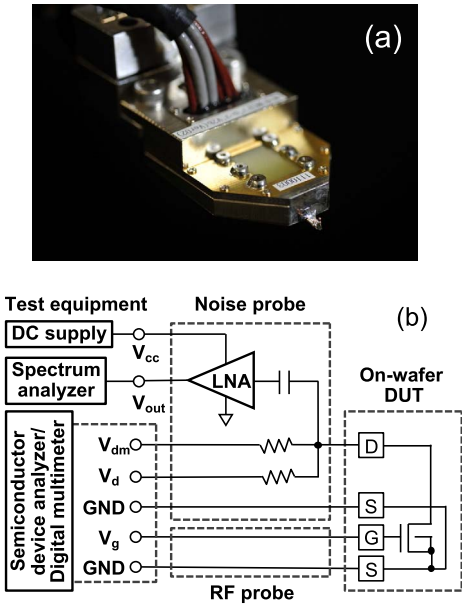

Fig. 1. (a) Photograph of a noise probe. An LNA is located inside the probe. (b) Schematic of the measurement system. V_{dm} is for monitoring the drain voltage.

ac-component (i.e., noise) of dc drain current is amplified by the LNA in the noise probe and its output is read by a spectrum analyzer (N9030A, Agilent Technologies). Each individual noise probe is calibrated by extensive measurements, and that information is stored in a postprocessing software program [21]. It calculates the drain current noise from raw power spectrum reading by the spectrum analyzer, accounting for the noise generated by the LNA. The noise generated by the spectrum analyzer itself is accounted for, in effect, by turning on its Noise Floor Extension option [22]. Measurement results at LFs (<100 kHz), where commercial LF measurement solutions work reliably, correlate well with results from such a system (9812D, ProPlus Design Solutions). In all measurements presented in the following, we employed a semiconductor device analyzer (B1500A, Agilent Technologies), equipped with four high-resolution source-measure units (HR-SMUs), for biasing DUTs. Custom-built low-pass filters were used to filter out noise from the HR-SMUs.

We characterized nMOSFETs with gate length/width of 120 nm/10 μm, which were fabricated by using 0.13-μm CMOS technology. Each DUT has two sets of ground-signal-ground (GSG) pads: one connected to the drain and the source, and the other connected to the gate and the source. The gate was biased through an RF probe and the drain was biased through and probed by the noise probe. All measurements were conducted at room temperature between 24 °C and 26 °C.

III. Results and Discussion

Fig. 2 shows $I_d - V_d$ curves of an nMOSFET at gate voltages, V_g, of 0.5, 0.6, 0.7, and 0.8 V. The symbols on the curves represent bias points where noise measurements were carried out. The drain current increases even in the saturation region owing to the short channel length ($L = 120$ nm). The threshold voltage estimated from an $I_d - V_g$ curve (not shown) at V_d of 30 mV is 0.44 V. Fig. 3(a) shows drain-current noise power

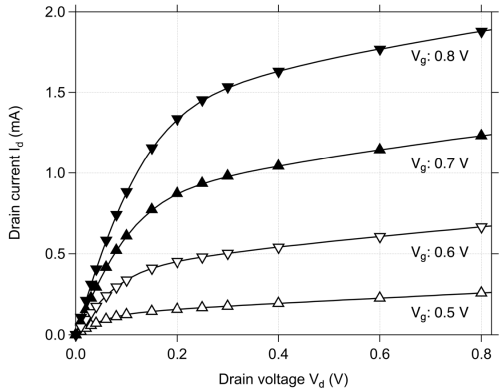

Fig. 2. Measured $I_d - V_d$ curves of an nMOSFET with gate length/width of 120 nm/10 μm. The triangular symbols indicate bias points at which noise measurements were made.

spectral density, S_{Id}, for $V_d = 0$ V. The spiky peaks observed in the frequency range from 20 to 400 kHz were induced by gate biasing. The white noise seen above 1 MHz can be regarded as thermal noise associated with the differential resistance $R_{\mathrm{dif}} = \partial V_d / \partial I_d$ [23]. As V_g increases, R_{dif} decreases, resulting in higher white noise levels. We extracted S_{Id} values at 500 MHz and compared them with theoretical values in Fig. 3(b). The horizontal axis is the theoretical thermal current noise spectral density $S_{\mathrm{th}} = 4k_{\mathrm{B}}T/R_{\mathrm{dif}}$ at $V_d = 0$ V, where k_{B} and T are the Boltzmann's constant and the DUT absolute temperature, respectively. A very good agreement was obtained from 7×10^{-24} to 2×10^{-22} A^2/Hz, corresponding to R_{dif} values from 1670 to 83.5 Ω, respectively.

When a nonzero V_d is applied, a dc drain current flows. Fig. 4(a) shows the S_{Id} spectra of six MOSFETs with the same dimensions under the same bias condition ($V_d = 0.2$ V, $V_g = 0.7$ V). Flicker noise is considered to result from a large number of traps located near the channel [5]. Each trap exhibits a Lorentzian power spectrum with a certain time constant, also known as the burst noise [23]. In nanoscale MOSFETs, the number of traps in a device is small and some Lorentzian components become visible as in Fig. 4(a) [24], [25]. Such outlying components manifest themselves in the time domain as random telegraph noise (RTN). By measuring many devices in the time domain and analyzing the results statistically, further information could be obtained about traps near the channel [26], [27]. Studies on RTN have generally been performed in an LF region due to measurement limitations. Since the raw output from the noise probe is a time-domain waveform, the use of a real-time oscilloscope in place of a spectrum analyzer [Fig. 1(b)] will allow us to observe RTN beyond 1 MHz. In this study, we focus on the frequency-domain evaluation of white noise. Note that Lorentzian components below 10 MHz do not usually affect the shape of $S_{\mathrm{Id}}(f)$ above 100 MHz because each of them drops with $1/f^2$. Therefore, $S_{\mathrm{Id}}(f)$ above 100 MHz can be regarded as the sum of white noise and residual flicker noise. The noise spectral density above 100 MHz can, therefore, be approximated as

$$S_{\mathrm{Id}}(f) = A/f^{\beta} + S_w \tag{1}$$

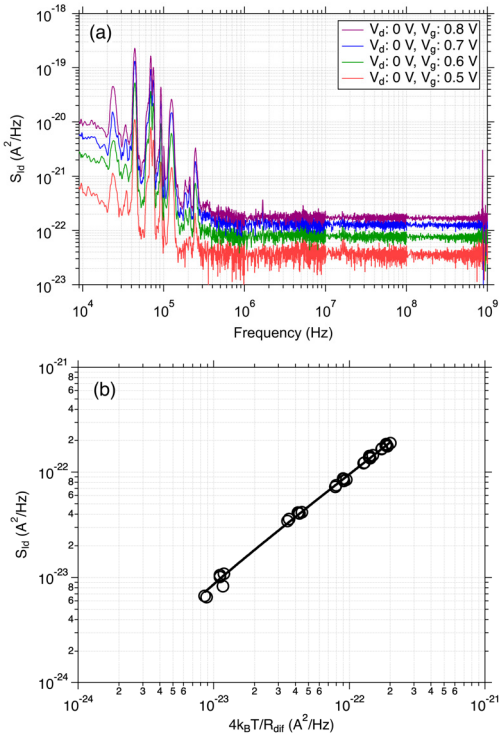

Fig. 3. (a) Drain current noise spectral density S_{Id} for $V_g = 0.5, 0.6, 0.7$, and 0.8 V and $V_d = 0$ V. (b) Measured S_{Id} at 500 MHz versus theoretical thermal noise $S_{th} = 4k_BT/R_{dif}$. S_{Id} values from six DUTs are plotted.

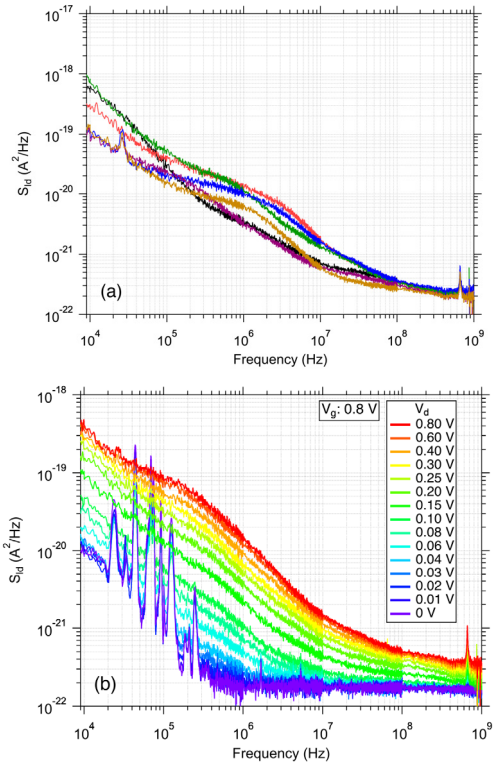

Fig. 4. (a) Variability of noise spectral densities of six DUTs over a frequency range from 9 kHz to 1 GHz. The bias condition was $V_d = 0.2$ V and $V_g = 0.7$ V. (b) Noise spectral densities for $V_g = 0.8$ V and V_d ranging from 0 to 0.8 V.

where $-\beta(\approx -1)$ is the slope of flicker noise power spectrum on a log–log plot, S_w is the white noise level, and $(A/S_w)^{1/\beta}$ is the corner frequency (onset frequency of the white noise region).

Fig. 4(b) shows $S_{Id}(f)$ at $V_g = 0.8$ V with V_d ranging from 0 to 0.8 V. It clearly shows that predominant noise changes from flicker noise $(1/f^{\beta})$ to white noise $(1/f^0)$ as the frequency becomes higher. As V_d becomes larger, flicker noise power increases, resulting in a higher corner frequency. Although the slope of $S_{Id}(f)$ becomes very small at HFs (>100 MHz), the slope for large V_d values is not quite zero. Note that the absolute value of the slope of (1) above the corner frequency is smaller than $\beta(\approx 1)$.

Fig. 5 shows the dependences of S_{Id} on V_d and V_g. Open circles and diamonds show measured S_{Id} at 300 and 500 MHz, respectively. As seen in Fig. 4(b), these values are nearly the same in the low-V_d region ($V_d < 0.1$ V). Meanwhile, as V_d increases, S_{Id} at 500 MHz becomes lower than that at 300 MHz due to higher levels of residual flicker noise [Fig. 4(b)]. The solid squares in Fig. 5 show estimated white noise S_w, calculated by using (1) with $\beta = 1$ and measured values of S_{Id} at 300 and 500 MHz, from which A, too, can be determined. Using measured $I_d - V_d$ curves (Fig. 2), we calculated the full shot noise intensity, $2qI_d$, shown by the thick solid (orange) lines in Fig. 5. Theoretical V_d-dependent thermal noise intensity is shown in Fig. 5 by the dashed (green) lines, given by [23], [28]

$$S_{th} = \frac{4k_BTR_{ch}(V_d)}{[R_{dif}(V_d)]^2} \tag{2}$$

where $R_{ch}(V_d) = V_d/I_d$ is the chord resistance [29]. Note that $R_{ch}(V_d) \neq R_{dif}(V_d)$ unless $V_d = 0$ V. Note also that we used (2) instead of the better-known integral expression [10], [23], because the latter requires more *a priori* knowledge about the DUT, making its purely measurement-based evaluation difficult.

The S_w values at $V_d = 0$ V, shown in Fig. 5, agree well with S_{th}, consistent with Fig. 3(b). Given the fact that experimentally observed shot noise is usually lower than the full shot noise [30], S_w should lie somewhere between S_{th} and $S_{th} + 2qI_d$. The latter is shown in Fig. 5 by the dot-dashed (blue) lines. As V_d increases, S_w increases similar to $2qI_d$. The V_d value at the point of intersection of $2qI_d$ and S_{th} could be regarded as the onset point of shot noise dominance. Notably, S_w of Fig. 5(a) ($V_g = 0.5$ V, moderate inversion), assumes a minimum value at $V_d \approx 0.04$ V. Although the difference between the observed minimum and the S_w value at $V_d = 0$ V is small, most of our DUTs showed similar behavior at $V_g \lesssim 0.5$ V. It is known that, in *weak inversion* of a *long-channel* device, the following white noise power expression (3) can be derived whether assuming a thermal noise origin or a shot noise origin [4], [5]

$$S_{w,wi} = 2qI_{sat}\left(1 + e^{-qV_d/k_BT}\right) \tag{3}$$

where I_{sat} is the saturation current corresponding to the given gate voltage. Equation (3) implies that at $V_d = 0$ V, $S_{w,wi} = 4qI_{sat} = S_{th}$. Although our devices are short-channel and we have no weak-inversion data because of the limited device

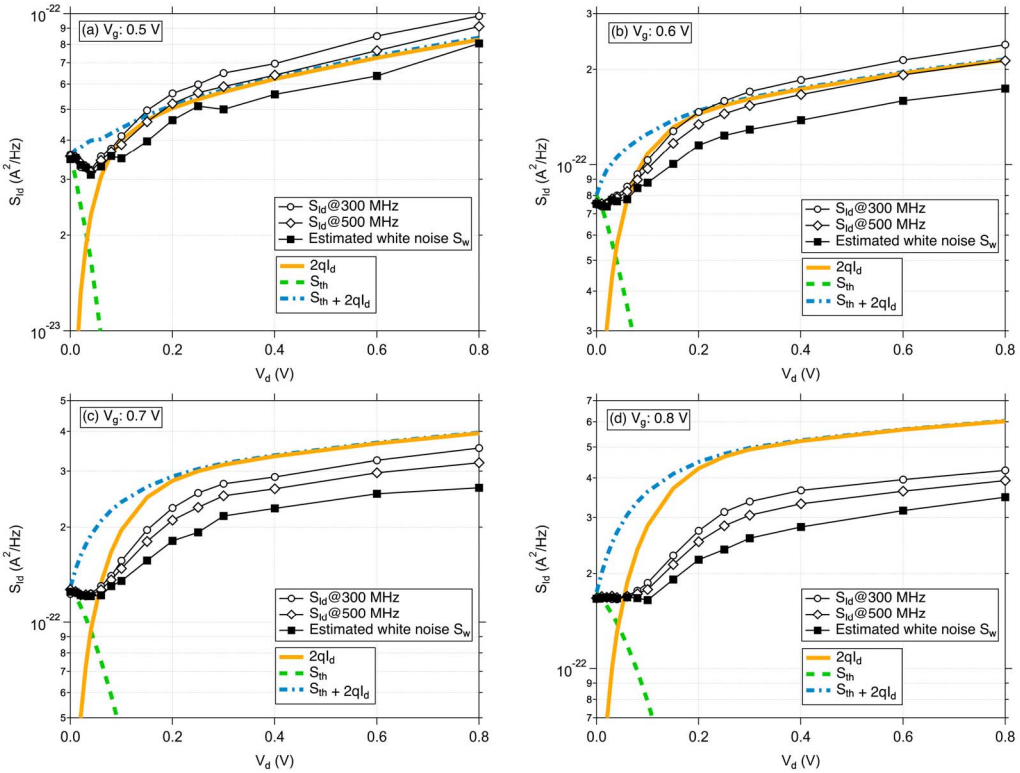

Fig. 5. Dependence of noise power spectral density on V_d for V_g of (a) 0.5 V, (b) 0.6 V, (c) 0.7 V, and (d) 0.8 V. Open circles and diamonds show measured S_{Id} at 300 and 500 MHz, respectively. Solid squares show estimated white noise S_w. Solid (orange) lines show full shot noise $2qI_d$. Dashed (green) lines show theoretical thermal noise $S_{th} = 4k_B TR_{ch}(V_d)/[\,R_{dif}(V_d)]^2$. Dot-dashed (blue) lines show the sum $2qI_d + S_{th}$.

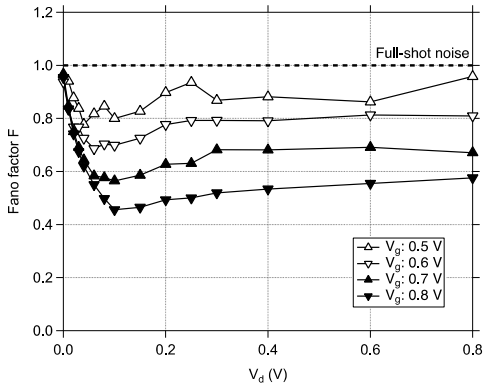

Fig. 6. Fano factor F versus drain voltage V_d for $V_g = 0.5, 0.6, 0.7$, and 0.8 V.

width of $W = 10\mu$m, the observed minimum in S_w at $V_d \approx 0.04$ V could be related to the second term of (3), originating from electrons flowing in the reverse direction (from drain to source). Theoretically expected decrease in S_w (versus V_d) in strong inversion due to channel pinch-off [5] is not clearly observed in Fig. 5(d).

Fano [31] considered a theoretical limit for the statistical fluctuation in the number of traveling particles. The full shot noise corresponds to the situation where statistical fluctuation is maximized. The so-called Fano factor $F(\leq 1)$ [32] is a coefficient for shot noise suppression and is defined as the ratio of the actual shot noise power to the full shot noise power $2qI_d$. F has successfully been employed for describing white noise of nanoscale MOSFETs when V_d is sufficiently high [30]. However, the conventional expression, $F = S_{Id}/[2qI_d \coth(V_d/2k_BT)]$ [30], is not suitable for the measurement-based evaluation of F near $V_d = 0$ V. To find an expression suitable for measurement-based evaluation, it should be defined such that it equals unity at $V_d = 0$ V in weak inversion, considering (3), which includes shot noise contributions from currents flowing in both directions [4], and Fig. 3(b). We herein introduce an empirical expression for the Fano factor F that exhibits the desired behavior, as follows:

$$F = \frac{S_w}{2qI_d + S_{th}} \tag{4}$$

where I_d is the measured drain current, S_{th} is given by (2), and S_w is the measured (estimated) white noise. The denominator of (4) corresponds to the dot-dashed (blue) lines in Fig. 5. The S_{th} in the denominator makes up for the "lost" full shot noise when V_d is below a few times the thermal voltage, $(k_BT/q) \approx 0.026$ V.

Fig. 6 shows the suppression factor F as a function of V_d for $V_g = 0.5, 0.6, 0.7$, and 0.8 V. F decreases as V_g increases presumably due to the reduction of the potential barrier near the source [33]. Shot noise is generally considered to be generated primarily due to the presence of this potential barrier, although quasi-ballistic transport in the pinched-off region near the drain may also play a role in short-channel devices. More precise discussions will require physical modeling and simulation including quasi-ballistic transport and Coulomb interaction [6], [34].

IV. Conclusion

In summary, we have developed a methodology for conveniently characterizing white noise of dc-biased nanoscale MOSFETs through wafer probing without a hot noise source or complicated de-embedding procedures. Using the approach developed, we have successfully measured white noise in short-channel MOSFETs under various bias conditions, including $V_d = 0$ V. We also proposed an empirical expression for the Fano factor (shot-noise suppression factor) F, which is well-behaved at $V_d \to 0$ V and suitable for purely measurement-based, modeling-free evaluation.

In general, various factors such as device structures and dimensions, impurity profiles, and choice of materials should affect F and other properties. Therefore, the actual measurement of devices will be important for the understanding of device properties and physics.

Note also that in circuits like a FET resistive mixer, which boasts the best low-noise performance among FET mixers [35], FETs are used under a zero-drain-bias condition. Accurate noise modeling, including near $V_d = 0$ V, therefore, is very important. The actual measurement of white noise will be essential for developing a predictive transistor noise model valid in all regions of operation. The direct measurement approach could be a perfect complement to NF measurement and device modeling based on the latter measurement method [36].

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