1.2-kV Vertical GaN Fin-JFETs: High-Temperature Characteristics and Avalanche Capability

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***Abstract*— This work describes the high-temperature performance and avalanche capability of normally-OFF 1.2-kV-class vertical gallium nitride (GaN) fin-channel junction field-effect transistors (Fin-JFETs). The GaN Fin-JFETs were fabricated by NexGen Power Systems, Inc. on 100-mm GaN-on-GaN wafers. The threshold voltage (V_{TH}) is over 2 V with less than 0.15 V shift from 25 °C to 200 °C. The specific ON-resistance (R_{ON}) increases from 0.82 at 25 °C to 1.8 mΩ·cm^2 at 200 °C. The thermal stability of V_{TH} and R_{ON} are superior to the values reported in SiC MOSFETs and JFETs. At 200 °C, the gate leakage and drain leakage currents remain below 100 μA at −7-V gate bias and 1200-V drain bias, respectively. The gate leakage current mechanism is consistent with carrier hopping across the lateral p-n junction. The high-bias drain leakage current can be well described by the Poole–Frenkel (PF) emission model. An avalanche breakdown voltage (BV_{AVA}) with positive temperature coefficient is shown in both the quasi-static *I–V* sweep and the unclamped inductive switching (UIS) tests. The UIS tests also reveal a BV_{AVA} over 1700 V and a critical avalanche energy (E_{AVA}) of 7.44 J/cm^2, with the E_{AVA} comparable to that of state-of-the-art SiC MOSFETs. These results show the great potentials of vertical GaN Fin-JFETs for medium-voltage power electronics applications.**

***Index Terms*— Avalanche, breakdown voltage (*BV*), FinFET, gallium nitride (GaN), high temperature, JFET, power devices, robustness.**

I. Introduction

GALLIUM nitride (GaN) is becoming a mainstream power semiconductor material. Recently, GaN high-electron-mobility transistors (HEMTs) have been commercialized up to the 600/650-V voltage classes [1]. Compared with the lateral GaN HEMT, vertical GaN devices have several potential advantages: 1) higher breakdown voltage (*BV*) and current capability for a given chip area, 2) superior reliability due to the reduced electric field (*E*-field) crowding near the device surface, 3) improved thermal management [2], 4) reduced dynamic on-resistance changes due to less reliance on surface passivation, and 5) reduced defect density in the GaN-on-GaN homoepitaxial layers. These advantages made vertical GaN devices particularly promising for medium-voltage (600–10 kV) and high-power applications. Until now, several 1.2-kV-class vertical GaN transistors have been demonstrated on GaN substrates, such as current-aperture vertical electron transistors (CAVETs) [3], [4], trench MOSFETs [5]–[7], and fin-channel MOSFETs [8], [9].

Another key promise that vertical GaN devices hold is the avalanche robustness, which is highly desired in many power applications such as power grid and motor drive inverters [10]. Due to the lack of a p-n junction connected between source and drain, the GaN HEMT has no or very little avalanche capability and thus requires considerable overvoltage design to handle the surge energy [10]. By contrast, avalanche capability has been widely reported in vertical GaN p-n diodes [11], [12], with an avalanche current (I_{AVA}) over 50 A and an avalanche energy (E_{AVA}) over 60 mJ [12]. However, no avalanche capability has been reported in vertical GaN transistors to date.

Recently, submicrometer, multigate fin channels have been employed in vertical GaN power transistors, which allow for high channel density, normally-OFF operation, superior gate control, and bidirectional unipolar conduction [13]. Depending on the gate structure, vertical power FinFETs have two major types: Fin-MOSFETs and Fin-JFETs [13]. Superior static and switching figure of merits (FOMs) have been demonstrated in 1.2-kV, 5-A vertical GaN Fin-MOSFETs as compared with the similarly rated SiC and Si transistors [8]. Compared with the Fin-MOSFET, it is easier to realize the avalanche capability in Fin-JFET due to the interfin p-GaN region. In addition, the Fin-JFET can avoid the potential oxide reliability issues in Fin-MOSFETs. Although a 1.2-kV GaN Fin-JFET was simulated in [14], the experimentally demonstrated devices showed

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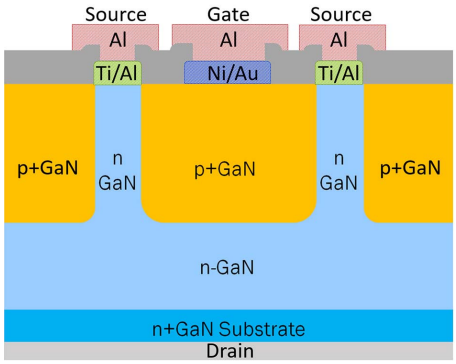

Fig. 1. Schematic cross section of the fabricated vertical GaN Fin-JFET (not to scale).

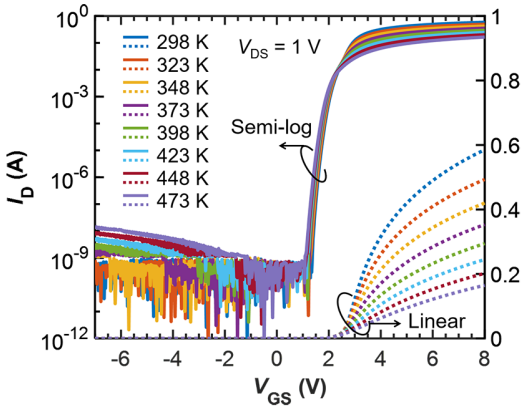

Fig. 2. Transfer characteristics in semilog scale (solid) and linear scale (dash) at 298–473 K. The ON/OFF current ratio is $\sim 10^9$. V_{TH} is 2.05 at 298 and 1.90 V at 473 K (extracted at $I_D = 1$ mA).

deficient transistor behaviors with minimal voltage-blocking capabilities and $<10^2$ current ON/OFF ratios [15], [16].

At the 2020 IEEE International Electron Devices Meeting (IEDM), we reported the first 1.2-kV-class vertical GaN Fin-JFETs [17]. The device shows $\sim 10^9$ ON/OFF ratio, a specific ON-resistance (R_{ON}) of 0.82 mΩ·cm^2, and robust avalanche capability in an unclamped inductive switching (UIS) circuit. This was the first report of avalanche capability in vertical GaN transistors. In addition, double-pulse tests at 600 V/4 A switching conditions revealed a rise/fall time of 12.9/10.3 ns with a total loss of 37 μJ, showing the superior switching performance over other vertical GaN transistors [17].

This article is an extended version of [17], focusing on the static characteristics and avalanche capability of 1.2-kV vertical GaN Fin-JFETs. Similar to [17], this article highlights the following new results: 1) a new batch of normally-OFF vertical GaN Fin-JFETs with higher threshold voltage (V_{TH}) and similar R_{ON} and BV, 2) ON-state and OFF-state characteristics at high temperatures up to 200 °C, 3) physical mechanisms of the drain leakage current and gate leakage current, and 4) critical avalanche energy obtained in the UIS failure tests. These new results allow a comprehensive comparison between 1.2-kV vertical GaN Fin-JFETs with 1.2-kV SiC MOSFETs, SiC JFETs, and Si IGBTs.

This article is organized as follows. Section II introduces the device structure and fabrication. Section III presents the temperature-dependent device characteristics, followed by the UIS test results described in Section IV. Section V benchmarks the device performance, and Section VII concludes the article.

II. Device Structure

Fig. 1 shows the schematic cross section of the vertical GaN Fin-JFETs designed and fabricated by NexGen on 100-mm GaN-on-GaN wafers at their facility in New York. The Fin-JFET consists of an array of $\sim$1-μm high n-GaN fin-shaped channels with a net donor concentration (N_D) of $\sim 10^{17}$ cm^{-3}, surrounded by the interfin p^+-GaN gate regions with a $\sim 10^{19}$-cm^{-3} metallurgical acceptor concentration. These p^+-GaN regions are commonly connected. A 10.5-μm n-GaN drift layer with a net N_D of $\sim 10^{16}$ cm^{-3} is located below the fin-channel region, grown on 100-mm bulk n^+-GaN substrates. Front-side contacts are formed using Ni/Au for the gate on p^+-GaN, Ti/Al for the source on n-GaN, with both of them routed to aluminum pads. An ohmic drain contact is formed on the backside of the substrate, and the GaN substrates are thinned before backside metallization. The JFET region is isolated using an implantation-based edge termination scheme similar to the one reported in [12]. All vertical GaN Fin-JFETs tested in this work have been packaged in the standard TO-247-4L package.

Devices with two different die sizes were characterized in this work. The device with an active region area of 0.132 mm^2 was characterized over a wide temperature range of 25 °C–200 °C (298–473 K) by quasi-static I–V sweeps on a semiconductor parameter analyzer (Keysight B1505A). A larger device with an active region area of 0.454 mm^2 was tested to failure in the UIS circuit. Note that the capacitance–voltage (C–V) characteristics and switching performance of the 0.132 mm^2 devices have been reported in [17].

III. Static Characterization

A. Output and Transfer Characteristics

Fig. 2 shows the device transfer characteristics at a drain-to-source voltage (V_{DS}) of 1 V measured at temperatures from 298 to 473 K. A normally-OFF operation within the entire measured temperature range can be clearly shown from the semilog plot, with the drain current (I_D) starting to rise from the noise floor at a gate voltage (V_{GS}) $\approx$ 1.5 V. The ON/OFF current ratio is $\sim 10^9$ at 298 K and 3×10^8 at 473 K. V_{TH} extracted at a I_D of 1 mA is 2.05 V at 298 K and shows no hysteresis. V_{TH} shows very little change (<0.15 V) at high temperatures up to 473 K. As a comparison, commercial SiC MOSFETs from various vendors show a 0.6–1 V decrease in V_{TH} from 298–373 K [18].

Fig. 3(a) shows the device output characteristics at 0 to 8 V V_{GS} at 298 K. The R_{ON} is 0.63 Ω, producing a specific R_{ON} of 0.82 mΩ·cm^2. Fig. 3(b) shows the normalized R_{ON} of the GaN Fin-JFET at 298–473 K, and its comparison to commercial SiC MOSFET [19], GaN gate injection transistor (GIT) [20], GaN Schottky-type p-GaN gate HEMT (SP-HEMT) [21], and GaN cascode HEMT [22]. Among these devices, the GaN Fin-JFET shows the smallest R_{ON} increase

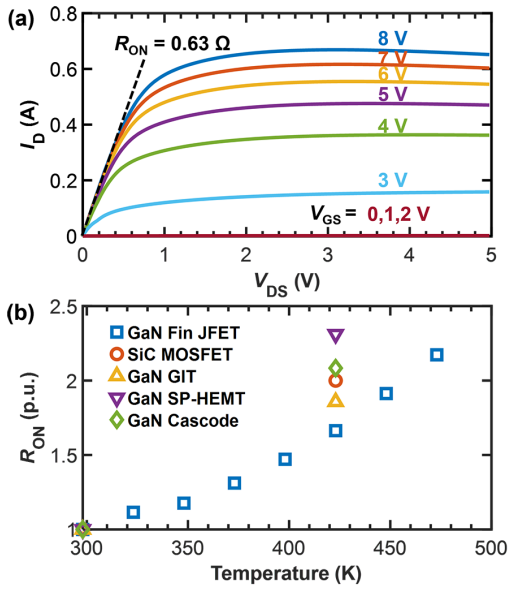

Fig. 3. (a) Output characteristics for 0–8 V V_{GS} at 298 K. (b) Normalized R_{ON} variation of the GaN Fin-JFET at 298–473 K and its comparison to commercial SiC and GaN power transistors.

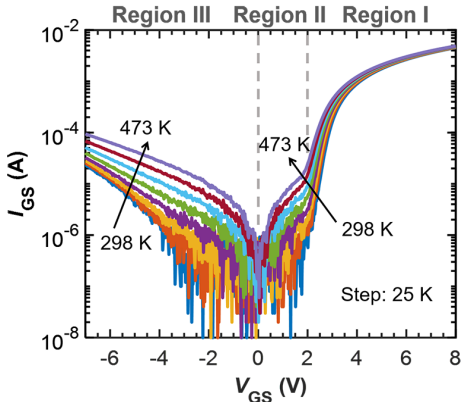

Fig. 4. I_{GS}–V_{GS} characteristics of the vertical GaN Fin-JFET at 298–473 K and the illustration of three regions.

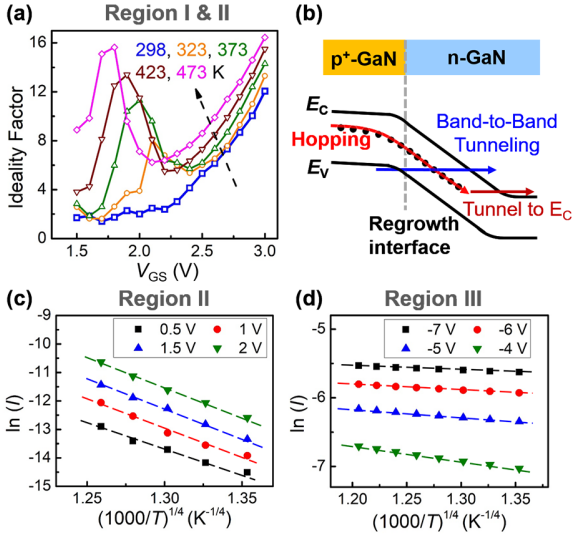

Fig. 5. (a) Ideality factor as a function of V_{GS} at 298–473 K. (b) Schematic of the hopping and band-to-band tunneling in the lateral regrown p-n junction. The ln(I) versus $(1000/T)^{0.25}$ plot and the linear fitting at (c) forward V_{GS} of 0.5–2 V and (d) reverse V_{GS} of 4–7 V.

with temperature (1.7-fold increase at 150 °C and 2.2-fold at 200 °C). The precommercial normally-OFF SiC JFETs were reported to have an even larger R_{ON} temperature dependence (3.7-fold at 200 °C) [23]. Hence, the excellent thermal stability of vertical GaN Fin-JFETs is believed to be related to both the vertical JFET structure and the high-quality GaN-on-GaN material properties.

It should be mentioned that the Fin-JFET presented in this work has a lower saturation current (I_{DSAT}) than the device in [17], whereas the two devices have a similar specific R_{ON}. This is due to the lower saturation drain voltage (V_{DSAT}) in the Fin-JFET presented in this work. In power JFETs, there is a tradeoff between V_{DSAT} and V_{TH} that V_{DSAT} decreases with the increased V_{TH} [24]. Note that power devices usually operate in the linear regime for power switching applications; hence, R_{ON} and V_{TH} are typically more critical than V_{DSAT} and I_{DSAT}.

B. Gate Leakage Current Characteristics and Mechanisms

The gate-to-source current (I_{GS}) characteristics of the GaN Fin-JFETs are direct indicators of the quality of the lateral p-n junction. Fig. 4 shows the I_{GS} versus V_{GS} characteristics measured at a temperature of 298–473 K. I_{GS} is about 5 mA at a V_{GS} of 8 V up to 473 K. The I_{GS} at the reverse V_{GS} up to −4 V has a similar level when compared to that in commercial GITs. The gate shows no degradation or failure at V_{GS} of −7–8 V, suggesting a sufficient gate drive margin.

The $I_{GS} - V_{GS}$ characteristics can be divided into three regions, i.e., high forward V_{GS} region (region I), low forward V_{GS} region (region II), and reverse V_{GS} region (region III). Fig. 5(a) shows the extracted ideality factor (η) in the regions I and II. At 25 °C, η is 1.5–2 at V_{GS} of 1.5–2.2 V, implying the current transport is partly limited by diffusion ($\eta = 1$) and recombination ($\eta = 2$). The dominance of diffusion–recombination current reflects the high quality of the lateral p-n junction. At higher temperatures, a much higher η is observed in region II due to excessive leakage current. In region I, η shows relatively small temperature dependence and increases with V_{GS}, due to the limitation of series and contact resistances [25].

The excessive leakage currents in GaN p-n junctions are often attributed to several transport mechanisms, including tunneling, hopping, and field-enhanced thermionic emission [i.e., Poole–Frenkel (PF) emission] [26]–[29]. As shown in Fig. 4, I_{GS} has a strong temperature dependence but is nearly symmetric at low forward and reverse V_{GS}, suggesting a weak field dependence (as the built-in potential varies a lot between forward and reverse V_{GS}). This behavior indicate that the low-field I_{GS} is not dominated by tunneling or PF, as both of them expect a strong field dependence, and tunneling is weakly temperature-dependent [27]. Instead, the leakage current behaviors can be explained by carrier hopping via

localized defect-related traps in the depletion region, as illustrated in Fig. 5(b). The hopping current at low E-field can be described by [26], [29]

$$I_{\text{hopping}}^{\text{low-F}} \propto I_0 \exp\left[-(T_0/T)^{\gamma}\right] \tag{1}$$

where T_0 is the characteristic temperature, and γ is a coefficient depending to hopping mechanisms, e.g., $\gamma = 0.25$ for 1-D variable-range-hopping (VRH) [26], $\gamma = 1/3$ for 2-D VRH [28], and $\gamma = 1$ for nearest-neighbor hopping (NNH) [26]. Fig. 5(c) shows a good linear relation between ln (I) and $(1000/T)^{0.25}$ at $V_{\text{GS}} = 0.5$, 1, 1.5, and 2 V (region II) with a similar slope. This linearity is also confirmed at the low reverse V_{GS} (region III). At higher reverse V_{GS}, the linearity still holds with smaller temperature dependence, as shown in Fig. 5(d). This can be explained by the hopping model at a moderate or high E-field [30]

$$I_{\text{hopping}}^{\text{high-F}} \propto I_{\text{hopping}}^{\text{low-F}} \exp[C \cdot qE/kT] \tag{2}$$

where C is a constant, k is the Boltzmann's constant, and E is the E-field. The field term in (2) has a negative temperature dependence, which compensates the positive temperature dependence of the low-field hopping current. While $\gamma = 0.25$ in Fig. 5(c) and (d), a good linearity was also observed for other γ values between 0.25 and 1, suggesting the need for scrutinizing the physical hopping types in the future work.

In previous Fin-JFET reports, a high leakage current is present in the regrown lateral GaN p-n junctions [15], [16], due to the band-to-band tunneling (BTBT) assisted by interfacial defects and impurities [27], [31] [see Fig. 5(b)]. It is worth highlighting that no BTBT leakage current is present in the GaN JFETs characterized in this work.

C. OFF-State Drain Leakage Current and BV

The voltage blocking in vertical GaN Fin-JFETs hinges on the vertical p-n junction between p^+-GaN and the n-GaN drift regions. Fig. 6(a) shows the OFF-state I–V characteristics under $V_{\text{GS}} = 0$ V and $V_{\text{GS}} = -4$ V at 298 K, showing both I_{D} and gate current (I_{G}). The identical I_{D} confirms the device's capability to block high V_{DS} at zero V_{GS}. Fig. 6(b) shows the OFF-state I_{D}–V_{DS} characteristics at 298– 473 K under $V_{\text{GS}} = 0$ V. The device shows no destructive breakdown before I_{D} reaches the measurement compliance (1 mA) at 1365 (298) and 1523 V (473 K). The positive temperature coefficient (0.89 V/K) suggests avalanche capability. At high V_{DS}, $I_{\text{D}} \approx I_{\text{G}}$, implying that the avalanche current path is mainly through the p-GaN gate.

As shown in Fig. 6, the high-bias I_{D} shows substantial temperature-and field-dependences. These dependences were found to be consistent with the PF emission model [32], which involves the field-assisted ionization of deep traps and carrier emission to the conduction band, as illustrated in Fig. 7(a). The PF current can be mathematically described as [33]

$$I_{\text{PF}} \propto E_{\text{avg}} \exp(-E_a/kT) \tag{3}$$

where E_a is the thermal activation energy, and E_{avg} is the average electric field in the depletion region, which is

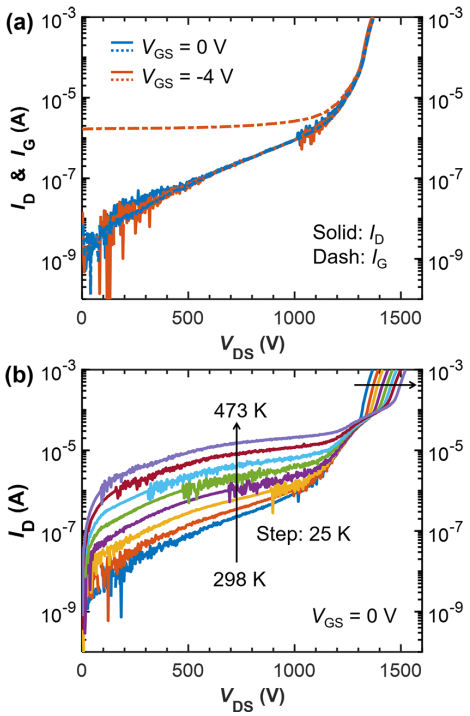

Fig. 6. (a) OFF-state I–V characteristics of the vertical GaN Fin-JFET under $V_{\text{GS}} = 0$ and $V_{\text{GS}} = -4$ V at 298 K, showing both I_{D} (solid) and I_{G} (dash). (b) OFF-state I–V characteristics at 298–473 K under $V_{\text{GS}} = 0$ V.

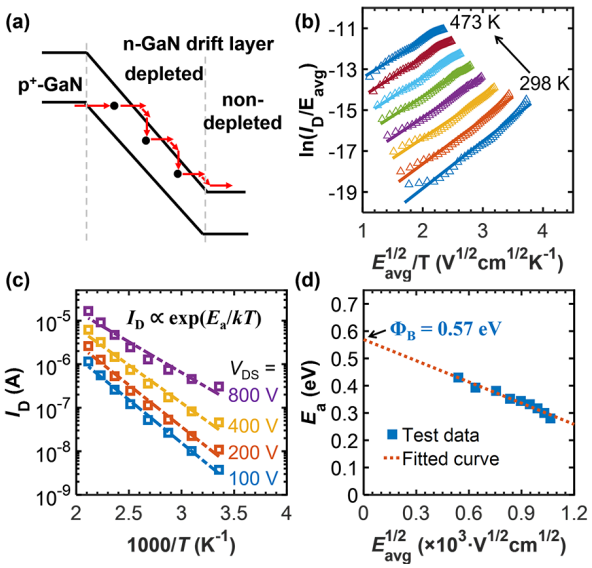

Fig. 7. (a) Schematic of the PF conduction mechanism. (b) ln(I_D/E_{avg}) versus $E_{\text{avg}}^{1/2}/T$ plot at 298–473 K. (c) Arrhenius plot of the drain leakage current measured at 100–800 V. (d) Thermal activation energy E_a as a function of $E_{\text{avg}}^{1/2}$. A 0.57 eV trap level is extracted at zero E_{avg}.

given by

$$E_{\text{avg}} = \sqrt{qN_{\text{D}}(V_{\text{bi}} + V_{\text{D}})}/2\varepsilon_{\text{S}} \tag{4}$$

where V_{bi} is the built-in voltage of the p-n junction (~3.4 V for GaN), and ε_s is the permittivity of GaN.

Fig. 7(b) shows the ln(I_D/E_{avg}) versus $E_{\text{avg}}^{1/2}/T$ plot from 298–473 K at V_{DS} from 50 to 1000 V. According to (3) and (4),

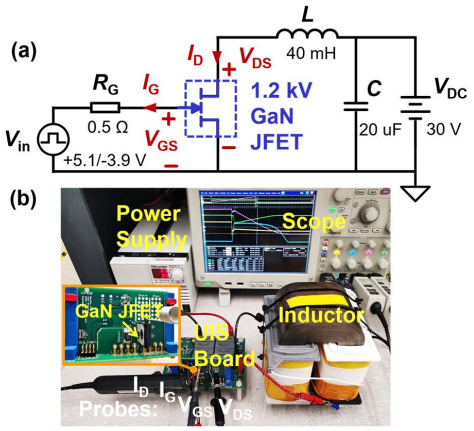

Fig. 8. (a) UIS circuit schematic and (b) photo of the setup.

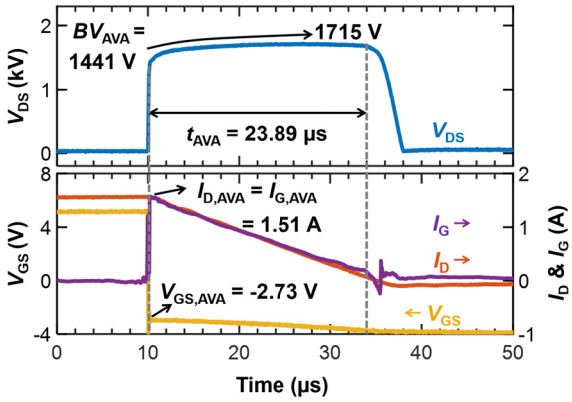

Fig. 9. Critical UIS test waveforms of the vertical GaN Fin-JFET. BV_{AVA} increases from 1441 to 1715 V, indicating the increase in T_j. Critical E_{AVA} is calculated to be 33.8 mJ (7.44 J/ cm^2).

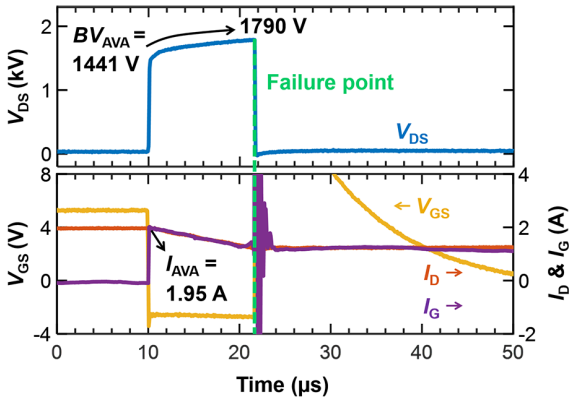

Fig. 10. Failure UIS test waveforms. The failure happened at a higher BV_{AVA} of 1790 V, suggesting that the failure is thermally induced.

the fit validates that PF is the dominant drain leakage current mechanism at high drain bias. Fig. 7(c) shows the Arrhenius plots for I_D at V_{DS} from 100 to 800 V, where the E_a within the temperature range of 298–473 K can be extracted. In the PF transport, E_a can be also expressed as

$$E_a = q\Phi_B - \beta_{PF}\sqrt{E}_{avg} \tag{5}$$

where Φ_B is the barrier height for the electron emission from the trap states without an external electric field, and β_{PF} is the PF coefficient. Fig. 7(d) shows the plot of E_a as a function of $E_{avg}^{1/2}$. A linear fitting yields a β_{PF} of 2.592×10^{-4} eV·V$^{-1/2}$·cm$^{-1/2}$, which is very close to the theoretical value (2.5×10^{-4} eV·V$^{-1/2}$·cm$^{-1/2}$ [33]) of the GaN material. A 0.57 eV trap level is obtained at the zero E_{avg} intercept [see Fig. 7(d)], implying that the dominant trap for the PF transport is likely the $E_C-0.6$ eV electron trap widely reported in the GaN epitaxial layers on GaN substrates grown by the metal–organic chemical vapor deposition (MOCVD) [34]–[36], which may originate from the residual carbon atoms [34], point defects [35], or nitrogen antisites [36].

IV. UIS Test

To validate and evaluate the avalanche capability, the device was characterized in the UIS test (a JEDEC industrial standard [37]). In the UIS test, an inductive load forces a high I_{AVA} into the device at its BV_{AVA}, with the inductive load energy dissipated in the device through avalanching.

A customized UIS test setup, as shown in Fig. 8, was built based on our prior work on GaN HEMTs [10]. The device under test (DUT) was in series with an inductor (L) and was initially turned on for a certain time duration to build up a linear current. The DUT was then switched off, forcing the inductor energy into the DUT, hence, driving it into avalanche. During the test, the turn-on duration was stepped up to increase the avalanche current and energy applied on the DUT. After each UIS test, the device was measured on the curve tracer to identify any possible degradation. Standard MOSFET driver IC Si8271GB-IS was used with the input gate voltage (V_{in}) of +5.1/−3.9 V. A 0.5-Ω external gate resistor (R_G) and 40-mH inductor were used. The dc bus voltage (V_{DC}) was 30 V. V_{DS}, I_D, and V_{GS} were measured by probes, and I_G was calculated by measuring the voltage across R_G.

Fig. 9 shows the test waveforms of the last UIS pulse before failure of the vertical GaN Fin-JFETs. After V_{DS} reaches BV_{AVA}, a textbook-like avalanche waveform is shown, where V_{DS} first clamps at a BV_{AVA} of 1441 V and increases to 1715 V. The increase in the BV_{AVA} indicates a dramatic junction temperature (T_j) rise during the ∼24 μs avalanche time (t_{AVA}). I_D gradually reduces to zero and resonates to the reverse direction afterward. In the avalanche process, I_G is found to follow I_D with an almost identical magnitude, verifying that the avalanche current goes through the p-GaN gate region instead of the n-GaN fin source for the value of R_G selected. When the avalanche starts, a V_{GS} rise of ∼1.2 V suggests that the internal gate resistance is ∼0.8 Ω. No permanent change in the static I–V parameters was observed before the device failure.

Fig. 10 shows the failure UIS waveforms. Under a higher inductor current and energy, V_{DS} is driven to and fails at a higher BV_{AVA} (1790 V), suggesting that the failure is thermally induced. All terminals were shorted after failure. From the failure voltage (1790 V) and the temperature coefficient of BV_{AVA} (0.89 V/K), T_j at the failure can be roughly estimated to be 503 °C (776 K).

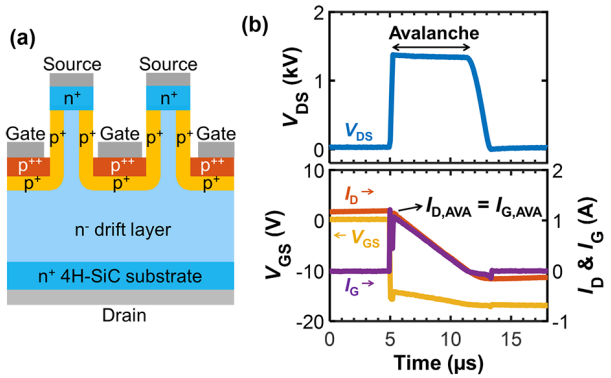

Fig. 11. (a) Schematic of the SiC normally-ON vertical JFET. (b) UIS test waveforms of the SiC JFET. Its avalanche current is also found to flow through the gate.

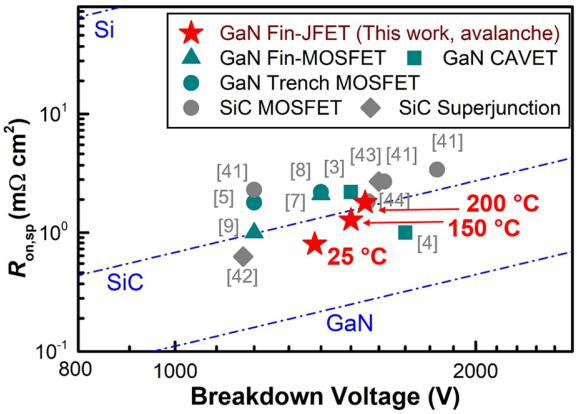

Fig. 12. Specific R_{ON} versus BV of the NexGen's vertical GaN Fin-JFET at 25 °C, 150 °C, and 200 °C, benchmarked with the state-of-the-art GaN and SiC power transistors. The data of all the benchmarked devices used in this figure are at 25 °C. The unipolar limits of Si, SiC, and GaN at 25 °C are also plotted.

By integrating the avalanche power (voltage and current) over time on Fig. 9, the critical avalanche energy (E_{AVA}) in GaN JFET is calculated to be 33.8 mJ (7.44 J/cm^2). As a thermally sensitive metric, E_{AVA} highly relies on t_{AVA} as T_j depends on the heating/cooling process. Tested at the similar t_{AVA}, state-of-the-art SiC MOSFETs showed an E_{AVA} density of 6–15 J/cm^2 [38], [39]. The comparable E_{AVA} density values in GaN FinFETs and SiC MOSFETs manifest the excellent avalanche robustness of the vertical GaN Fin-JFET.

It should be noted that the avalanche process of the vertical GaN Fin-JFET has also been studied by the TCAD device simulation with Silvaco Atlas, and the results were presented in [17]. The simulated contours of the impact ionization generation rates and hole current at BV_{AVA} validate that the avalanche happens at the gate–drain p-n junction and the avalanche current mainly flows through the gate [17].

The avalanche-through-gate phenomenon in GaN Fin-JFETs is very different from that in power MOSFETs, and it requires new considerations of the gate driving circuitry. Driver ICs, as well as other components in the gate loop, should be selected with a peak sink current higher than the Fin-JFET avalanche current. On the other hand, it should be mentioned that this avalanche behavior does not come from GaN but from the power JFET structure under this specific driving condition.

To verify the generalization of this avalanche behavior in power JFETs, a commercial 1.2-kV SiC JFET [40] was tested in the similar UIS setup. Fig. 11(a) shows the cell structure of the SiC JFET, which features a normally-ON operation with a V_{TH} of around–12 V [40]. V_{in} was then set as −18/0 V. External R_G was 2 Ω. Other circuit parameters remained the same as in the ones in Fig. 8. Fig. 11(b) shows the UIS test waveforms of the SiC JFET. During its avalanche, I_G is also found to follow I_D, indicating the avalanche-through-gate phenomenon in SiC JFET under similar driving conditions.

V. Benchmark and Discussion

Fig. 12 benchmarks the specific R_{ON} versus BV at 25–200 °C of the NexGen's vertical GaN Fin-JFETs with the state-of-the-art GaN [3]–[5], [7]–[9] and SiC [41]–[44] power transistors. The unipolar physical limits of the Si, SiC, and GaN materials at 25 °C are also plotted in the figure. Note that the BV at 1 mA I_D is used in this benchmark, whereas the vertical GaN Fin-JFET can sustain higher BV_{AVA} in the circuit applications. The vertical GaN Fin-JFETs show superior R_{ON} versus BV tradeoffs over the similarly rated SiC MOSFETs and one of the highest Baliga's FOMs (2.5 GW/cm^2) in vertical GaN power transistors. The vertical GaN Fin-JFET also shows faster switching speed, smaller switching losses, and minimal reverse recovery loss when compared with Si and SiC superjunction devices, which has been presented in [17].

Based on the experimental results, we provide comparative perspectives on vertical GaN Fin-JFETs and SiC power JFETs. The SiC JFET also utilizes a vertical n-type channel but forms the p^+-regions through ion implantation onto channel sidewalls [see Fig. 11(a)]. Both normally-OFF and normally-ON SiC JFETs have been demonstrated. However, it was later found that the narrow and implanted fin channel in normally-OFF SiC JFETs makes their R_{ON} several times higher than the normally-ON counterparts [45]. As a result, the commercially available SiC JFET is normally-ON; it is co-packaged with a Si MOSFET in a cascode configuration to realize the normally-OFF operation.

In GaN JFETs, the p-GaN regrowth allows better control of dopant diffusion when compared with ion implantation and obviates the need for ion activation at high temperatures. This inherent advantage of GaN processing favors the realization of fin channel with low ON-resistance [13] and, therefore, the high-performance of normally-OFF vertical GaN JFETs. Their high-temperature stability and avalanche ruggedness make them a preferred alternative to SiC cascode-JFETs or SiC MOSFETs, which are limited by the Si MOSFET capability and the SiC gate oxide instability, respectively, in the high-temperature applications.

VI. Conclusion

This work presents the high-temperature characteristics and avalanche capabilities of the 1.2-kV-class vertical GaN Fin-JFETs manufactured by NexGen Power Systems, Inc. on

100-mm GaN-on-GaN wafers. The device shows excellent thermal stability up to at least 200 °C, with a V_{TH} shift below 0.15 V, a merely 2.2-fold higher R_{ON}, an increased BV_{AVA}, and small gate–drain leakage currents at 200 °C. The device demonstrates one of the best Baliga's FOM in vertical GaN transistors and at least 2–3-fold lower specific R_{ON} than the best-performance 1.2-kV SiC MOSFETs in the literature. The UIS test reveals a critical E_{AVA} density similar to state-of-the-art SiC MOSFETs. These results show the great potential of vertical GaN Fin-JFETs for medium-voltage power electronics and the harsh-environment power applications.

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