Improved Model on Buried-Oxide Damage Induced by Total-Ionizing-Dose Effect for HV SOI LDMOS

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***Abstract*— In this article, an improved model on buried-oxide (BOX) damage induced by total-ionizing-dose (TID) effect considering positive oxide trapped charge (N_{ot}) generated in silicon on insulator (SOI) /BOX interface under negative electric field bias (field lines perpendicular to the SOI/BOX interface pointing from the top to the bottom of the BOX) and N_{ot} saturation effect is proposed and adopted in accurate simulated analysis to predict the postirradiation device behavior. Moreover, the mechanism of high-voltage (HV) SOI lateral double diffused metal oxide semiconductor field effect transistor (LDMOS) degradation during irradiation is also revealed by the proposed accurate simulation method. Tolerance design for radiation-hardened HV SOI LDMOS is discussed with the aid of the presented model. The tradeoff between postirradiation electrical characteristics and fresh electrical characteristics should be taken into account to meet the radiation hardening requirement. The radiation-hardened-by-design LDMOS introduced in this article keeps an OFF-state breakdown voltage above 120 V at $D = 500$ krad(Si) with operating voltage equal to 80 V, which is fabricated on a commercial SOI substrate material with plain interface quality parameters. The corresponding hardening strategy is also given.**

***Index Terms*— Buried-oxide (BOX) damage model, hardening strategy, high-voltage (HV) silicon on insulator (SOI) lateral double diffused metal oxide semiconductor field effect transistor (LDMOS), negative electric field bias, OFF-state bias, total-ionizing-dose (TID) effect.**

I. Introduction

As SPACE power electronics system grows toward smaller size and weight, higher integration level and performance are required. Because of ease to integration and fast switching, silicon on insulator (SOI) lateral double diffused metal oxide semiconductor field effect transistor (LDMOS) is an attractive option with growing attention for monolithic ICs in space radiation-hardening application [1], [2]. Total-ionizing-dose (TID) effect is one of the most common irradiation damages for semiconductor devices applied in space equipment [3]–[10]. For TID effect on low-voltage SOI MOSFET, the damage on buried-oxide (BOX) may lead to the increase of OFF-state leakage and coupling effect [11]–[13]. The degradation mechanism is ascribed to the positive oxide trapped charge (N_{ot}) induced by TID generated near the SOI/BOX interface under the positive applied field bias in the BOX (field lines perpendicular to the SOI/BOX interface pointing from the bottom to the top) [3], [6], [7], [12].

For the high electric field in the thick oxide under long drift region of high-voltage (HV) SOI LDMOS, the degradation of electrical characteristics under OFF-state bias is worthier of studying. For OFF-state bias, BOX is under negative electric field bias during irradiation (the vertical electric field lines in BOX are pointing from top to bottom), which did not draw much attention in previous reports. The traditional TID model only explains the damage well under positive electric field bias [3]. Thus, it is hard to predict the N_{ot} distribution in BOX under OFF-state bias in the postirradiation device and the traditional model for TID effect is not applicable for HV SOI LDMOS at OFF-state in the simulated analysis.

In this article, the distribution of radiation-induced N_{ot} in BOX with different applied electric fields for HV SOI LDMOS is investigated. In contrast to the traditional model which depends upon N_{ot} buildup near the interface that the field lines point to, the verified experimental results in this article indicate that there is still a nonnegligible set of N_{ot} generated in SOI/BOX interface even if the electric field plays a negative role, which is responsible for the electrical characteristic shift behavior. Then an improved model on the BOX damage induced by TID effect including the function relationship between N_{ot} in SOI/BOX interface and negative electric field is proposed, and the N_{ot} saturation effect is also considered. By tunning the improved model with the extracted interface quality parameters into TCAD code, the simulation results show a good agreement with the experimental results.

The proposed accurate simulation method in this article provides convenience for analyzing electrical characteristic shift mechanism in HV SOI LDMOS and gives an insight into tolerance design work of HV SOI LDMOS in space radiation-hardening application. The tradeoff between postirradiation electrical characteristics and fresh electrical characteristics has been taken into account. The radiation-hardened-by-design LDMOS introduced in this article can keep an OFF-state breakdown voltage (BV) above 120 V at $D = 500$ krad(Si)

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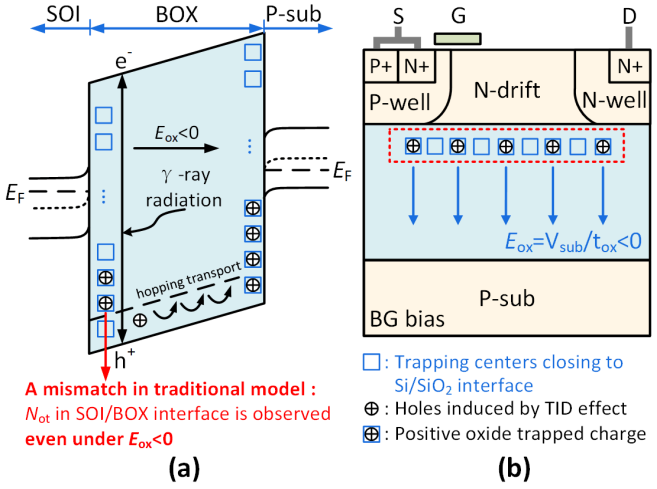

Fig. 1. Schematic of (a) TID model of HV SOI LDMOS under negative electric field bias and (b) evaluation of BOX damage induced by TID effect under negative BG bias.

with operating voltage equal to 80 V, which is fabricated on a low-cost and highly accessible commercial SOI substrate material without radiation-hardening-by-process.

II. Experiment and Mechanism

The traditional model explains TID effect well under positive field bias. Electron–hole pairs are created in oxide layer by γ-ray radiation, where the holes are attracted toward the SOI/BOX interface, then part of them are trapped by trapping centers located in the region close to the SOI/BOX interface. As described in the traditional model, N_{ot} should only be generated in the P-sub/BOX interface under negative electric field bias [negative back-gate (BG) bias and OFF-state] for HV SOI LDMOS due to that the electric field pushes holes away from SOI/BOX interface. Because of the out-diffusion of oxygen in the oxide and lattice mismatch at the Si/SiO_2 interface, there are a large number of oxygen-vacancies acting as trapping centers which are close to the interface. Thus, the trapping process in the bulk of SiO_2 layer is usually not taken into account [14], [15]. However, the verified evidence below manifests the N_{ot} is also generated in the SOI/BOX interface, because there are still a fraction of holes reaching the Si/SiO_2 interface and getting trapped even if the electric field plays a negative role [see Fig. 1(a)]. Then a more comprehensive improved model on BOX damage is proposed, which is more applicable for HV SOI LDMOS. Fig. 1(b) shows the schematic of evaluation of BOX damage induced by TID effect under negative BG bias, and then the function relationship between the uniform N_{ot} in SOI/BOX interface and negative E can be determined. Subsequently, the N_{ot} distribution is calculable for OFF-state bias condition. Interface traps (N_{it}) induced by TID are negligible in the evaluation work, due to the fact that it is much less than N_{ot} and plays a trivial role [$D < 1$ Mrad(Si)] [16].

Gate-oxide (GOX) hardened HV SOI LDMOS without thermal field-oxide (FOX) investigated in the TID experiment is fabricated on 1.2-μm BOX layer and 1.5-μm SOI layer. Due to TID insensitivity of the deposited SiO_2 [17], the device can exclude the influence of N_{ot} in the upper surface of SOI layer. Then the degradation of the device in TID experiment

TABLE I
Bias Conditions in Irradiation Experiment

Bias type	V_g (V)	V_d (V)	V_s (V)	V_{sub} (V)
off-state	0	80	0	0
back-gate bias	0	0	0	+60/+10/-10/-20/ -40/-60/-80/-100

is only related to the damage on BOX. The devices were irradiated by ^{60}Co irradiation source with 50 rad/s at room temperature and the measurement results of postirradiation electrical characteristics were obtained out of the radiation environment within 15 min. The irradiation bias conditions of OFF-state bias and BG bias are given in Table I. In this article, the OFF-state BV and the ON-state linear drain current (I_{dlin}) are defined as the drain voltage while $I_d = 1$ μA at OFF-state and the drain current while $V_{gs} = 20$ V and $V_{ds} = 0.1$ V at ON-state, respectively.

III. Improved Model on BOX Damage

Before the discussion of the designed experiment, the influence of N_{ot} in P-sub/BOX interface and SOI/BOX interface on electrical characteristics of HV SOI LDMOS should be determined. Fig. 2(a) shows the simulated electrical characteristic shift behavior with different positive fixed charges in BOX (Q_{BOX}) located in different interfaces. As the Q_{BOX} in the P-sub/BOX interface lies far from the SOI layer, it does not affect electrical characteristics of the device. For the device with Q_{BOX} in the SOI/BOX interface, the positive Q_{BOX} could cause negative mirror charges in the SOI layer with the same density at ON-state and modulate the electric field distribution at OFF-state. As a result, I_{dlin} increases and BV increases at early stage then drops with Q_{BOX} increasing. It can be inferred that only the Q_{BOX} in the SOI/BOX interface, rather than Q_{BOX} in the P-sub/BOX interface, can influence the I_{dlin} when Q_{FOX} and Q_{GOX} are excluded. Fig. 2(b) shows the measured transfer curves with different BG bias at $D =$ 10 krad(Si), indicating there is a radiation-hardened threshold voltage of 2.4 V for all curves. Based on the concept above, the increment of I_{dlin} under negative BG bias proves that N_{ot} is generated in the SOI/BOX interface.

A. Model of f_y Under Negative Electric Field Bias

Fig. 3(a) shows the measured fresh I_{dlin} with different V_{sub}. The uniform N_{ot} introduced in the SOI/BOX interface could cause mirror electrons with the same density and the BOX capacitance would reserve charges equal to $V_{sub} \cdot C_{BOX}$. Thus, the TID induced uniform N_{ot} in SOI/BOX under different BG bias can be extracted by comparing TID induced I_{dlin} shift in postirradiation device and V_{sub} induced I_{dlin} shift in the fresh device. Fig. 3(b) shows the extracted N_{ot} in SOI/BOX interface induced by TID at 1 krad(Si) with different applied electric field bias. Under positive BG bias, the values of N_{ot} fit well with the traditional model [3], as shown in

$$N_{ot} = g_0 \cdot f_{ot} \cdot f_y^+ \cdot t_{ox} \cdot D \tag{1}$$

$$f_y^+ = \left(\frac{|E_{ox}| + E_0^+}{|E_{ox}| + E_1^+} \right)^m \tag{2}$$

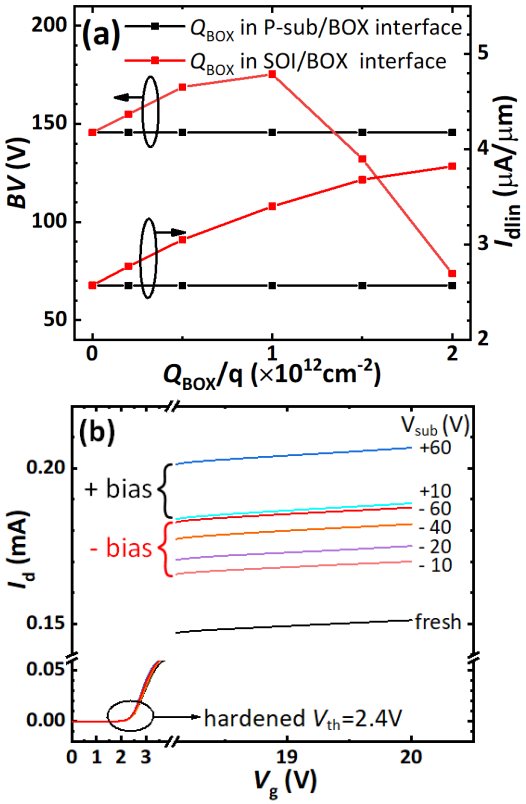

Fig. 2. (a) Simulated BV and I_{dlin} shift curves of the LDMOS with different Q_{BOX} located in different interfaces. (b) Measured transfer curves with different BG bias at $D = 10$ krad(Si) and the fresh transfer curve.

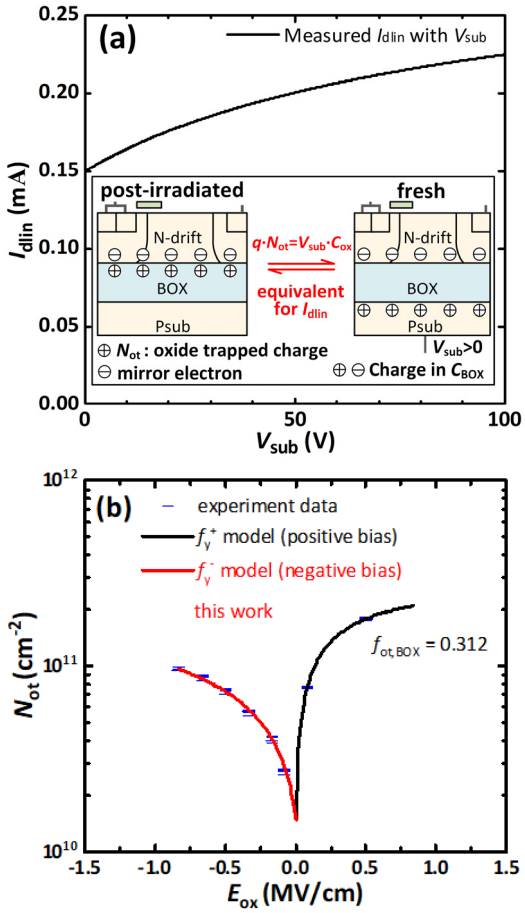

Fig. 3. (a) Measured I_{dlin}–V_{sub}curve in fresh device. The inset is the schematic of the equivalent relationship to I_{dlin} between V_{sub} and N_{ot} in SOI/BOX interface. (b) Extracted N_{ot} in SOI/BOX interface with different BG bias at 1 krad (Si).

where g_0 is the electron–hole pair generation rate induced by γ-ray in SiO_2. f_y^+ is the fraction of holes that escape recombination and reach the Si/SiO_2 interface, as shown in (2). E_0^+, E_1^+, and m in (2) are constants, $E_1^+ = 0.55$ MV/cm, $E_0^+ = 7.62 \times 10^{-3}$ MV/cm, and $m = 0.7$ for Co^{60}, $f_y^+ = 0.05$ in low electric field [18], [19]. f_{ot} is the hole trapping efficiency with dependence on quality of Si/SiO_2 interface. t_{ox} is the thickness of oxide layer. E_{ox} is the vertical electric field in the oxide layer during irradiation. In this article, f_{ot} is 0.312 [extracted at positive BG bias, $D = 1$ krad(Si)] for silicon direct bonding (SDB) SOI technology. Moreover, N_{ot} generated in SOI/BOX interface under the negative bias shows a great dependence on electric field too. However, it is far less than that generated in positive bias. In the function of the traditional model, f_y is related to electric field. Then, an empirical equation of f_y^- can be determined by experimental data, as shown in

$$f_y^- = \left(\frac{|E_{ox}| + E_0^-}{|E_{ox}| + E_1^-}\right)^m \tag{3}$$

where $E_1^- = 3.62$ MV/cm and $E_0^- = 0.05$ MV/cm. f_y^- and f_y^+ are continuous at $E_{ox} = 0$.

B. N_{ot} Saturation Effect

With N_{ot} induced by TID increasing, the trapping efficiency of the following holes induced by TID in SiO_2 would decrease linearly. At last, the trapping centers near the Si/SiO_2 interface are filled with holes, and no more following holes can be trapped there. Based on this concept, f_{ot} is also a function of N_{ot} which can be expressed as

$$f_{ot}(N_{ot}) = f_{ot}(0) \cdot \left(1 - N_{ot}/N_{ot,SAT}\right) \tag{4}$$

where $f_{ot}(0)$ is the trapping efficiency for fresh interface. $N_{ot,SAT}$ is the saturation N_{ot} numerically equal to the value of trapping centers in Si/SiO_2 interface and is related to interface quality.

The differential form of (1) represents the growth rate of N_{ot} induced by TID, which remains the understanding of physical processes in (1), as shown in

$$dN_{ot}/dD = g_0 \cdot f_{ot}(N_{ot}) \cdot f_y \cdot t_{ox}. \tag{5}$$

The boundary conditions of $N_{ot}(D)$ define the fresh and saturation points, as shown in

$$N_{ot}(0) = 0, N_{ot}(+\infty) = N_{ot,SAT}. \tag{6}$$

Solve equations of (4)–(6) simultaneously, N_{ot} distribution can be determined, as shown in

$$\begin{aligned} N_{ot}(D) &= N_{ot,SAT} \cdot [1 - \exp(-D/D_0)], \\ D_0 &= N_{ot,SAT}/(g_0 \cdot f_{ot}(0) \cdot f_y \cdot t_{ox}) \end{aligned} \tag{7}$$

where D_0 and f_y are related to the local electric field during irradiation bias.

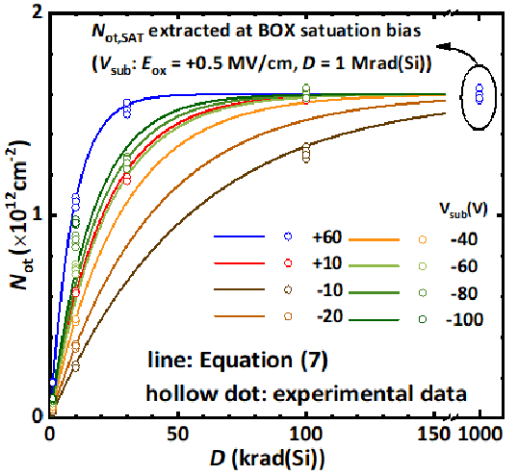

Fig. 4. Modeling N_{ot}–D curves with different $E_{ox,\,BOX}$ and experimental data under different BG bias.

Fig. 4 shows modeling N_{ot}–D curves with different E_{ox} in BOX and the corresponding experimental data under different BG bias. Equation (1) can only explain the linear increasing damage at very first stage of radiation. Due to the N_{ot} saturation effect, the extracted f_{ot} would be distorted and smaller at a larger D. Thus, $f_{ot} = 0.312$ is extracted at 1 krad(Si) in this article. $N_{ot,SAT} = 1.6 \times 10^{12}$ cm^{-2} for SOI/BOX interface of SDB technology is also extracted at BOX saturation bias condition [V_{sub}: $E_{ox} = +0.5$ MV/cm, $D = 1$ Mrad(Si)].

C. Simulation of TID Effect on HV SOI LDMOS

In our previous work [20], [21], uniform positive fixed charges are set in the SOI/BOX interface to analyze TID effect on HV SOI LDMOS. However, N_{ot} distribution is supposed to be determined more strictly. In [22], a simulation method of TID on bulk-Si LDMOS introducing a nonuniform distribution of N_{ot} in oxide blocks is reported, but the influence of electric field direction on N_{ot} distribution is not considered. Consequently, it is not applicable for HV SOI LDMOS. Since the model considering f_y^- and N_{ot} saturation effect is established, a more accurate simulation method is proposed for prediction of TID effect on HV SOI LDMOS. Fig. 5(a) shows the schematic flowchart for the simulation of TID effect on HV SOI LDMOS. Fig. 5(b) shows the schematic of introduction of N_{ot} values as fixed charges in each oxide block in SOI/BOX for TID simulation on HV SOI LDMOS.

For preirradiated device, E_{ox} distribution profile along the SOI/BOX interface during irradiation bias is extracted, as shown in Fig. 6(a). Then the N_{ot} distribution profile along the SOI/BOX interface can be calculated by (7), as shown in Fig. 6(b). Since the electric field under drain side is higher than that under source side, N_{ot} increases quickly and saturates fast there. It manifests that the BOX under drain side is the sensitive spot under OFF-state irradiation bias.

IV. Results and Discussions

Simulated results with TCAD tool [23], [24] including the calculated N_{ot} distribution and N_{it} with different D have been compared with the experimental data to validate the proposed model and analyze TID effect on HV SOI LDMOS, as shown in Fig. 7. The comparison of electrical characteristic shift

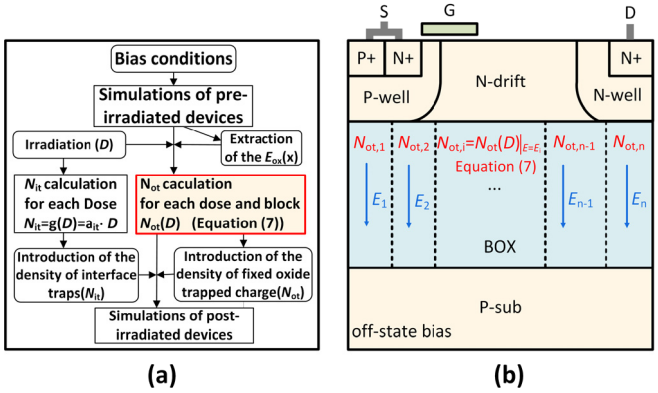

Fig. 5. Schematic of (a) flowchart for the simulation of TID effect on HV SOI LDMOS and (b) introduction of N_{ot} values as fixed charges in each oxide block in SOI/BOX for TID simulation on HV SOI LDMOS.

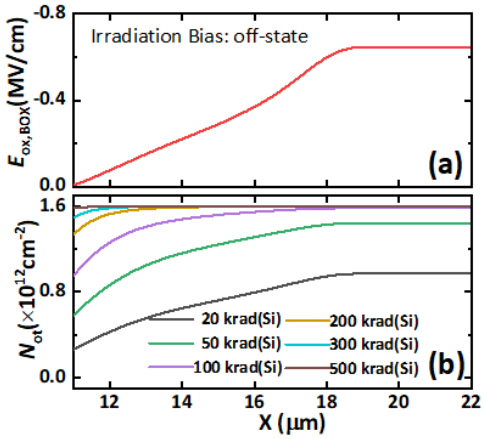

Fig. 6. (a) Simulated E_{ox} distribution profile along the SOI/BOX interface. (b) Calculated N_{ot} distribution profiles along the SOI/BOX interface with different D under OFF-state bias.

curves between radiation-hardened LDMOS in this article and the conventional reduced-surface-field (RESURF) LDMOS with optimal charges is also given. The implantation doses of N-drift region (D_N) are 0.6×10^{12} and 1.4×10^{12} cm^{-2} for the radiation-hardened HV SOI LDMOS and the conventional RESURF HV SOI LDMOS, respectively.

A. Mechanism of BV Shift and Hardening Strategy

As shown in Fig. 7(a), the BV shift curves are given and the simulation results show a good agreement with the experimental results. The corresponding simulated electric field distributions at a series of D with the proposed model are given in Fig. 8(a) and (b) to reveal the BV shift mechanism. In order to facilitate our quantitative discussion of the mechanism, BV_L is defined as the lateral BV from drain to source, which is related to drift length and drift doping concentration. BV_V is defined as the vertical BV from drain to substrate, as shown in [25]

$$BV_V = \frac{1}{2} t_{Si} \cdot E_c + \frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{ox} \cdot E_c \tag{8}$$

where t_{Si} and t_{ox} are the thicknesses of SOI layer and BOX layer, respectively; ε_{Si} and ε_{ox} are the relative dielectric constants of Si and SiO_2, respectively; E_c is the critical breakdown

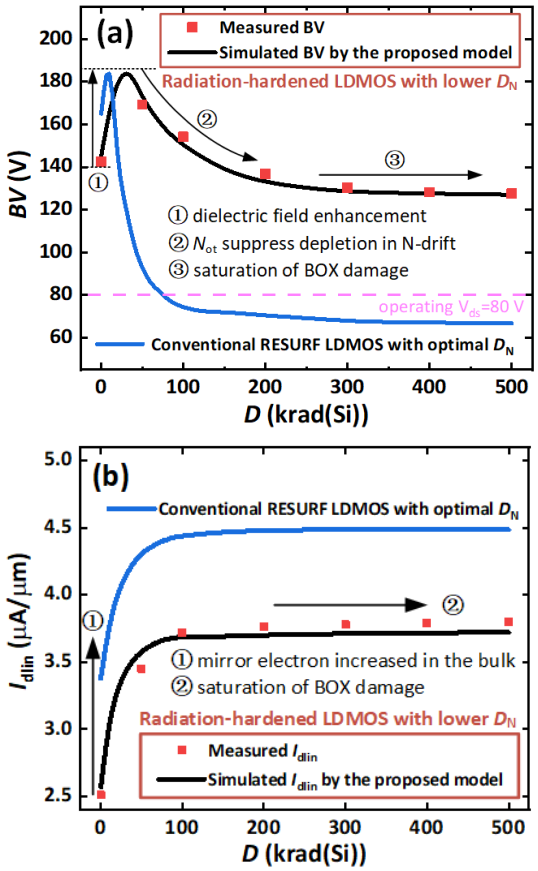

Fig. 7. (a) Measured BV and simulated BV shift curves with TID under OFF-state bias with different D_N. (b) Measured I_{dlin} and simulated I_{dlin} shift curves with TID under OFF-state bias with different D_N.

electric field for Si. The BV of HV SOI LDMOS is determined by the smaller one between BV_L and BV_V.

The BV shift behavior is divided into three stages. For the fresh device, the breakdown point is located in the bulk and BV is determined by BV_V. In the first stage, N_{ot} under drain side will enhance electric field in the BOX layer by Gauss's law and BV_V increases, as shown in

$$\Delta BV_V = t_{ox} \cdot \Delta E_{ox} = t_{ox} \cdot q \cdot N_{ot|\text{under drain side}} / \varepsilon_{ox}. \quad (9)$$

Due to the fact that the breakdown point still locates in the bulk, BV_V rises from 145 to 185 V at $D = 30$ krad(Si), and then BV reaches its maximum value. With D increasing further, N_{ot} under drift region begins to suppress depletion in drift region causing the breakdown point transferring from bulk to surface, and the electric field peak in the p-well/N-drift junction increases, accounting for the sharp drop of BV. After $D = 200$ krad(Si), N_{ot} gradually saturates and the BV falling trend slows down, then BV maintains about 127 V at last, which can meet the radiation-hardening requirement. By contrast, Fig. 7(a) also gives the BV shift curve of the conventional RESURF LDMOS with optimal N-drift charges. The TID tolerance of the conventional RESURF LDMOS is not enough and BV will soon drop below the operating voltage before 100 krad(Si). The corresponding simulated electric field distributions at a series of D are also given in Fig. 8(c) and (d).

The BV shift behavior in the radiation-hardened HV SOI LDMOS has been carefully designed and the methodology is described below. For conventional HV SOI LDMOS in consumer electronics, RESURF technology is widely applied to pursue high BV with high current capacity in fresh devices [26]–[29]. However, for HV SOI LDMOS in space radiation-hardening application, nondegradation BV is supposed to be guaranteed whereas other electrical characteristics in the fresh device can be sacrificed moderately.

To postpone the premature breakdown at surface and leave margin for the unwanted increasement in surface electric field peak at source side, a lower doping concentration in N-drift region rather than the conventional optimized RESURF doping concentration is introduced in the device and the surface electric field peak at source side can be lower than that at drain side in the fresh device. As a result, BV performance of the radiation-hardened device in this article is tolerant with the radiation at the first stage and benefits by dielectric field enhancement while ensuring the breakdown happens in the bulk.

B. Mechanism of I_{dlin} Increase

As shown in Fig. 7(b), the I_{dlin} shift curves are given. Due to the fact that N_{ot} could cause mirror electrons in the SOI layer at ON-state, an extra conduction path is generated above the SOI/BOX interface. I_{dlin} ascends from 2.5 to 3.7 μA/μm at $D = 100$ krad(Si), and then reaches a plateau with N_{ot} saturating. ON-resistance (R_{on}) is defined as the resistance of the device at a linear region with $V_{gs} = 20$ V, which can be briefly expressed as

$$R_{ON} = R_{ch} + R_{acc} + R_d // \Delta R(D) + R_{nwell} \quad (10)$$

where R_{ch} and R_{acc} are the channel resistance and resistance of accumulation region, respectively; R_{nwell} is the resistance of n-well region; R_d is the resistance of drift region; $\Delta R(D)$ is the resistance of the extra conduction path induced by TID, as shown in (11). R_d is in parallel with $\Delta R(D)$

$$\Delta R(D) = \int_{L_d} dx / q \mu_n N_{ot}(D, x). \quad (11)$$

For higher D_N, the fresh current capability is higher. However, it brings premature breakdown as mentioned above. Thus, the modest sacrifice of fresh I_{dlin} has to be accepted.

C. Tolerance Design of Radiation-Hardening HV SOI LDMOS

The tradeoff between fresh electrical characteristics and postirradiation BV performance has to be carefully considered in HV SOI LDMOS for a given substrate material. Fig. 9 shows the simulated BV and I_{dlin} with different D_N under OFF-state bias at a series of D. The values of the interface quality parameters set in the simulation are the extracted values of the experiment. Higher margin of postirradiation BV performance can be obtained at lower D_N. However, lower D_N will induce lower fresh BV and current capability. In order to ensure that the device under OFF-state irradiation bias with 100 krad(Si) can meet the radiation-hardening requirement of BV > 80 V, D_N can be set to 1.2×10^{12} cm^{-2} at most. Under the same conditions, D_N can only be set to 1.0×10^{12} cm^{-2} at most for the requirement of withstanding 300 krad(Si). It indicates that the higher TID tolerance is easier to accomplish with the lower value of D_N.

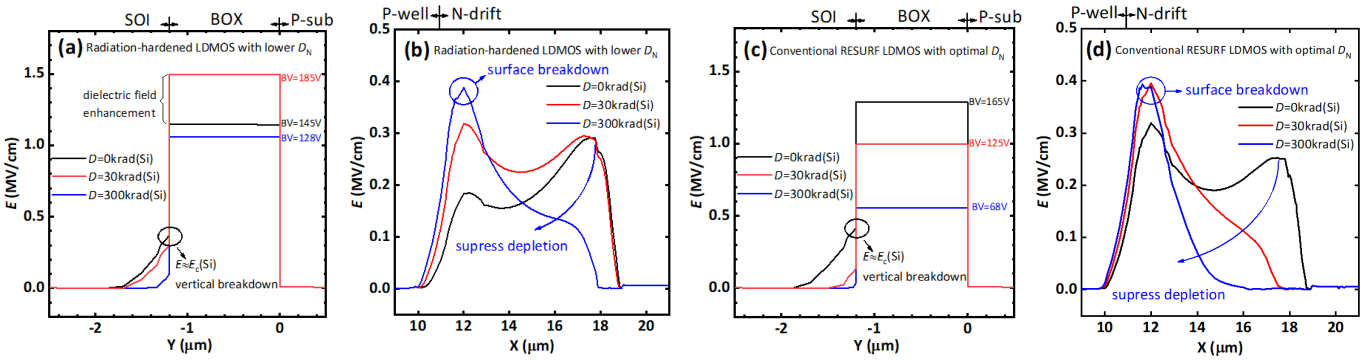

Fig. 8. Simulated (a) vertical electric field distributions at drain side and (b) surface electric field distributions of HV SOI LDMOS with different D under OFF-state bias on radiation-hardened HV SOI LDMOS. Simulated (c) vertical electric field distributions at drain side and (d) surface electric field distributions of HV SOI LDMOS with different D under OFF-state bias on conventional RESURF HV SOI LDMOS with optimal D_N.

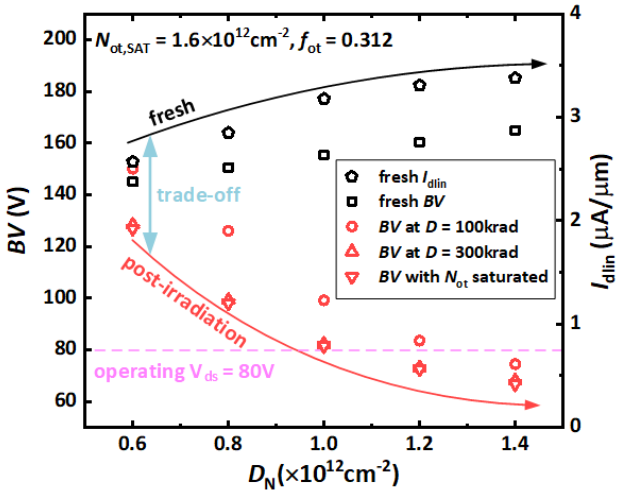

Fig. 9. Simulated BV and I_{dlin} with different D_N under OFF-state irradiation bias at a series of D. The tradeoff between fresh electrical characteristics and postirradiation BV performance.

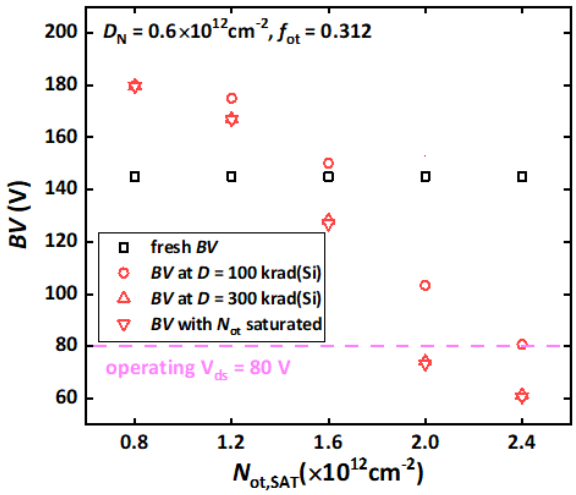

Fig. 10. Simulated BV with different $N_{ot,\,SAT}$ under OFF-state bias at a series of D.

The interface quality is strongly related to the oxide formation process, such as oxidation time, temperature, atmosphere, and annealing process [30]–[34]. We benefit by the establishment of the simulated method with the proposed model; the influence of the values of $N_{ot,SAT}$ and f_{ot} on postirradiation behavior for HV SOI LDMOS is clear. The value of $N_{ot,SAT}$ dominates the worst postirradiation electrical characteristics at last and the value of f_{ot} dominates how fast N_{ot} saturates. Besides, the tolerance design work should also focus on the interface quality parameter selection for space radiation-hardening HV SOI LDMOS. Fig. 10 shows the simulated BV with different $N_{ot,SAT}$ under OFF-state bias at a series of D. For $N_{ot,SAT} = 0.8 \times 10^{12}$ cm^{-2}, N_{ot} saturates soon, and the postirradiation BV is almost a constant after 50 krad(Si). As the value of $N_{ot,SAT}$ is not enough to suppress the depletion of the drift region and the breakdown point is still located in bulk, then the postirradiation BV can maintain at a high level about 180 V. For $N_{ot,SAT}$ as high as 1.6×10^{12} cm^{-2}, the postirradiation device can guarantee BV $>$ 120 V with the N_{ot} saturated in SOI/BOX interface. As $N_{ot,SAT}$ further rises to 2.4×10^{12} cm^{-2}, the postirradiation device barely meets the requirement of BV $>$ 80 V at $D = 100$ krad(Si) with little margin.

The radiation-hardened-by-design HV SOI LDMOS investigated in this article obtains a satisfied radiation-hardened BV performance, which is based on a low-cost and highly accessible commercial SOI substrate material with plain interface quality parameters. Meanwhile, as discussed in Fig. 10, smaller $N_{ot,SAT}$ indeed aids to increase the design margin of radiation-hardening HV SOI LDMOS. As one of the main considerations in radiation-hardening-by-process technology, there are many reported technologies focusing on improving the Si/SiO$_2$ interface quality during irradiation [35]–[37]. For HV SOI LDMOS, the BOX layer should be thick to support the high vertical BV, which requires a long time for thermal oxidation process. Thus, the radiation-hardening-by-process realization in SDB technology deserves further investigation.

V. Conclusion

By analyzing the I_{dlin} shift behavior under different BG bias, N_{ot} generation in SOI/BOX interface under negative electric field is confirmed, and the empirical function relationship between N_{ot} in SOI/BOX interface and negative electric field is obtained by experimental data. Then, the TCAD tool can be more suitable to predict the postirradiation device behavior, especially for HV SOI LDMOS under OFF-state bias, by appropriately tunning the proposed model on BOX

damage into its code. Moreover, the electrical characteristic shift mechanism induced by TID effect on HV SOI LDMOS under OFF-state bias is also revealed by accurate simulation analysis. Ultimately, the accurate simulation method in this article can provide convenience for the tolerance design of radiation-hardening HV SOI LDMOS. Besides, the radiation-hardened-by-design HV SOI LDMOS introduced in this article is fabricated on a commercial SOI substrate material with plain interface quality parameters and the corresponding BV hardening strategy is also discussed in detail.

REFERENCES

[1] P. M. Shea and Z. J. Shen, "Numerical and experimental investigation of single event effects in SOI lateral power MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 6, pp. 2739–2747, Dec. 2011, doi: 10.1109/TNS.2011.2172956.

[2] S. Diez, M. Ullan, G. Pellegrini, M. Lozano, R. Sorge, and D. Knoll, "Radiation studies of power LDMOS devices for high energy physics applications," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 6, pp. 3322–3328, Dec. 2010, doi: 10.1109/TNS.2010.2085051.

[3] H. J. Barnaby, "Total-ionizing-dose effects in modern CMOS technologies," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3103–3121, Dec. 2006, doi: 10.1109/TNS.2006.885952.

[4] Y. Arai, T. Miyoshi, and I. Kurachi, "SOI monolithic pixel technology for radiation image sensor," in *IEDM Tech. Dig.*, Dec. 2017, pp. 16.2.1–16.2.4, doi: 10.1109/IEDM.2017.8268401.

[5] G. Yang *et al.*, "Experimental investigation on the electrical properties of SOI-LIGBT under total-ionizing-dose radiation," in *Proc. ISPSD*, Sep. 2020, pp. 431–434, doi: 10.1109/ISPSD46842.2020.9170168.

[6] X. Li *et al.*, "Degradation of radiation-hardened vertical double-diffused metal-oxide-semiconductor field-effect transistor during gamma ray irradiation performed after heavy ion striking," *IEEE Electron Device Lett.*, vol. 41, no. 2, pp. 216–219, Feb. 2020, doi: 10.1109/LED.2019.2961259.

[7] D. Seo, L. D. Trang, J.-W. Han, J. Kim, S. Lee, and I.-J. Chang, "Total ionizing dose effect on ring oscillator frequency in 28-nm FD-SOI technology," *IEEE Electron Device Lett.*, vol. 39, no. 11, pp. 1728–1731, Nov. 2018, doi: 10.1109/LED.2018.2872345.

[8] Y. T. Roh and H. C. Lee, "Layout modification of a PD-SOI n-MOSFET for total ionizing dose effect hardening," *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 308–315, Jan. 2019, doi: 10.1109/TED.2018.2881668.

[9] J.-Y. Park *et al.*, "Local electro-thermal annealing for repair of total ionizing dose-induced damage in gate-all-around MOSFETs," *IEEE Electron Device Lett.*, vol. 37, no. 7, pp. 843–846, Jul. 2016, doi: 10.1109/LED.2016.2574341.

[10] E. Chatzikyriakou, K. Morgan, and C. H. K. de Groot, "Total ionizing dose hardened and mitigation strategies in deep submicrometer CMOS and beyond," *IEEE Trans. Electron Devices*, vol. 65, no. 3, pp. 808–819, Mar. 2018, doi: 10.1109/TED.2018.2792305.

[11] O. Flament, A. Torres, and V. Ferlet-Cavrois, "Bias dependence of FD transistor response to total dose irradiation," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 6, pp. 2316–2321, Dec. 2003, doi: 10.1109/TNS.2003.822594.

[12] I. S. Esqueda *et al.*, "Modeling the radiation response of fully-depleted SOI n-channel MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 4, pp. 2247–2250, Aug. 2009, doi: 10.1109/TNS.2009.2012709.

[13] C. Peng *et al.*, "Total-ionizing-dose induced coupling effect in the 130-nm PDSOI I/O nMOSFETs," *IEEE Electron Device Lett.*, vol. 35, no. 5, pp. 503–505, May 2014, doi: 10.1109/LED.2014.2311453.

[14] H. E. Boesch, F. B. McLean, J. M. Benedetto, J. M. McGarrity, and W. E. Bailey, "Saturation of threshold voltage shift in MOSFET's at high total dose," *IEEE Trans. Nucl. Sci.*, vol. NS-33, no. 6, pp. 1191–1197, Dec. 1986, doi: 10.1109/TNS.1986.4334577.

[15] S. P. Kama, R. D. Pugh, C. P. Brothers, W. Shedd, and B. B. K. Singaraju, "Microscopic structure and generation mechanism of Eγ centers in buried oxide," in *Proc. IEEE Int. SOI Conf.*, Oct. 1997, pp. 32–33, doi: 10.1109/SOI.1997.634918.

[16] K. O. Petrosjanc, A. S. Adonin, I. A. Kharitonov, and M. V. Sicheva, "SOI device parameter investigation and extraction for VLSI radiation hardness modeling with SPICE," in *Proc. IEEE Int. Conf. Microelectronic Test Struct.*, San Diego, CA, USA, Mar. 1994, pp. 126–129, doi: 10.1109/ICMTS.1994.303490.

[17] K. Neumeier, P. Seegebrecht, and H. P. Bruemmer, "Radiation tolerance of double layer field oxides," *IEEE Trans. Nucl. Sci.*, vol. 39, no. 3, pp. 391–395, Jun. 1992, doi: 10.1109/23.277524.

[18] S. Wang *et al.*, "A model for radiation-induced off-state leakage current in N-channel metal-oxide-semiconductor transistors with shallow trench isolation," *J. Appl. Phys.*, vol. 107, no. 2, Jan. 2010, Art. no. 024515, doi: 10.1063/1.3277017.

[19] M. R. Shaneyfelt, D. M. Fleetwood, J. R. Schwank, and K. L. Hughes, "Charge yield for cobalt-60 and 10-keV X-ray irradiations of MOS devices," *IEEE Trans. Nucl. Sci.*, vol. 38, no. 6, pp. 1187–1194, Dec. 1991, doi: 10.1109/23.124092.

[20] X. Zhou *et al.*, "Total-ionizing-dose irradiation-induced dielectric field enhancement for high-voltage SOI LDMOS," *IEEE Electron Device Lett.*, vol. 40, no. 4, pp. 593–596, Apr. 2019, doi: 10.1109/LED.2019.2900370.

[21] L. Shu *et al.*, "Numerical and experimental investigation of TID radiation effects on the breakdown voltage of 400-V SOI NLDMOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 66, no. 4, pp. 710–715, Apr. 2019, doi: 10.1109/TNS.2019.2905218.

[22] P. Fernández-Martínez *et al.*, "Simulation of total ionising dose on LDMOS devices for high energy physics applications," in *Proc. RADECS*, Sep. 2011, pp. 384–389, doi: 10.1109/RADECS.2011.6131412.

[23] *Taurus TSUPREM-4 User Guide Version Q-2019.12*, Synopsys, Mountain View, CA, USA, Dec. 2019.

[24] *Taurus Medici User Guide Version Q-2019.12*, Synopsys, Mountain View, CA, USA, Dec. 2019.

[25] B. Zhang, Z. Li, S. Hu, and X. Luo, "Field enhancement for dielectric layer of high-voltage devices on silicon on insulator," *IEEE Trans. Electron Devices*, vol. 56, no. 10, pp. 2327–2334, Oct. 2009, doi: 10.1109/TED.2009.2028405.

[26] J. A. Appels and H. M. J. Vaes, "High voltage thin layer devices (RESURF devices)," in *IEDM Tech. Dig.*, Dec. 1979, pp. 238–241, doi: 10.1109/IEDM.1979.189589.

[27] A. Popescu, F. Udrea, and W. Milne, "A numerical study of the RESURF effect in bulk and SOI power devices," in *Proc. Int. Semiconductor Conf.*, vol. 1, Oct. 1997, pp. 127–130, doi: 10.1109/SMICND.1997.651563.

[28] S.-K. Chung, "An analytical model for breakdown voltage of surface implanted SOI RESURF LDMOS," *IEEE Trans. Electron Devices*, vol. 47, no. 5, pp. 1006–1009, May 2000, doi: 10.1109/16.841233.

[29] J. A. van der Pol *et al.*, "A-BCD: An economic 100 V RESURF silicon-on-insulator BCD technology for consumer and automotive applications," in *Proc. ISPSD*, May 2000, pp. 327–330, doi: 10.1109/ISPSD.2000.856836.

[30] Y. Wu and J. Hwu, "Improvement in radiation hardness of reoxidized nitrided oxide (RNO) in the absence of post-oxidation anneal," *IEEE Electron Device Lett.*, vol. 14, no. 1, pp. 1–3, Jan. 1993, doi: 10.1109/55.215081.

[31] Y. Zhao, Y. Hu, R. Yan, G. Zhang, and D. Ren, "A thermal field oxidation process for ionizing radiation hardness," in *Proc. 4th Int. Conf. Solid-State IC Technol.*, 1995, pp. 665–667, doi: 10.1109/ICSICT.1995.503384.

[32] K. Neumeier and H. P. Bruemmer, "A systematic investigation of the influence of processing parameters on the radiation hardness of reoxidized nitrided oxides," in *Proc. 3rd Eur. Conf. Radiat. Effects Compon. Syst.*, Sep. 1995, pp. 131–136, doi: 10.1109/RADECS.1995.509765.

[33] T.-Y. Huang *et al.*, "Improving radiation hardness of EEPROM/flash cell by N_2O annealing," *IEEE Electron Device Lett.*, vol. 19, no. 7, pp. 256–258, Jul. 1998, doi: 10.1109/55.701435.

[34] P. Paillet, J. L. Autran, O. Flament, J. L. Leray, B. Aspar, and A. J. Auberton-Herve, "X-radiation response of SIMOX buried oxides: Influence of the fabrication process," in *Proc. RADECS*, Sep. 1995, pp. 147–151, doi: 10.1109/RADECS.1995.509768.

[35] S. T. Liu, W. C. Jenkins, and H. L. Hughes, "Total dose radiation hard 0.35 μm SOI CMOS technology," *IEEE Trans. Nucl. Sci.*, vol. 45, no. 6, pp. 2442–2449, Dec. 1998, doi: 10.1109/23.736484.

[36] K. Neumeier and H. P. Bruemmer, "Radiation hard LOCOS field oxide," *IEEE Trans. Nucl. Sci.*, vol. 41, no. 3, pp. 572–576, Jun. 1994, doi: 10.1109/23.299801.

[37] S. T. Liu, W. C. Jenkins, H. L. Hughes, and A. J. Auberton-Herve, "Total dose radiation induced back channel threshold voltage shifts and standby currents of CMOS devices fabricated in UNIBOND^{TM} materials," *Silicon Insulator Technol. Devices*, vol. PV97-23, pp. 307–312, 1997.