Interface States Characterization of UTB SOI MOSFETs From the Subthreshold Current

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***Abstract*—Quantification of interface traps for double-gate fully depleted silicon-on-insulator transistors is needed for accurate device modeling and technology development. The trap density can be estimated as a function of the activation energy from the subthreshold current using the methodology developed in this work. It combines the earlier proposed g_m/I_D method with a revised form of the *k*-sweep method. The method is verified using TCAD simulated data and applied on engineering samples produced in 22FDX (R) technology, yielding a typical trap density of $2 \cdot 10^{11}$ cm^{-2}eV^{-1}. Association of the traps to the front or back interface is nontrivial; a trap allocation error of at least 20% is reported.**

***Index Terms*—Ideality, interface states, MOS transistors, silicon devices, silicon on insulator, subthreshold, traps.**

I. Introduction

THE electrostatic charge in the channel of ultrathin body (UTB) transistors, such as FinFETs and fully depleted silicon-on-insulator (FD-SOI) devices, is controlled by two gates. Interface traps between the silicon channel and the oxide layers limit the electrostatic gate control [1]–[3]; and they are a source of noise [4], [5]. Quantification of these traps is, therefore, needed for accurate device modeling and technology development.

Floating-body devices lack a body contact. Without that, methods that are conventionally used to extract the density and energy landscape of the interface traps, such as the charge-pumping method [2] or quasi-static capacitance-voltage measurements [6], cannot be applied. The g_m/I_D-method was recently demonstrated for SOI FinFETs and circumvents the need for a body contact [7]. In this method, the subthreshold slope is used to determine the interface trap density as a function of the energy. The problem, however, is that this method only applies to symmetric double-gate (DG) devices, not to FD-SOI transistors. For these, another method was demonstrated which uses a combined sweep of both the front gate (V_{FG}) and the back gate (V_{BG}) with a constant ratio $k = V_{BG}/V_{FG}$ [8]. The method uses the *average* subthreshold swing as a function of k to obtain the total back oxide interface trap density.

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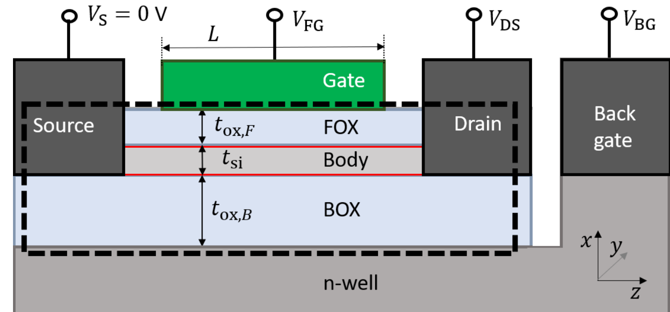

Fig. 1. Schematic cross section of an UTB SOI MOSFET. The contacts, material layers and layer thicknesses, the interfaces including traps (red lines), and the FEM structure (black dashed box) are indicated.

In this work, we propose a method to determine the interface trap density as a function of the energy from the subthreshold characteristics of state-of-the-art (asymmetric) UTB SOI MOSFETs (see Fig. 1). The method uses a simultaneous sweep of the front gate and the back gate with a constant ratio k, as proposed in [8] and [9], employing a modified, closed-form equation for the inversion charge and a correction for gate work-function differences. The g_m/I_D-method [7] is then used to obtain interface trap densities as a function of energy. We will refer to this combination of techniques as the *k-sweep energy profiling* method. The method is used to extract the total trap density and separate the trap densities of the front and back interfaces. Trap separation is nontrivial and the difficulties that arise are examined and explained using the underlying physics. This work extends [7]–[9] by combining both techniques, by proposing a physical description and methodology that is applicable to a wider range of device architectures, and by a rigorous validation using finite-element simulations and experimental data.

Section II presents the theoretical background of methodologies discussed in the literature and emphasizes the modifications made for the k-sweep energy profiling method. Details about the experimental approach, simulations, and data analysis are presented in Section III. The results are reported in Section IV, and Section V comprises the conclusions and recommendations.

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II. Theory

A. Subthreshold Swing and Interface Traps

In this section, we discuss the relation between the subthreshold swing and the interface trap density. We consider long channel devices and ignore inhomogeneities along the channel; therefore, 1-D electrostatics apply. Considering that the free carrier charge in the channel can be neglected in subthreshold, a linearly varying potential is present across the body [3], [10]–[12].

The subthreshold drain current for an n-type UTB DG device is then given by [13]

$$I_D = u_T \mu_n Q_i \frac{W}{L}\left[1 - \exp\left(\frac{-V_{DS}}{u_T}\right)\right] \tag{1}$$

with $u_T = k_B T/q$, k_B is Boltzmann's constant, T is the temperature, q is the elementary charge, μ_n is the electron mobility, W is the gate width, L is the (effective) channel length, V_{DS} is the applied drain-source voltage, and Q_i is the inversion charge. Control from the two gates may be symmetric or asymmetric, depending on the ratio of front oxide (FOX) capacitance to back oxide capacitance, $C_{ox,F}/C_{ox,B}$. For symmetric devices, e.g., FinFETs, and for strongly asymmetric devices, e.g., thick BOX layer FD-SOI devices, Q_i can be approximated as [13]

$$Q_i = -qn_i t_{si}\frac{1}{2}\left[\exp\left(\frac{\psi_{s,F}}{u_T}\right) + \exp\left(\frac{\psi_{s,B}}{u_T}\right)\right] \tag{2}$$

with n_i being the intrinsic carrier density and t_{si} the thickness of the silicon body, and where $\psi_{s,F}$ and $\psi_{s,B}$ are the front and back surface potentials.

A more generally applicable expression, valid for FD-SOI devices with any $C_{ox,F}/C_{ox,B}$-ratio, was derived as [13], [14]

$$Q_i = -qn_i t_{si}\left[\frac{\exp\left(\frac{\psi_{s,B}}{u_T}\right) - \exp\left(\frac{\psi_{s,F}}{u_T}\right)}{\left(\frac{\psi_{s,B}-\psi_{s,F}}{u_T}\right)}\right]. \tag{3}$$

The surface potentials in (2) and (3) are related to the front- and back-gate voltages through electrostatics relations. Following [3], [8], [9], and [12], we consider a simultaneous sweep of the front gate voltage and the back gate voltage with a constant ratio of $V_{BG} = k \cdot V_{FG}$ and obtain

$$\psi_{s,F} = \frac{C_{ox,F}C_B + kC_{si}C_{ox,B}}{C_F C_B - C_{si}^2}\cdot V_{FG} - \frac{\Delta\phi_{F,ch}C_{ox,F}C_B + \Delta\phi_{B,ch}C_{si}C_{ox,B}}{C_F C_B - C_{si}^2} \tag{4}$$

$$\psi_{s,B} = \frac{kC_{ox,B}C_F + C_{si}C_{ox,F}}{C_B C_F - C_{si}^2}\cdot V_{FG} - \frac{\Delta\phi_{B,ch}C_{ox,B}C_F + \Delta\phi_{F,ch}C_{si}C_{ox,F}}{C_B C_F - C_{si}^2} \tag{5}$$

with $C_F \equiv C_{si} + C_{ox,F} + C_{it,F}$ and $C_B \equiv C_{si} + C_{ox,B} + C_{it,B}$ being the front and back equivalent capacitances, respectively, and $C_{it,F}$ and $C_{it,B}$ the front and back interface trap capacitances, respectively. $C_{si} \equiv \varepsilon_{si}/t_{si}$ is the depleted silicon film capacitance, with ε_{si} being the permittivity of silicon, and $\Delta\phi_{F,ch}$ and $\Delta\phi_{B,ch}$ are the front and back gate work-function differences with the channel. The front interface is characterized for $k = 0$, and the back interface is characterized when k is very high.

The interface trap density can be extracted from the measured current–voltage characteristics more easily if there is no vertical field in the silicon body, i.e., if the two surface potentials are equal. We, therefore, define the desired ratio $k = k_0$ for $\psi_{s,F} = \psi_{s,B}$. By assuming that $\partial\psi_{s,F}/\partial V_{FG} = \partial\psi_{s,B}/\partial V_{FG}$ suffices to obtain $\psi_{s,F} = \psi_{s,B}$, it is derived in [8] that

$$k_0 = \frac{C_{ox,F}\left(C_{ox,B} + C_{it,B}\right)}{C_{ox,B}\left(C_{ox,F} + C_{it,F}\right)}. \tag{6}$$

Without interface traps, $k_0 = 1$, independent of the oxide thicknesses. In practice, however, interface traps do contribute, and k_0 is not known ($k_0 \neq 1$).

The desired voltage ratio k_0 can be defined from the subthreshold swing with respect to the front gate; $SS_F = dV_{FG}/d\log_{10}(I_D)$ [or from the subthreshold swing with respect to the back gate; $SS_B = dV_{BG}/d\log_{10}(I_D)$]. The subthreshold swing is thus generally defined by combining (1) and (3)–(5). In this case, no analytical solution exists, and we have to numerically solve for SS_F around k_0, as explained in Section II-C. Because of the assumed two conducting channels in (2), $I_D = I_{D,F}(\psi_{s,F}) + I_{D,B}(\psi_{s,B})$. For the front gate referred subthreshold swing at $k = k_0$ [see (6)], it then follows that [8]:

$$SS_F|_{k_0} = \ln(10)u_T\left(1 + \frac{C_{it,F}}{C_{ox,F}}\right) \tag{7}$$

which induces only a minor error around $k = k_0$; hence, (2) can be used instead of (3) to obtain the subtreshold swing around k_0 analytically.

We can thus conclude that the front interface trap capacitance $C_{it,F}$ can be extracted from the front gate referred subthreshold swing at $k = k_0$ if k_0 is known. Also, (7) is equal to that obtained for (symmetric) FinFET devices [7]. Combining (6) and (7) shows the relation between the subthreshold swing and the front and back interface trap densities, $D_{it,F} = C_{it,F}/q$ and $D_{it,B} = C_{it,B}/q$ [7].

B. Extracting the Front or Back Interface States

The formalism presented in Section II-A is insufficient for an unambiguous quantification of the front or back interface state densities. Assuming that the front and back oxide capacitances are known, we have two equations, (6) and (7), and three unknowns, $C_{it,F}$, $C_{it,B}$, and the $SS_F|_{k_0}(k_0)$-relation. Therefore, an additional condition needs to be imposed.

Three realistic conditions in practical technologies, where the interface trap density is relatively small compared with the oxide capacitance, are

$$D_{it,F} \ll D_{it,B} \tag{8a}$$

$$D_{it,F} \gg D_{it,B} \tag{8b}$$

$$D_{it,F} = D_{it,B}. \tag{8c}$$

The first condition (8a) often holds for earlier SOI technologies with relatively thick body and BOX layers and with thermally grown SiO_2 as top gate dielectric. This was qualitatively shown for Silicon Implanted with Oxygen (SIMOX) wafers with charge pumping measurements [15] and quantitatively for FD-SOI devices, where a ratio of $D_{it,B}/D_{it,F} \approx 25$ was obtained [9]. The second condition (8b) commonly applies in modern

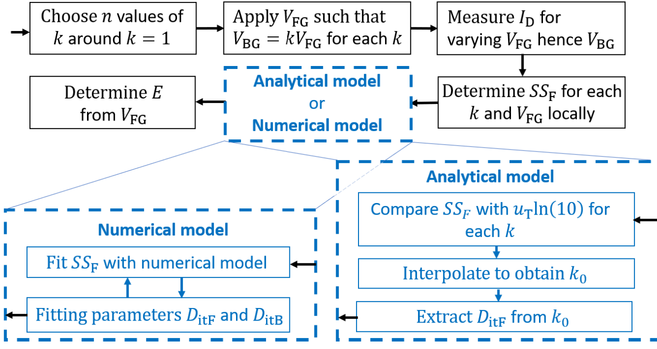

Fig. 2. Flow diagram of the energy profiling *k*-sweep methodology. Measurements are performed to obtain SS_F curves around the required value of $SS_F|_{k_0} \approx \ln(10)u_T$, from which k_0 is then extracted with the analytical model, for each V_{FG} locally. The numerical model circumvents the need for k_0 by fitting all measurements simultaneously, for each V_{FG} locally.

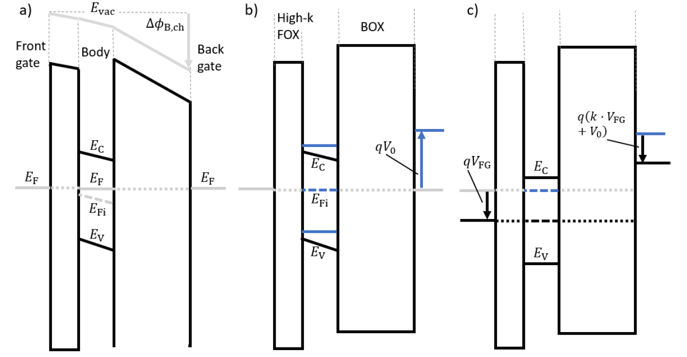

Fig. 3. Band diagram for energy profiling *k*-sweep methodology for an asymmetric UTB SOI MOSFET with back gate work-function difference (a) under thermal equilibrium, (b) with applied offset voltage V_0, and (c) with applied voltages, where $k = k_0$. In this diagram, the device is assumed to be free of interface traps; hence, $k_0 = 1$.

SOI processes, where the front gate has a high-*k* dielectric, as used in this work. For high-*k* FOX layers, the front interface trap density is typically expected to be a decade higher than the back interface trap density [16], but a measured ratio of $D_{it,F}/D_{it,B} \approx 3.3$ was obtained [16]. These experimentally established ratios indicate that conditions (8a) and (8b) can be used to estimate the trap density of the dominantly contributing interface. The last condition (8c) describes a device where the front and back (or buried) oxides are formed in a single step. This is the case for FinFETs where front and back trap densities are actually identical [7], [17]. Also, for UTB SOI devices with SiO_2 as FOX, $D_{it,F} \approx D_{it,B}$ was obtained [18], [19].

If the first condition (8a) is imposed, (6) and (7) can be solved. Then, $SS_F|_{k_0} \approx \ln(10)u_T$ [see (7)], and $k_0 \approx (C_{ox,B} + C_{it,B})/C_{ox,B}$ [see (6)]. The back interface trap density $D_{it,B} = C_{it,B}/q$ can thus be extracted from that gate voltage ratio k where we find the given $SS_F|_{k_0}$. Similarly, we can find $D_{it,F} = C_{it,F}/q$ from $SS_B|_{k_0}$ if the second condition (8b) is imposed.

In the third case (8c), we can additionally assume identical oxide layers ($C_{ox,F} = C_{ox,B}$) because the two gate oxides are created in the same fabrication step. Then, $k_0 = 1$ for all gate voltages, and we can apply the g_m/I_D-method [7]. In case the oxide layers are not identical, or any intermediate conditions are imposed, the system can still be numerically solved, as discussed in Section II-C.

Fig. 2 sketches the parameter extraction procedure, as described earlier. The last step in the procedure is the association of trap energy to the interface states.

Since we extract the interface trap density at $k = k_0$, which implies $\psi_{s,F} = \psi_{s,B}$, this translation step for our quasi-symmetric case is the same as that for the symmetric case with, e.g., FinFET devices [7]

$$E - E_V = \frac{E_G}{2} + q \cdot \psi_{s,F} \tag{9}$$

with E_V being the valence band energy and E_G the bandgap energy.

When $D_{it}(E)$ is nonuniform, as with, e.g., P_b centers, energy profiling yields information on the (chemical) nature of the traps that cause nonideal subthreshold behavior. The energy resolution of the g_m/I_D method is discussed in [7]. In this article, we treat the possibilities to extend this method to asymmetric DG transistors.

C. Separating the Interface Trap Contributions

Various combinations of front and back interface trap densities correspond to the extracted k_0 when using the analytical model. Therefore, only a total interface trap density value can be determined. To distinguish the front and back interface states, it is necessary to create a surface potential difference. This renders (7) inaccurate, as we depart from the condition $k = k_0$. However, one can use (3) instead. Then, an inverse modeling approach can be applied to (1) and (3)–(5). In an iterative process, the front and back interface trap densities are varied until a set of measured subthreshold curves at various *k*-values is best approached. An implementation is sketched in Fig. 2. With the numerical model, a set of n subthreshold swing curves around k_0 is fitted simultaneously. Since the slope of the SS_F versus k curve is additionally considered, the $D_{it,F}$ and $D_{it,B}$ corresponding to the measured device can then be uniquely determined.

In modern UTB SOI processes, the front gate is a metal with a midgap work function ($\Delta\phi_{F,ch} = 0$ eV), and the back gate is a doped silicon well (so $\Delta\phi_{B,ch} \neq \Delta\phi_{F,ch}$). A constant bias between the front and back gates is then necessary to obtain equal surface potentials; hence, $V_{BG} = kV_{FG} + V_0$. From (4) and (5), assuming that $\psi_{s,F} = \psi_{s,B}$, we find $V_0 = \Delta\phi_{B,ch}/q$.

This offset voltage is additionally applied to the back gate for the numerical computation method, and the effect of this is shown in Fig. 3.

III. Methods

Electrical measurements were performed on state-of-the-art 22FDX (R) GlobalFoundries FD-SOI flipped well nMOS transistors with $W/L = 1/1$ μm/μm [20]. The devices have few-nanometer-thin body, FOX and BOX layers, with $t_{BOX}/t_{FOX} \approx 15$. The natural length should be considered for the thick BOX layer to ensure that the long channel approximation holds [21]. All device terminals and the substrate were separately connected.

The measurement setup consists of a Keithley 4200-SCS semiconductor characterization system equipped with 4200-PA

remote preamplifiers and a Suss Microtech PM300 probe station. The wafer temperature was set to 25 °C ± 0.5 °C with an Advanced Temperature Test (ATT) Systems temperature control unit. Measurements were performed at the "quiet" setting.

The drain current I_D was measured as a function of V_{FG} and the coupled $V_{BG} = k \cdot V_{FG}$ with $V_{DS} = 25$ mV. We used $0 \le V_{FG} \le 0.3$ V with a small voltage step size of $\Delta V_{FG} = 0.2$ mV (see [22]).

Because the value of k_0 is not *a priori* known, measurements were performed for a range of k-values. The subthreshold swing was determined for each k-value. The value of k_0 is then found as the k-value, where $SS_F \approx \ln(10)u_T$ (see Fig. 2).

The drain current slope in subthreshold can be rather noisy when obtained using direct differentiation. Therefore, we use regression analysis on the drain current data within a regression window range of $V_{FG} \pm u_T/2$, imposing $I_{D,reg} \propto \exp(V_{FG}/u_T)$ to acquire the slope around V_{FG} [22].

Experimental results from the k-sweep energy profiling method were compared with compact model simulations. For this, the independent multigate BSIM simulation tool [23] was adopted in Promost [24]. The model incorporates the physical parameters of the measured device and contains a single trap density parameter to describe the traps of both interfaces [25], which is varied to obtain the best fit to the measurement data.

Both the analytical and numerical models were tested with Silvaco Atlas [26] finite-element method (FEM) simulations. A 2-D FG/FOX/body/BOX/BG structure was simulated as indicated by the dashed box in Fig. 1, with the same materials and dimensions as the experimental devices. We assumed a constant mobility, $\mu_n = 600$ cm^{2}V^{-1}s^{-1}, and included doping-induced bandgap narrowing in the n-well. The BG was explicitly implemented as n-well for the investigation of the effects of back-gate depletion and an offset voltage (V_0, as per $V_{BG} = k \cdot V_{FG} + V_0$) to compensate for a back-gate work-function difference ($\Delta\phi_{B,ch}$); for the other simulations, the BG was defined as an ideal electrode.

In the FEM simulations, the applied voltages were the same as for the measurements, except that for the former the offset voltage was included for the structure with n-well.

The interface traps were implemented at the FOX/body and body/BOX interfaces with a fixed trap density (assuming a fixed cross section of $\sigma_n = 2.84 \cdot 10^{-15}$ cm^2) at each discrete energy level inside the silicon bandgap. Small trap energy spacings of 5.66 meV ensured a quasi-continuum of traps.

The FEM simulations were fitted with the numerical model at each V_{FG} using a MATLAB *fit*()-algorithm, with $D_{it,F}$ and $D_{it,B}$ as variable fitting parameters, as shown in Fig. 2.

IV. Results

A. Experimental Results

An exemplary measured drain current is shown in Fig. 4. The inset shows the drain current for an extended front gate voltage range. The subthreshold swing with respect to the front gate was then computed, and from that, k_0 was extracted, as visualized in Fig. 5. As shown in Fig. 5(b), k_0 could only be extracted for $V_{FG} \le 0.21$ V (vertical dotted line) since the measured subthreshold swing increases beyond the desired value for higher front gate voltages.

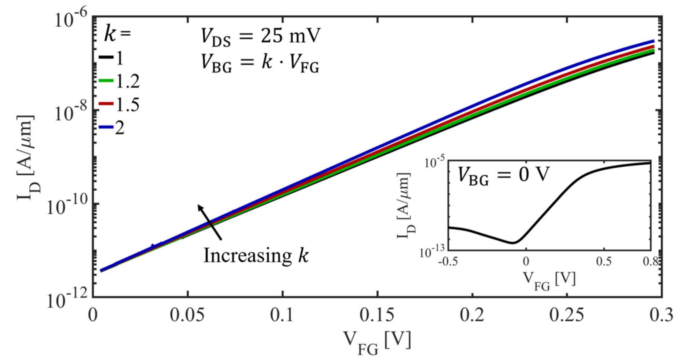

Fig. 4. Drain current per unit width as a function of the front gate voltage for $k = 1, 1.2, 1.5, 2$, and $V_{DS} = 25$ mV within the subthreshold regime. Inset: the curve for $k = 0$ ($V_{BG} = 0$ V) over an extended voltage range.

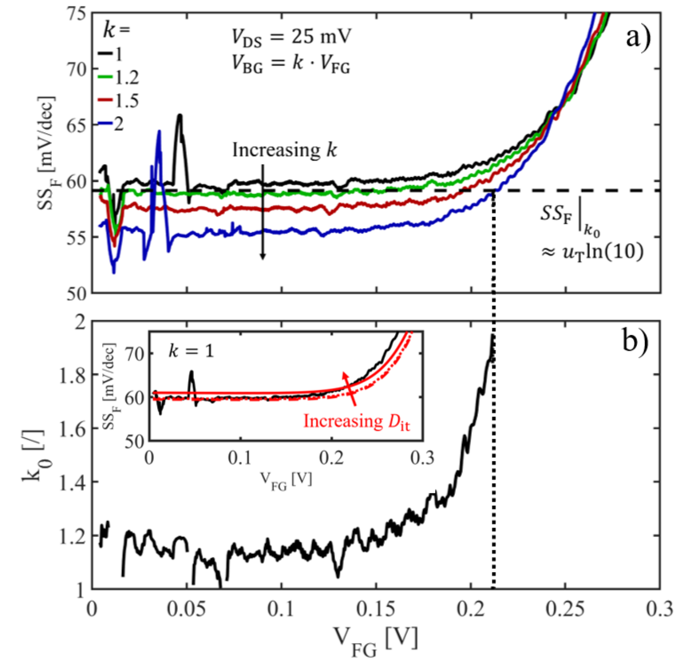

Fig. 5. (a) SS_F for $k = 1, 1.2, 1.5, 2$, and (b) extracted k_0, as a function of the front gate voltage, for $V_{DS} = 25$ mV. $SS_F|_{k_0} \approx u_T\ln(10)$ (dashed line), and the maximum interpolation voltages for extracting k_0 (dotted line) are indicated. Inset: the measurement (black) compared with BSIM simulations (red) for $k = 1$ with $D_{it} = 6.2 \cdot 10^{10}$ cm^{-2}eV^{-1} and $D_{it} = 4.4 \cdot 10^{11}$ cm^{-2}eV^{-1}. The peak around $V_{FG} \approx 0.04$ V in (a) is due to a calibration artifact of the Keithley measurement system.

The (front or back) interface trap density was then extracted from k_0, as shown in Fig. 6. A D_{it} value of approximately $2 \cdot 10^{11}$ cm^{-2}eV^{-1} ($V_{FG} < 0.2$ V) is obtained. For $V_{FG} \ge 0.2$ V, an apparent increase in interface traps arises because the free charge carriers can no longer be ignored [7]. Then, (1) no longer holds, which is the reason for the limited k_0 extraction range.

The quantitative results for $D_{it,F}$ and $D_{it,B}$ should ideally be equal. The found difference provides a measure of the interpolation error for obtaining k_0 from $SS_F|_{k_0}$. The effective D_{it}-value of $2 \cdot 10^{11}$ cm^{-2}eV^{-1} is similar for both conditions [see (8a) or (8b)]; hence, the interpolation error is acceptable

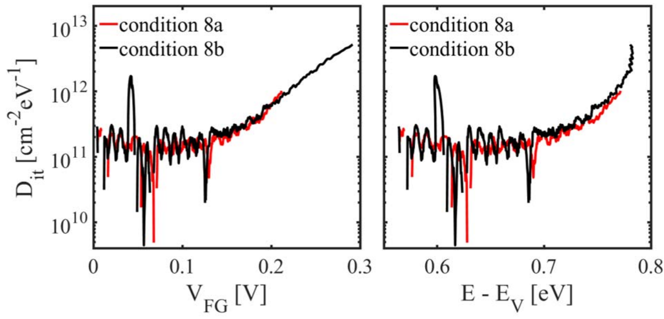

Fig. 6. Front and back interface trap densities per unit area per energy as a function of the front gate voltage (left) and energy (right). For each trap density, the other interface is assumed without traps [conditions (8a) and (8b)].

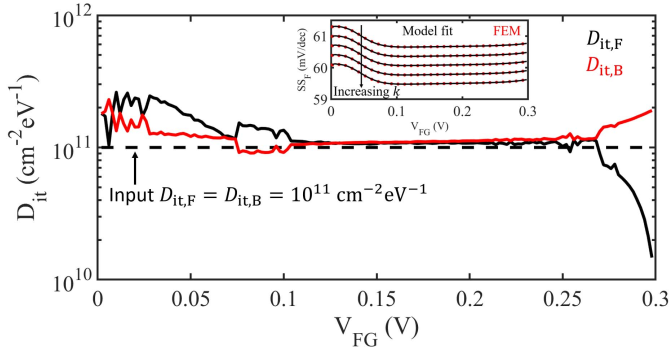

Fig. 7. Best-fit extracted trap density obtained from the model (solid lines), as well as the (actual) trap density used as input for the FEM simulations (dashed line). The inset shows SS_F as a function of the front gate voltage for different k's, for the FEM simulations (red) and the model fitted to this (black). The shown results are for an asymmetric device with $t_{BOX}/t_{FOX} \approx 15$. A symmetric interface trap distribution of $D_{it,F} = D_{it,B} = 10^{11}$ cm^{-2}eV^{-1} is used. We used $\Delta\phi_{B,ch} = 0$ eV.

in this case. BSIM simulations indicate a similar effective D_{it}-value (see Fig. 5(b), inset).

B. Finite-Element Modeling Results

The FEM simulation results for a symmetric trap distribution ($D_{it,F} = D_{it,B} = 10^{11}$ cm^{-2}eV^{-1}) and the results for the numerical model fitted to those FEM simulations are shown in Fig. 7. Especially in the range of $0.1 < V_{FG} < 0.25$ V the numerical model can be used to accurately extract the trap densities at both interfaces from the FEM simulations. For lower front gate voltages, the discrete trap implementation used in the FEM simulations limits the output accuracy. Perhaps a continuous trap implementation resolves this issue [27]. For higher front gate voltages, the apparent conduction band edge reduces the accuracy.

To determine how well the trap densities of the front and back interfaces can be separated, an asymmetric interface trap distribution ($D_{it,F} = 2.5 \cdot 10^{11}$ cm^{-2}eV^{-1} and $D_{it,B} = 0$ cm^{-2}eV^{-1}) was considered. The trap densities extracted with the model are shown in Fig. 8. Consistent with the chosen input, the extracted front interface trap density is higher than the back interface trap density across the figure, but a minor fraction of the traps is erroneously linked to the back interface.

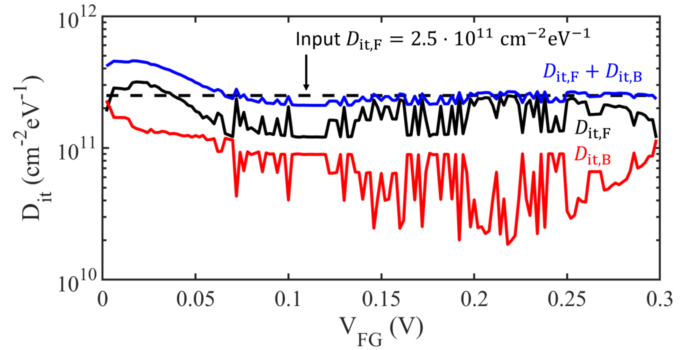

Fig. 8. Best-fit extracted interface trap density obtained from the model against the FEM simulation input. The total trap density ($D_{it,F} + D_{it,B}$) and the trap density used as input for the FEM simulations are also shown. The results are for an asymmetric device with $t_{BOX}/t_{FOX} \approx 15$. An asymmetric interface trap distribution of $D_{it,F} = 2.5 \cdot 10^{11}$ cm^{-2}eV^{-1} and $D_{it,B} = 0$ cm^{-2}eV^{-1} is used. We used $\Delta\phi_{B,ch} = 0$ eV.

Thus, in this case, the technique correctly identifies which of the two interfaces has the higher trap density. While the total trap density can be accurately extracted, an error of about 20% is observed for allocating the traps to the correct interface, caused by the coupling between the two surface potentials.

The general limit of detection for trap densities is 10^{10} cm^{-2}eV^{-1} determined by fitting FEM simulations without traps. This corresponds well to the lower limit reported in [22]. An input delta-peak trap density could not be translated back to the correct energy level due to the thermal noise, as was previously reported [7].

C. Impact of Inherent Nonidealities

With FEM simulations, we determined the impact of nonidealities in the k-sweep methodology models.

Starting with a symmetric device, increasing the BOX layer thickness reduces electrostatic control of the BG and with it the influence of k. Visually, for increasing the BOX layer thickness, $SS_F(k)$ would rotate counterclockwise with $k = k_0$ as the pivot point. This is correctly captured by the analytical and numerical models provided in this work.

Both models are valid in the limit of $N_{well} \rightarrow \infty$ and do not account for back-gate depletion since C_B in (4) and (5) does not contain any n-well doping-dependent term. By decreasing the doping concentration, N_{well}, the influence of k on the subthreshold swing is reduced, as shown in Fig. 9. A similar counterclockwise rotation as for an increasing BOX layer thickness is observed. Therefore, the depletion effect is equivalent to the effect of increasing the BOX layer thickness for k closely around k_0, and the observed trend was found to be similar for all front gate voltages. We can thus conclude that the depletion width of the n-well, $w_{depletion}$, can be regarded as an effective increase in the BOX layer thickness, i.e., $t_{BOX,eff} = t_{BOX} + (\varepsilon_{ox}/\varepsilon_{si}) \cdot w_{depletion}$.

The FEM simulations include inversion charge in the channel and thus more accurately describe the excess traps near the conduction band edge than the model [see (1)–(3)].

Finally, when n-well depletion effects are included in the FEM simulations, we find that a large portion of the traps

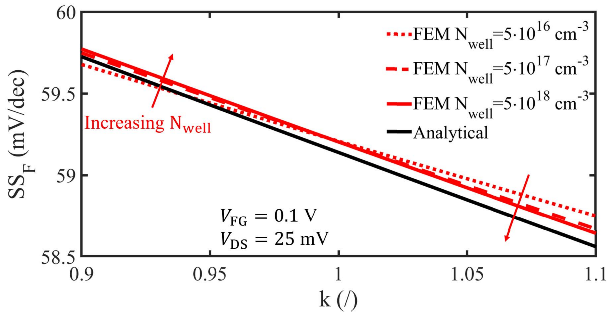

Fig. 9. SS_F as a function of k for $V_{FG} = 0.1$ V. The SS_F is shown for an asymmetric device with $t_{BOX}/t_{FOX} \approx 15$ as computed with the analytical model (black) and from FEM simulations (red). The FEM simulations include an n-type doped silicon well as a back gate electrode with various doping concentrations (N_{well}). The device contains no interface traps.

may be incorrectly attributed to the back interface if these effects are not accounted for in the model.

V. Conclusion

By applying the methodology developed in this work, the trap density at the dominantly contributing interface can be estimated from the subthreshold current as a function of the activation energy for DG FD-SOI transistors. For our 22FDX (R) GlobalFoundries nMOS transistors, an average interface trap density of $2 \cdot 10^{11}$ cm^{-2}eV^{-1} was obtained. Separating the trap densities of the front and back interfaces is feasible, but not very accurate. A trap allocation error of 20% was obtained from fitting FEM simulations with the developed numerical model, neglecting back gate depletion effects and using constant mobility. In practice, effects of depletion, field-dependent mobility, and variations in, e.g., the front and buried oxide thickness would further increase this allocation error. The limit of detection for the interface trap density extraction is 10^{10} cm^{-2}eV^{-1}.

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