An Over 120 dB Single Exposure Wide Dynamic Range CMOS Image Sensor With Two-Stage Lateral Overflow Integration Capacitor

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***Abstract*— This article presents a prototype linear response single exposure CMOS image sensor with two-stage lateral overflow integration capacitors (LOFIC) exhibiting over the 120-dB dynamic range (DR) with 11.4 Me^- full well capacity (FWC) and maximum signal-to-noise ratio (SNR) of 70 dB. The measured SNR at all switching points were over 35 dB thanks to the proposed two-stage LOFIC.**

***Index Terms*— CMOS image sensor (CIS), lateral overflow integration capacitor (LOFIC), signal-to-noise ratio (SNR), wide dynamic range (WDR).**

I. Introduction

SENSING technologies using CMOS image sensors (CISs) have been utilized in many applications, such as machine vision, automotive, analytical instruments, and absorption imaging. In such application areas, a wider dynamic range (WDR) performance without signal-to-noise ratio (SNR) drop at the signal switching point is desired for improving sensing accuracy over the wide range of illumination conditions. In addition, suppression of motion blur is important when capturing moving objects [1].

Several WDR technologies have been reported so far; multiple exposure [2]–[10], dual photodiode (Dual PD) [11]–[14], dual conversion gain (DCG) [15]–[18], lateral overflow integration capacitors (LOFICs) [19]–[26], and combination of the above [1], [27]–[31]. The multiple exposure approach captures a few images with different exposure periods. The approach with a combination of PDs captures an image with multiple PDs with different size or light sensitivity in a single exposure. The DCG approach changes conversion gain (CG) by controlling a switch connected to a capacitor and floating diffusion (FD) in a pixel during the horizontal blanking period. The LOFIC approach accumulates overflow-electrons from PD and FD capacitors and reads out signals with different sensitivity in a single exposure. This approach allows the independent design of CG and full well capacity (FWC), resulting about 100 dB single exposure DR [19]–[20]. Consequently, the maximum SNR on the high light side can be increased without decreasing sensitivity. In addition, single PD architecture is to be beneficial to maintain the optical performance when applying the image sensors to the various optical configurations.

The purpose of this article is to demonstrate the principle of the two-stage LOFIC for further improvement of the DR with high SNR at signal switching points [32]. A 16-μm pixel pitch prototype CIS with two-stage LOFIC introducing a high capacitance density trench MOS capacitor as LOFIC was fabricated.

Recently, an over 120-dB DR CIS introducing a 1.6 pF lateral overflow integration trench capacitor (LOFITreC) to improve both maximum SNR and SNR at signal switching point was reported [26].

In this article, we additionally discuss in detail the two-stage LOFIC and its potential tuning procedure, the SNR characteristics, and the prospects of pixel shrinking. Section II shows key technologies of this work, Section III shows measurement results, and the conclusion is in Section IV.

II. Developed CIS

A. Circuit Architecture and Operation

Fig. 1 shows the circuit block diagram of the developed CIS. The pixel consists of a pinned PD, a transfer gate (T), an FD, a source follower driver (SF), a select switch (X), a first overflow switch (S1), a LOFIC1, a second overflow switch (S2), a LOFIC2, and a reset gate (R). In this work, the 67-fF LOFIC1 and 1.5-pF LOFIC2 are integrated adjacent to the PD. The values of the capacitances are designed to achieve sufficient SNR at signal switching points. The developed prototype chip has three pairs of parallel analog outputs and they are converted by differential analog-to-digital converters (ADCs) outside the chip. When column-parallel ADCs are introduced, their suitable circuit architecture needs to be examined.

Figs. 2 and 3 show the operation timing diagram and the potential diagram of the two-stage LOFIC operation, respectively. After the PD reset, a reset signal for the highest FWC signal S3 converted at FD + LOFIC1 + LOFIC2 is read out

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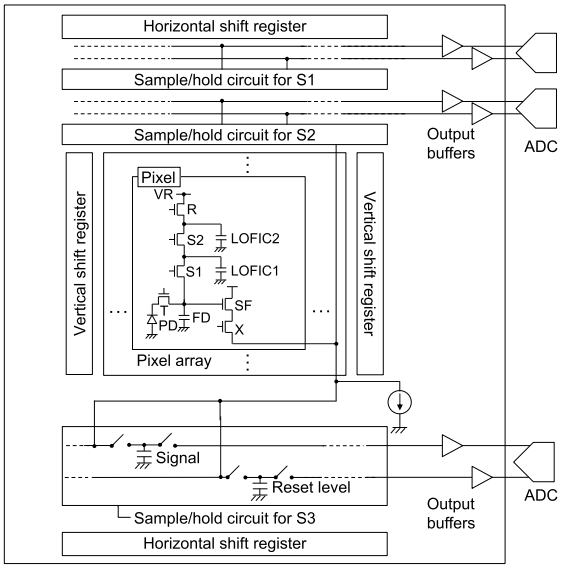

Fig. 1. Circuit block diagram of the developed CIS with two-stage LOFIC.

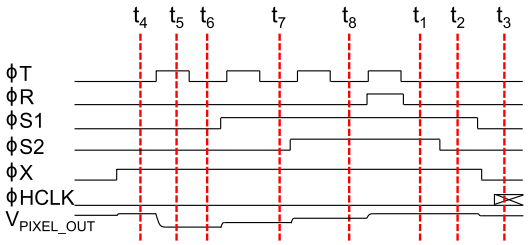

Fig. 2. Operation timing diagrams of two-stage LOFIC operation.

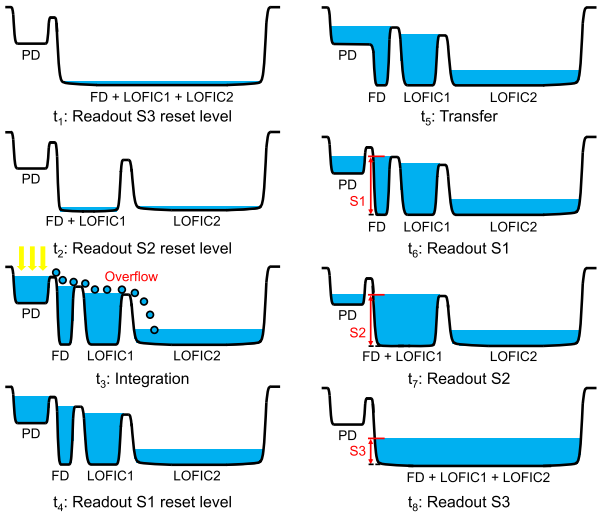

Fig. 3. Potential diagrams of a two-stage LOFIC operation, illustrating a high illumination condition.

at t1. A reset signal for high FWC signal S2 converted at FD + LOFIC1 is read out at t2. When high-intensity light is irradiated to the pixel during the integration period (t3), overflow photoelectrons from PD and FD are accumulated in the LOFIC1 and overflow photoelectrons from LOFIC1 are accumulated in the LOFIC2. A reset signal for high sensitivity signal S1 converted at FD is read out at t4. Photoelectrons accumulated in the PD are transferred to the FD at t5. A high

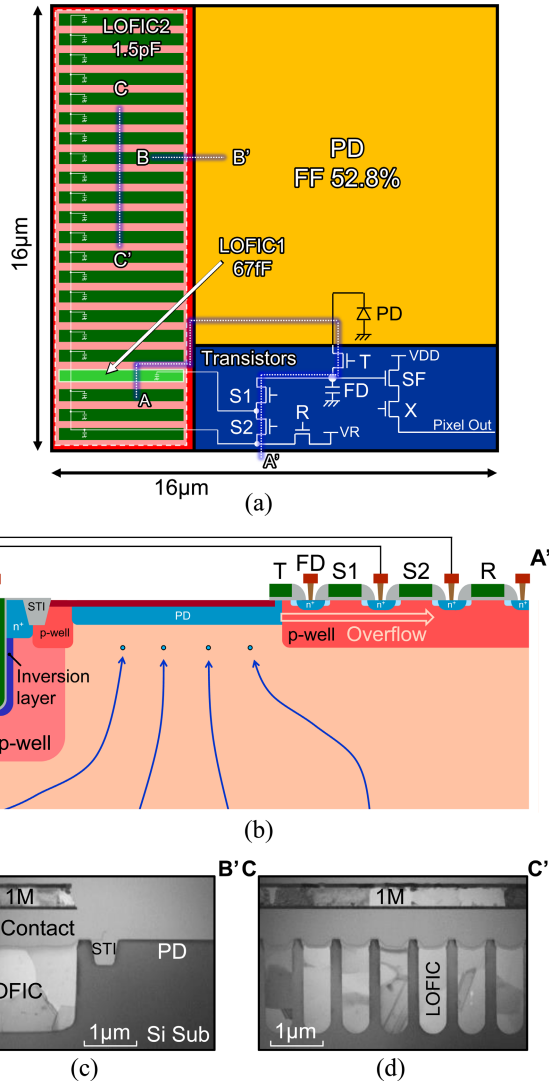

Fig. 4. (a) Pixel layout and (b) pixel cross-sectional diagram of line A-A', and cross-sectional TEM images of (c) line B-B', and (d) line C-C'.

sensitivity signal converted at small capacitance FD (S1) at t6, a high FWC signal converted at FD+LOFIC1 (S2) at t7 and a highest FWC signal converted at FD + LOFIC1 + LOFIC2 (S3) at t8 are read out to achieve WDR under a single exposure.

Fig. 4(a) shows the layout diagram of the 16-μm pitch pixel of the prototype CIS developed in this work and 4(b) shows the pixel cross-sectional diagram. The trench capacitors were integrated inside each pixel as LOFICs to achieve high FWC and a sufficiently high fill factor (FF). The TEM images of LOFIC are shown in Fig. 4(c) and (d). A deep p-well (DPW) was formed around the LOFIC in order to form a potential barrier between the inversion layer of LOFIC and the buried n-type layer of pinned PD. The concentration of DPW was optimized to obtain a uniform capacitance of LOFIC across the signal range. To suppress the leakage current of the charge integration node of LOFIC, overflown-photoelectrons from the PD and FD are accumulated at the n^+-doped poly-Si buried electrode. The inversion layer induced at the Si substrate side interface and n^+ layer are connected to the ground.

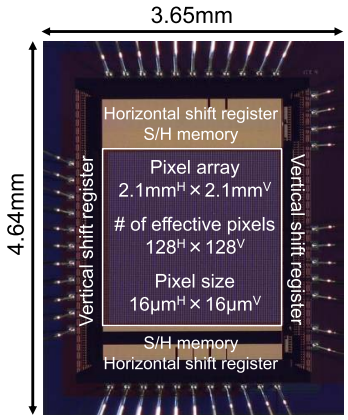

Fig. 5. Micrograph of the developed CIS chip.

B. Chip Fabrication

The developed CIS was fabricated by using a 0.18-μm 1-Poly-Si 5-Metal layer CIS technology with a 20-μm thick p-epitaxial layer on an n-type Si substrate. The chip size is 3.65 mm^H × 4.64 mm^V and the effective pixel array size is 2.05 mm^H × 2.05 mm^V. A 3.3-V power supply voltage is employed.

Fig. 5 shows the micrograph of the fabricated chip with 128^H× 128^V effective pixels. The number of pixels is easily extendable under the same design.

III. Measurement Results

Figs. 6 and 7 show the potential diagrams for each of the voltage levels of pixel transistors and the measured dependence of the light signal on voltage levels of pixel transistors along the overflow path, respectively. The objective of this measurement is to find the potential setting to obtain a stable and sufficiently high saturation of each signal and to form an overflow path so that all photoelectrons are to be accumulated during the integration period simultaneously. V_{FD} is the input-referred FD voltage for reading out S1, S2, and S3. V_{TL}, V_{S1L}, and V_{S2L} are the voltage levels of T, S1, and S2 during the integration period shown in the top figure of Fig. 6 (Definition) and on the x-axis in Fig. 7, respectively. The vertical axis of Fig. 6 indicates the potential for electrons. Since photoelectrons have a negative charge, as the number of photoelectrons increases, the V_{FD} voltage becomes the lower. Fig. 6(A"), (A'), and (A) shows the typical choice of potential condition for determining the voltage settings of the pixel transistors. Both formation of overflow-path and sufficient saturation of each signal are achieved in these conditions. The potential tuning of the two-stage LOFIC is carried out by following three steps: first forming overflow path from PD to FD by tuning V_{TL} shown in Fig. 7(a), from FD to LOFIC1 by V_{S1L} in Fig. 7(b), and from LOFIC1 to LOFIC2 by V_{S2L} in Fig. 7(c). The measurement procedure is as follows: first setting the target voltage to get the highest saturation level, and setting the light level to an intensity that saturates the target signal and then, sweeping the target voltage. In Fig. 7(a), the V_{TL} was first set to −1.0 V and the light level was set to saturate signal S1, and then the V_{TL} was swept to measure

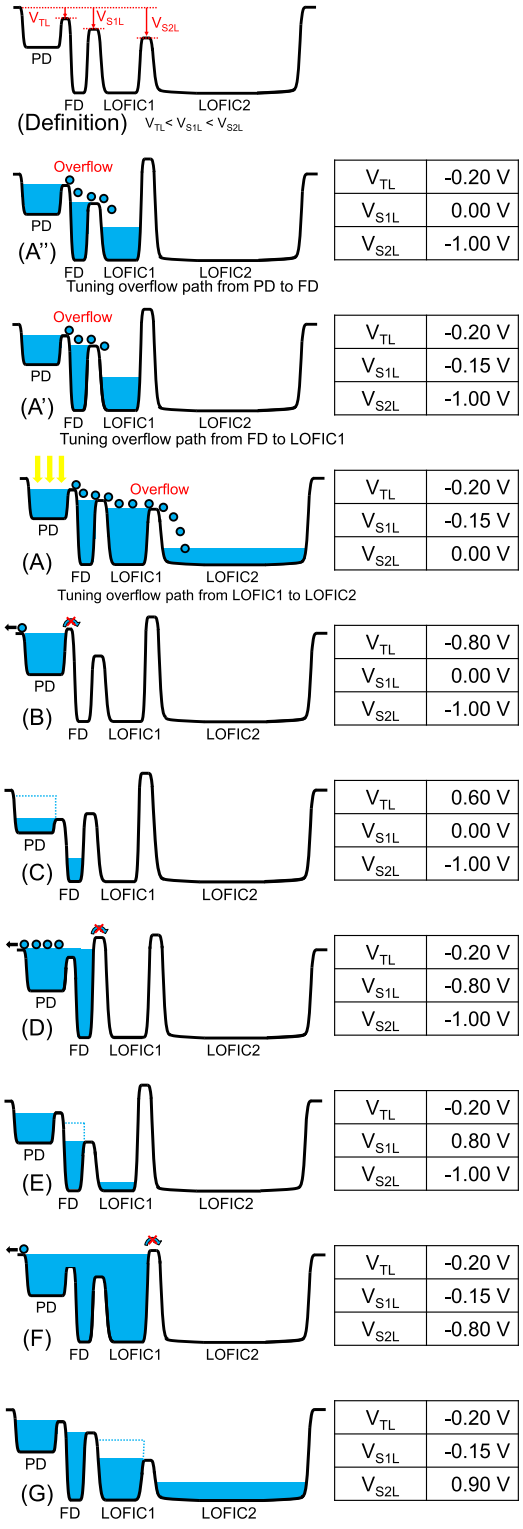

Fig. 6. Potential diagrams for each of the voltage levels of pixel transistors shown in Fig. 7, (A)–(G).

the V_{FD} under the same light conditions. Fig. 6(A") shows the typical choice of the potential condition. Fig. 6(B) is in the condition that the potential barrier of the T transistor is too high to form an overflow path. Fig. 6(C) is in the condition that saturation of PD is reduced because the potential barrier of the T transistor is too low. This condition leads to the reduction

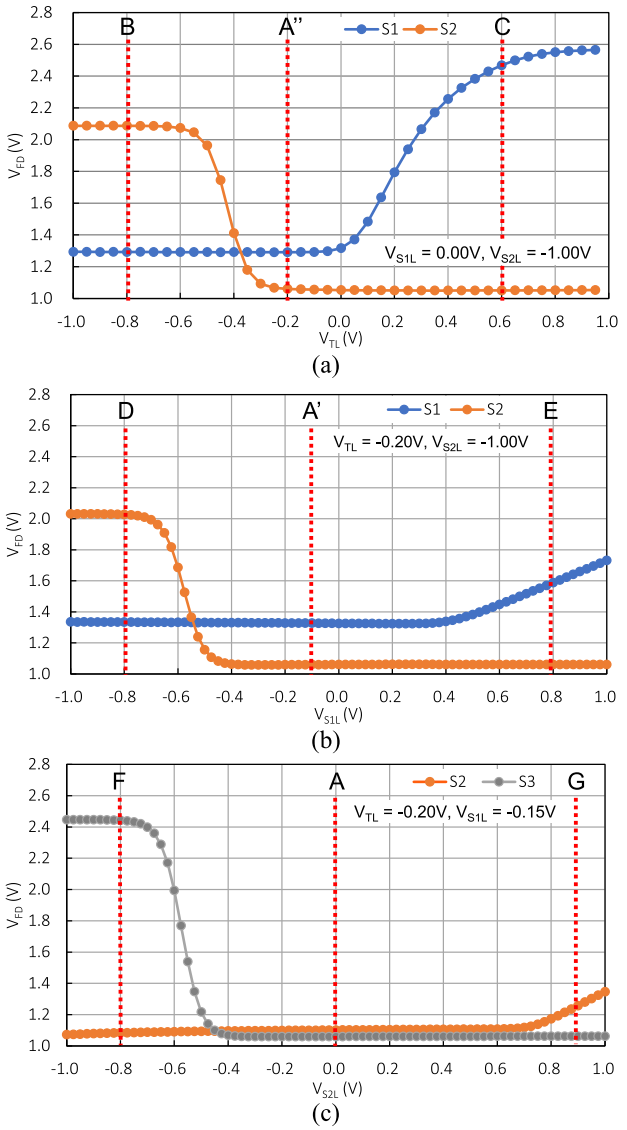

Fig. 7. (a)–(c) Measured dependence of the light signal on the voltage levels of pixel transistors along the overflow path in order to describe the potential tuning procedure of the two-stage LOFIC.

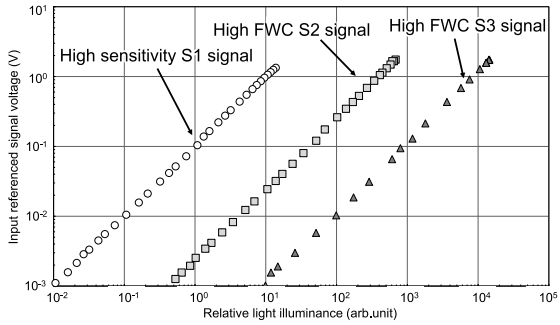

Fig. 8. Measured photoelectric conversion characteristics.

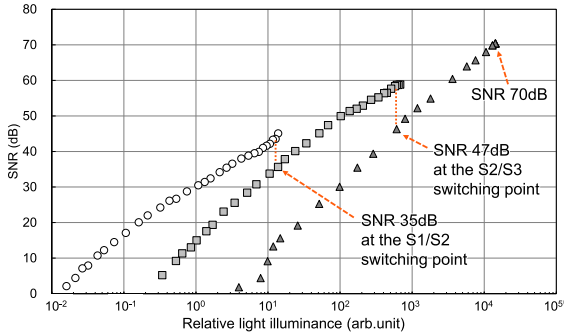

Fig. 9. Measured SNR characteristics.

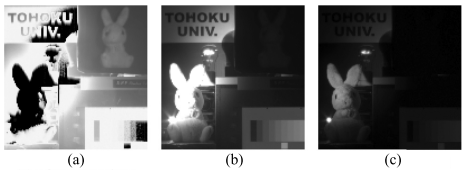

Fig. 10. Sample images by (a) S1, (b) S2 and (c) S3 signals captured at 285 fps with F# 4.0 lens. (a) High sensitivity S1. (b) High saturation S2. (c) High saturation S3.

of SNR at the signal switching points. In Fig. 7(b), the V_{S1L} was swept. Fig. 6(A') shows the typical choice of the potential condition. Fig. 6(D) is in the condition that the potential barrier of the S1 transistor is too high to form an overflow path. Fig. 6(E) is in the condition that the saturation of FD is reduced because the potential barrier of the S1 transistor is too low. In Fig. 7(c), the V_{S2L} was swept. Fig. 6(A) shows a typical choice of potential condition. Fig. 6(F) is in the condition that the potential barrier of the S2 transistor is too high to form an overflow path. Fig. 6(G) is in the condition that the saturation of LOFIC1 is reduced because the potential barrier of the S2 transistor is too low. From the results, V_{TL}, V_{S1L}, and V_{S2L} were set to −0.20, −0.15, and 0.00 V, respectively.

Fig. 8 shows the measured photoelectric conversion characteristics of the developed CIS. An over 120-dB WDR with linear response was obtained by S1, S2, and S3 signals under single exposure. The FWC of S1, S2, and S3 were 17.8 ke^-, 509 ke^-, and 11.4Me^-. And the spatial efficiency of the FWC for S1, S2, and S3 signals were 6.95×10^1, 1.99×10^3, and 4.45×10^4 $e^-/\mu m^2$, respectively. Fig. 9 shows the measured SNR characteristics of the developed CIS. A maximum SNR of 70 dB was achieved. The SNR at S1/S2 and S2/S3 switching points were 35 and 47 dB, respectively. The high SNR at two switching points was successfully achieved by the introduction of two-stage LOFIC. The readout noise of the S1 signal was 3.5 e^-_{rms}, it can be reduced by optimizing column readout circuit and increasing the CG of FD [33]. The dark current shot noise of the LOFIC1 at 7 fps was less than 10% of the thermal (kTC) noise of the LOFIC1 at room temperature. SNR at the signal switching point is not affected by introducing a trench capacitor for LOFIC.

Fig. 10 shows the sample images of a light bulb, a grayscale chart, printed paper, and two stuffed animals captured at 285 fps with F# 4.0 lens. The stuffed animal on the left was illuminated with high intensity lights from both its front and back to simulate the gray phenomenon. The other stuffed animal on the upper right was placed in a dark box. Fig. 10(a)–(c)

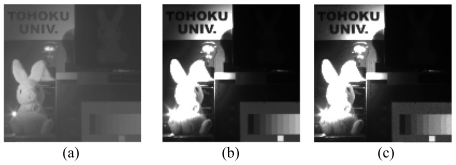

Fig. 11. Synthesized WDR images. (a) S1 + S2 + S3 $y = 0.2$. (b) S1 + S2 + S3 $\gamma = 1$. (c) S1 + S2 + S3 $\gamma = 1$.

TABLE I
PERFORMANCE SUMMARY OF THE DEVELOPED CIS

Process technology		0.18μm 1-poly-Si 5-Metal CMOS with pinned PD
Power supply voltage		3.3V
Die size		$3.65mm^H \times 4.64mm^V$
# of effective pixels		$128^H \times 128^V$
Pixel size		$16\mu m^H \times 16\mu m^V$
Fill factor		52.8%
Maximum frame rate		685fps @20MHz
Capacitance	FD	2.1fF
	LOFITreC1	67fF
	LOFITreC2	1.5pF
FWC [Spatial Efficiency]	High sensitivity S1	$17.8ke^-$ ($69.5e^-/\mu m^2$)
	High saturation S2	$509ke^-$ ($1.99ke^-/\mu m^2$)
	High saturation S3	$11.4Me^-$ ($44.5ke^-/\mu m^2$)
SNR	S1/S2 switching point	35dB
	S2/S3 switching point	47dB
	Maximum S3	70dB
Readout noise S1		3.5 e^-_{rms}
Dynamic range		>120dB
Spectral sensitivity range		200nm-1100nm

shows the capture of S1, S2, and S3 signals, respectively. The S1 signal captured the upper right stuffed animal under low light conditions. The S2 signal captured the printed paper on the back and the grayscale chart under high light conditions. The S3 signal captured the bulb filament and the stuffed animal on the left under very high light conditions. The results show that the developed CIS exhibits a single exposure WDR performance.

Fig. 11 shows the synthesized images of the captured sample images. Fig. 11(a) and (b) are composed of S1, S2, and S3 signals with gamma values of 0.2 and 1.0, respectively. Fig. 11(c) is composed of only S1 and S3. The SNR at the signal switching point of Fig. 11(b) and (c) are over 35 dB and about 16 dB, respectively. The image quality of Fig. 11(b) is higher than that of Fig. 11(c) especially in the medium-light region near the grayscale chart. This result shows that the SNR at the signal switching points has a significant effect on WDR image quality.

The performances of the developed CIS are summarized in Table I.

Fig. 12 shows the SNR at the switching point as a function of the DR, compared to other linear response CISs. For the

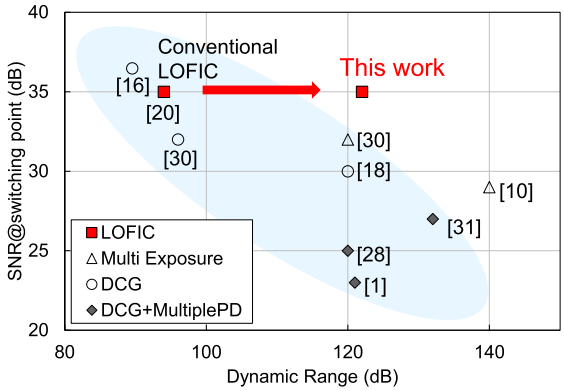

Fig. 12. SNR at switching point as a function of the DR, compared to other linear response CISs.

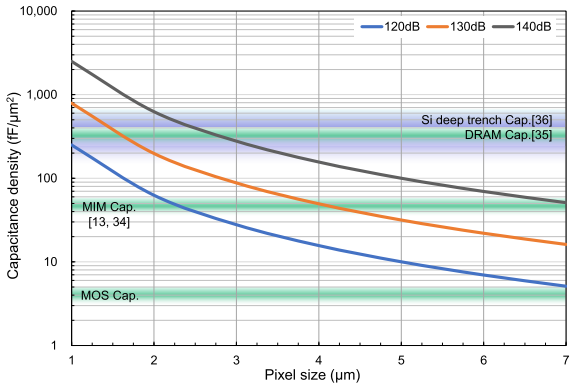

Fig. 13. Relationship between pixel size and capacitance density.

developed prototype chip, a high SNR at the switching point of 35 dB and over 120-dB DR were achieved by a single exposure.

The pixel pitch can be scaled while maintaining its high spatial efficiency of FWC, thanks to the high-density capacitor used for LOFIC. In addition, backside illumination and stacking technologies can increase the spatial efficiency of FWC further even if the pixel pitch is decreased. Fig. 13 shows the calculated relationship between pixel size and capacitance density required for each DR. Here, the calculation was carried out with the conditions that the capacitance area ratio is 80% of all the pixel area, the number of input-referred noise is 1 e^-_{rms}, and the signal voltage range at FD is 0.8 V. Typical MOS capacitors have a capacitance density of about 5 fF/μm^2. High-k dielectric MIM capacitors with a capacitance density of about 50 fF/μm^2 [13], [34], and dynamic random access memory (DRAM) capacitors with a capacitance density of about 350 fF/μm^2 [35] have been reported to be useful for CIS pixels. A versatile high capacitance density and highly reliable Si deep trench capacitors with over 230 fF/μm^2 and 9.0 V break down voltage are recently developed [36]. In addition, a 700 fF/μm^2 Si deep trench capacitor was also developed [37]. By combining these capacitors with 3-D stacking technology, it is highly possible to achieve a DR of over 120 dB even for a few microns' pixel pitch using the proposed two-stage LOFIC architecture.

IV. Conclusion

This article reported a two-stage LOFIC WDR CIS. The developed CIS achieved 11.4 Me^- FWC, over 120-dB DR and over 35-dB SNR at signal switching points. Furthermore, the two-stage LOFIC CIS can achieve over 120-dB WDR on a few microns pixel pitch by combining high capacitance density capacitors, stacking technology, and back-side illumination. The developed two-stage LOFIC CIS is promising for high contrast sensing application in many fields such as machine vision, automotive, analytical instruments, and absorption imaging fields.

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