Signal and Thermal Integrity Analysis of 3-D Stacked Resistive Random Access Memories

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***Abstract*— In this article, a 3-D electrothermal numerical model is used to perform the signal and thermal integrity analysis of 3-D stacked Resistive-switching random access memory (RRAM) arrays. Two main issues are found: voltage drop along the interconnects and thermal crosstalk between the memory cells. Possible solutions to these issues are here thoroughly investigated, based either on new biasing schemes or new materials. Especially, conventional nickel bars are replaced by interconnects made by copper (Cu) and carbon nanotubes (CNTs), whose electrical and thermal parameters are here described using physically based models. The analysis is performed on a $5 \times 5 \times 5$ array, under a real case of a RESET switching, which is the worst case scenario from the electrothermal point of view. Simulation results show that the use of CNTs reduces the voltage drop in both word and bitline (BL) interconnects, thermal crosstalk, and the maximum working temperature; hence, it mitigates many of the crucial issues in the roadmap for the large-scale monolithic 3-D RRAM integration.**

***Index Terms*— 3-D monolithic integration, carbon nanotubes (CNTs), electrothermal effects, resistive-switching random access memories (RRAM), signal integrity, thermal integrity.**

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I. Introduction

ONE of the most promising innovative memory concepts is given by the so-called resistive-switching random access memories (RRAMs) that show outstanding performance in terms of speed and power consumption compared with the existing technologies [1]. However, closely packed arrays of RRAM suffer from reliability issues related to phenomena, such as undesired sneak currents and write disturbance problems [2]. To address these issues and improve the read/write margin, new architectural solutions have been proposed, such as the complementary resistive switching [3], [4], the one selector-one resistor [5]–[7], or the one diode-one resistor (1D1R) [8]–[10].

The reference RRAM cell analyzed in this article belongs to the latter category: it is assumed as the unit cell [X-point, Fig. 1(b)] for a 3-D stacked arrays of RRAMs [see Fig. 1(a)].

The device in Fig. 1(b) is inserted between two nickel electrodes: the so-called word line (WL) (associated with the memory signal) and bitline (BL) (used as the ground reference). A unipolar RRAM switching device is given in Fig. 1(b) by the Ni/HfO_2/Pt stack, where a Ni^+ conductive filament (CF) is formed in the HfO_2 region between the top Ni and the bottom Pt electrodes. In the absence of the CF, the RRAM is at the high resistive state (HRS), whereas, once the CF is formed, it switches to the low-resistive state (LRS). The resistive switching behavior of Ni/HfO2/Pt device is widely accepted to obtain the formation/rupture of Ni CF. The reset current is $1.7 \times 10 - 4$ A. A Pt/TiO_2/Ti diode is added to limit the sneaky current during its read/write process, as pointed out before.

The 3-D architecture in Fig. 1(a) has been devoted a large interest in the literature since it naturally enables monolithic integration [11]. It was reported that the crosstalk effect in integrated RRAMs is more sensitive to the feature size spacing, interconnects, and CF widths, rather than the type/mode of device operation [12]. A larger spacing can suppress the crosstalk. However, this results in a smaller storage density. Hence, there should be a tradeoff between scalability and stability of the RRAM integration. On the other hand, the aggressive downscaling of the whole array dimensions and the wire

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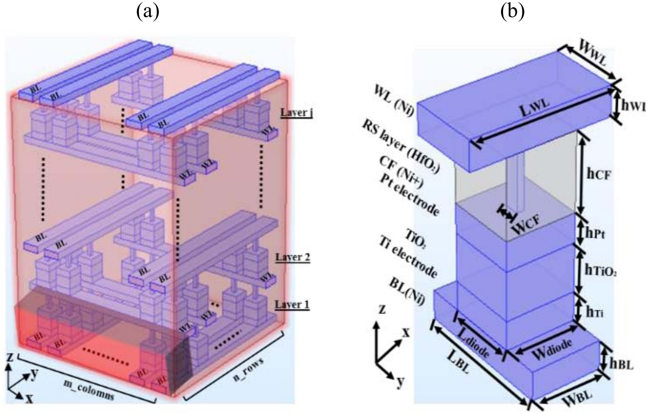

Fig. 1. (a) 3-D crossbar structure made by 1D-1R RRAM cells. (b) 1D-1R cell as the X-point RRAM building block.

widths result in major issues. For instance, the resistance of the WL and BL interconnects brings extra latency and energy consumption and causes voltage drop along the line [13]. The voltage drop significantly affects the signal integrity, by altering the requested level of voltage for reliable SET and RESET switching. To face this issue, the bias voltage applied to the WL could be increased, but this results in increasing power demand and increasing Joule dissipation, hence increasing temperature. Other proposed solutions are based on advanced bias schemes, such as, for instance, the 1/3 bias scheme that enables a larger read margin or the 1/2 one that leads to a lower power consumption [14], [15]. However, signal integrity analysis disregarded the coupled electrothermal effects. Indeed, studying the thermal behavior of the RRAM structure is important not only for studying thermal integrity but also for its impact on electrical performance [16], [17].

In this article, a full 3-D electrothermal numerical model is used to analyze the signal and thermal integrity of 3-D stacked RRAM arrays and study solutions to the above-mentioned issues. In this multiphysics model (described in Section II), the electrical power dissipation is the heat source of the thermal problem, and temperature-dependent electrical parameters are considered into the electrical one. In [18] and [19], the authors have already demonstrated that issues such as voltage drop and temperature rise may appear in 3-D RRAM x-bar structures. In this article, a more detailed signal and thermal integrity analysis is provided for a large ($5 \times 5 \times 5$) structure, including the electrical effects of the thermal crosstalk. In addition, possible mitigation solutions are investigated, such as the use of different bias schemes and/or the use of novel nanomaterials as interconnects.

Compared with the existing approaches in the literature, where the electrothermal analysis is carried out by checking the steady-state response after the application of a step-voltage bias [19], in this article, a more realistic condition is analyzed, where the voltage waveform is a train of pulses, as shown in Section II.

Another novel contribution of this article is the study of the array performance when new materials are adopted to realize the bars to be used for BL/WL, conventionally made by nickel. Toward this end, a conventional material (copper) and novel nanomaterial carbon nanotubes (CNTs) are considered.

The case study analyzed here (in Section III) is a $5 \times 5 \times 5$ RRAM crossbar structure under the RESET process: new biasing solutions and/or material replacing are discussed.

II. Electrothermal Model of the RRAM Array

The thermal behavior of the structures in Fig. 1 (both the unit cell and the whole array) is obtained by solving the following 3-D Fourier heat flow equation in each of the material regions:

$$\rho(T)C_P(T)\frac{\partial T(t)}{\partial t} = \nabla\kappa(T)\nabla T(t) + F(T) \qquad (1)$$

where $\kappa(T), \rho(T)$, and $C_P(T)$ are the temperature (T)-dependent thermal conductivity, mass density, and specific heat of the material in the considered region, respectively. $F(T)$ describes the heat production that is assumed to be only related to the Joule dissipation in the conducting regions. Therefore, $F(T)$ depends on the solution of the electrical problem (Poisson equation) that provides the potential distribution υ in the same region, $F(T) = \sigma(T)|\nabla\upsilon(t)|^2$, with $\sigma(T)$ being the temperature-dependent electrical conductivity.

The electrothermal model must be solved by imposing proper interface and boundary conditions. In our case, the computation domain is given by a box, including the structure under study, and the thermal and electrical flux exchange is only possible through the electrodes. In the electrical problem, the Dirichlet-type boundary conditions are assumed: the WL electrodes can be fed at one side or at both sides with a given bias voltage, whereas the BL bars are grounded. For the thermal problem, the electrodes are assumed to be in contact with an ideal heat sink, imposing constant temperature $T = 300$ K on the boundary surfaces of the closing box corresponding to nonconducting thermal and electrical materials, and the thermal adiabatic and dielectric electrical conditions are imposed. The electrothermal model is finally closed by setting the initial conditions.

A. Model Parameters for Conventional Materials

The thermal conductivity $\kappa(T)$ of Ni^+ CF can be modeled as formulated in [20], by means of an Arrhenius dependence on temperature. Here, we adopt the approach described in [21], where the model considers Wiedemann–Franz (WF) contribution in mesoscopic conductors

$$\kappa_{\mathrm{CF}}(T) = \sigma_{CF}(T) \cdot L \cdot T \qquad (2)$$

where $L = 2.4410^{-8}\mathrm{W} \cdot \Omega \cdot \mathrm{K}^{-2}$ is the WF Lorenz constant value, and $\sigma_{\mathrm{CF}}(T)$ is the electrical conductivity of the Ni+ CF, which can be modeled as [14]

$$\sigma_{\mathrm{CF}}(T) = \frac{\sigma_{CF0}}{1 + \alpha_{\mathrm{CF}}(T - T_0)} \qquad (3)$$

where σ_{CF0} is the electrical conductivity at $T_0 = 300$ K and α_{CF} is the temperature coefficient, with values in Table II. Besides, the electrical conductivity for nickel bars is assumed to be temperature-independent (e.g., $\sigma_{\mathrm{Ni}}(T) = \sigma_{\mathrm{Ni}}$), whereas, for copper, it can be again expressed as in (3), in which the α_{Cu} value is listed in Table II at T_0. Note that such values take into account the size effects of the submicron dimension of

TABLE I
FITTING COEFFICIENTS OF THE THERMAL CONDUCTIVITY (4)

film	a_1 $Wm^{-1}K^{-1}$	a_2 $Wm^{-1}K^{-1}$	b_1 K^{-1}	b_2 $10^{-3}K^{-1}$	c $W.m^{-1}K^{-1}$
TiO_2	230.2	22.3	0.037	6.5	5.1
HfO_2	0.14	−2.2	10.6	5.2	1.4

TABLE II
RRAM GEOMETRY AND PARAMETER VALUES AT T = 300 K

Material	CF	diode			BL/WL			HfO_2
		TiO_2	Pt	Ti	Ni	Cu	CNT	
Width (nm)	16	80			80			80
Height (nm)	80	50	30	30	30			80
κ $Wm^{-1}K^{-1}$	22	33.8	8.31	21.9	22	380	200	0.9
c $Jkg^{-1}K^{-1}$	445	133	710	523	455	400	700	286
σ $(S.m^{-1})$	0.12 M	3.07k (ON) 50m (OFF)	9.65 M	2.5 M	0.12 M	33.5 M		0,7u
α (K^{-1})	1.4m	--------			$2.7m$ (Cu)			----
ρ $(kg.m^{-3})$	8.9m	19.8k	4.2k	4.5k	8.9k	8.9k	1.6k	9.7k

the conductors, e.g., [22]. All the other parameters are almost constant with the temperature and are given in Table II, taken from [14] and [16].

As for the other materials, the experimental behavior of κ(T) is provided in [23] for the metal oxide TiO_2 film and in [24] for that in HfO_2. In both cases, it can be fitted as follows [19]:

$$\kappa(T) = a_1 \exp(-b_1 T) + a_2 \exp(-b_2 T) + c \quad (4)$$

whose fitting coefficients $a_i, b_i; i \in \{1, 2\}$ and c are in Table I. The thermal conductivity for all the other materials is almost constant with T, with the values given in Table II.

B. Model Parameters for CNTs

Given their outstanding physical properties, novel carbon-based nanomaterials, such as CNTs or graphene nanoribbons (GNRs), have been recently proposed to realize new architectural solutions for RRAM devices [25], [26]. This article investigates the use of these materials within the architectures in Fig. 1 to realize the WL/BL. Indeed, superior signal and thermal integrity performance have been demonstrated for CNT or GNR interconnects, e.g., [27] and [28].

Especially, here, we consider the use of bundles of multiwall CNTs (MWCNTs), given their excellent electrothermal behavior [29]. The electrical resistance of a bundle of N CNTs is evaluated as the parallel of the N resistances associated with each of them, modeled as [27]

$$R_{\mathrm{CNT}}(T) = \frac{R_c(T)}{M(T)} + \frac{R_0}{2M(T)} \frac{l}{l_{mfp}(T)} \quad (5)$$

where l_{mfp} is the electron mean free path, M is the number of conducting channels, and $R_0 = 12.9$ kΩ is the quantum resistance. The contact resistance R_c is a lumped term that takes into account the effect of the CNT/metal interface, whereas the second term in (5) is a distributed resistance that vanishes for short lengths $l \ll l_{mfp}$. The number of channels M is increasing with increasing CNT diameter D and temperature T [32], whereas the mean free path l_{mfp} and the contact resistance $R_c(T)$ are decreasing and increasing functions of T, respectively [29], [30]. The counteracting behaviors of l_{mfp} and M with T provide excellent thermal stability to $R(T)$, which may have zero or even negative derivative with T, as observed in [31]. Once the bundle resistance $R(T)$ is calculated, the equivalent electrical conductivity can be obtained as $\sigma(T) = l/R(T)S$ and can be fitted by means of formula (4), providing the results in Fig. 2.

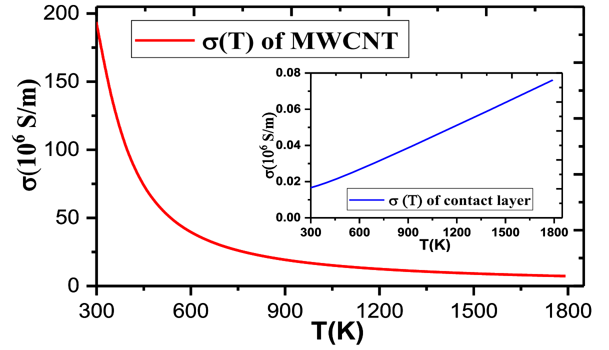

Fig. 2. Equivalent electrical conductivity of the bundle of MWCNT. Inset: equivalent electrical conductivity for the contact layer [18].

Taking into account the WL/BL dimensions in Table II, we assume a densely-packed bundle of ten identical MWCNTs, with $D = 16$ nm and 24 total shells. As for the contact resistance, we should take into account a CNT/Ni contact since the CNT bundles cannot completely replace the Ni bars; otherwise, it would be not possible to create the filament. Therefore, we assume the presence of a small Ni electrode at the top of the RRAM cell in Fig. 1(b). Unfortunately, huge contact resistances for CNT/Ni electrode are reported, in the range of $M\Omega$ [32]. Here, we assume the following model for the contact resistance:

$$R_C(T) = \beta(T - T_0) + R_{C0} \quad (6)$$

with $\beta = 13\ k\Omega \cdot K^{-1}$ and $R_{C0} = 30$ kΩ at $T = T_0 = 300$ K. Although lower values of contact resistance may be obtained for instance by using rapid thermal annealing [33], we assume here the above conservative values in view of studying realistic cases. These values for the contact resistance have been obtained by using the following.

1) A high number of CNTs in parallel for realizing the interconnect.
2) A layer of palladium (Pd) between the CNT bar and the Ni layer since Pd is considered as one of the best metals for creating low-resistive contacts with CNTs [34]. The resulting equivalent conductivity is fitted by (4) as shown in Fig. 2, with $a_1 = 2.5$ GS·m^{-1}, $a_2 = 1$ GS·m^{-1}, $b_1 = 9.6$ m·K^{-1}, $b_2 = 2.2$ m·K^{-1}, and $c = 5.64$ MS·m^{-1}. The values of the conductivity at 300 K are in Table II.

The thermal conductivity of the isolated CNTs can reach values as high as 3300 Wm^{-1}K^{-1}, but, when they are bundled, this value is strongly reduced, depending on the bundle quality (for instance, density, alignment, defects, and so on). Once again, to study a realistic case with a standard bundle quality,

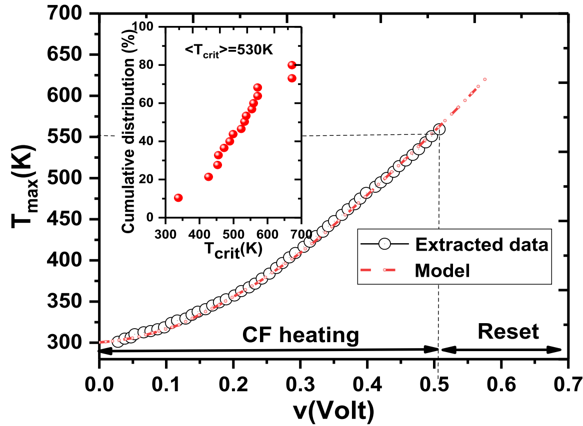

Fig. 3. Experimental validation of the model applied to the 1R-RRAM in [20]: CF temperature as a function of the voltage applied to the conducting filament: model solutions (dashed line) versus experimental data (white dots).

here, we consider the value of 200 $\mathrm{Wm^{-1}K^{-1}}$, the lower one reported in [29]. All the other parameters are given in Table II.

C. Numerical Implementation and Validation of the Model

The presented electrothermal model has been implemented in the COMSOL Multiphysics tool [35] and validated against experimental and simulation results available in the literature. The experimental results refer to the 1R RRAM studied in [20]. Here, we use the proposed model to reproduce the behavior of the temperature of the CF as a function of the reset voltage applied to the electrodes. In the 1R structure, the application of the reset voltage produces a CF temperature increase until a critical value T_{crit} is reached, at which the filament dissolution occurs, resetting the device. The geometrical parameters and the sweep voltage have been set according to the data provided in [16] and [20]. The only parameters that have been here tuned to fit the experiment are the filament width and the resistive temperature coefficient α_{CF} appearing in expression (3). Their values are reported in Table II. In Fig. 3, the numerical solution obtained by the COMSOL model (dashed line) is successfully compared to the experimental ones (dots), as provided in [20].

The second benchmark case study is provided by $1 \times 3 \times 2$ 1D1R X-bar structure analyzed in [36], with a row of RRAM that is active and another row that is passive. The computed transient behavior of the maximum temperature in the active and passive cells is shown in Fig. 4, successfully compared with the numerical solution given in [36], with an error $<4.3\%$.

III. Signal and Thermal Integrity Analysis

A. Transient Analysis of a Single RRAM Cell

Let us consider the single 1D1R RRAM cell in Fig. 1(b), with the dimensions in Table II. The typical RESET signal is made by a train of pulses: in each period, there is a "write" pulse of a typical amplitude of about 1 V, followed by a nondestructive "read" pulse, of the typical amplitude of 0.1 V [37], [38]. However, the electrothermal analysis in the literature usually refers to the application of a dc voltage,

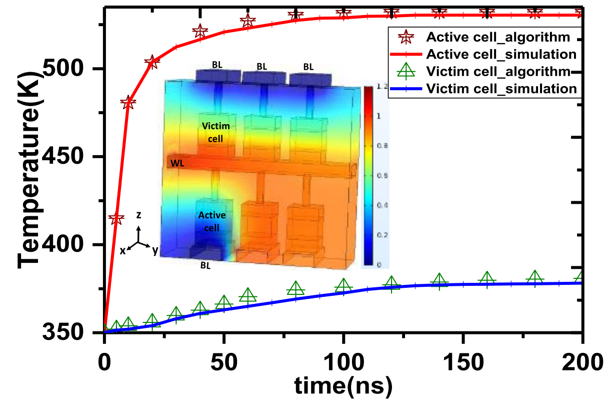

Fig. 4. Numerical validation of the model applied to the 1D1R-RRAM $1 \times 3 \times 2$ array in [35]: active and passive cell maximum temperatures as a function of time: our model (solid lines) versus model in [36] (crosses and triangles).

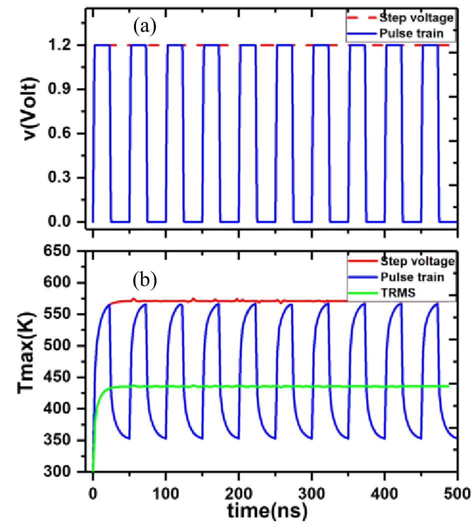

Fig. 5. Transient analysis for a single RRAM. (a) Applied step and pulse train voltages. (b) Corresponding maximum temperature for the two input signals and for the TRMS assumption.

rather than to the abovementioned train pulses, [16], [36]. To highlight the difference, let us study the RRAM (with Ni bars), under a bias voltage described by the following:

1) a step function of amplitude 1.2 V;
2) a pulse train with the same amplitude, a period equal to 50 ns, and a duty cycle of $D = 50\%$ [see Fig. 5(a)].

In both cases, rise and fall times of 2.5 ns are used. The maximum temperature of the device versus time is reported in Fig. 5(b): a step voltage highly overestimates the temperature.

However, the use of such a signal strongly reduces the computational cost. For this analysis, a mesh of about 6000 elements is needed to assess the error below 1%. By using this mesh, the transient simulation in Fig. 5 required 220 s for the step voltage and 1215 s for the pulsed one, on a 16-core CPU and 32 GB-RAM memory workstation. It is, however, possible to define an equivalent step voltage and avoid using the pulse train. To this end, we can express the maximum temperature reached after applying a bias voltage of amplitude V_p as

$$T^{\max} - T_0 = R_{\text{th}} P^J \quad (7)$$

TABLE III
ANALYZED CASES FOR THE 5 × 5 × 5 RRAM X-BAR ARRAY

Case	Bar material	Bias level	WL terminal conditions	BL terminal conditions
1	Ni	1.8 V	one side biased, other side floating	one side grounded, other side floating
2	Ni	1.5 V	both sides biased	both sides grounded
3	Cu	1.2 V	as in Case 1	as in Case 1
4	CNT	1,2 V	as in Case 1	as in Case 1

where R_{th} is the equivalent thermal resistance of the device and P^J is the dissipated Joule power, which can be expressed for the step and the pulse train voltage cases as

$$P^J_{\text{step}} = \frac{V_p^2}{R_e},\ P^J_{\text{pulse}} = \frac{V_{\text{trms}}^2}{R_e} \tag{8}$$

where R_e is the equivalent electrical resistance of the device and V_{trms} is the true root mean square (TRMS) value of the voltage pulse, given by $V_{\text{trms}} = V_p\sqrt{D}$. From (7) and (8), it is given as

$$T^{\max}_{\text{pulse}} = DT^{\max}_{\text{step}} + T_0(1 - D). \tag{9}$$

Hence, the pulse voltage train can be replaced by an equivalent step voltage of amplitude equal to V_{trms}. The actual solution is associated with the pulses, as shown in Fig. 5(b). In this case, this approach introduces an error of less than 4.5%.

B. Signal and Thermal Integrity Analysis of a 5 × 5 × 5 X-Bar

In this article, a 5 × 5 × 5 RRAM crossbar structure is studied, where the cells in each layer are connected by WL and BL bars of length 0.8 μm (the cross section dimensions are given in Table II). In the reference case, these bars are made by Ni, and therefore, they act both as the electrodes for each RRAM and as the electrical interconnect routing the signals through the array. Alternative solutions are here investigated, consisting of leaving only a small layer of Ni at the top and bottom of each cell (to provide the active electrodes) but replacing it in the bars with another conventional conductor, such as copper (Cu) or a novel conductor made by a bundle of MWCNT. The characteristics of CNTs are discussed in Section II-B, and the physical parameters for Cu and CNT are reported in Table II.

The RESET switching is analyzed: in this case, all the cells are in the low resistance state, hence providing the highest current levels and, consequently, the worst conditions in terms of voltage drop and heat production. The structure is fed as follows: the WL bars corresponding to the first, third, and fifth layers are biased at one side or at both sides. The BL bars are instead grounded at one side or both sides. Consequently, the RRAM cells belonging to the first, third, and fifth layers are active, whereas those belonging to the second and fourth are passive. Given the abovementioned considerations, four different cases have been defined, as summarized in Table III. As for the thermal management problem, here, we assume that the conducting bars at the top (fifth) and bottom (first) layers are connected to a heat sink, imposing the fixed temperature of $T = 300$ K.

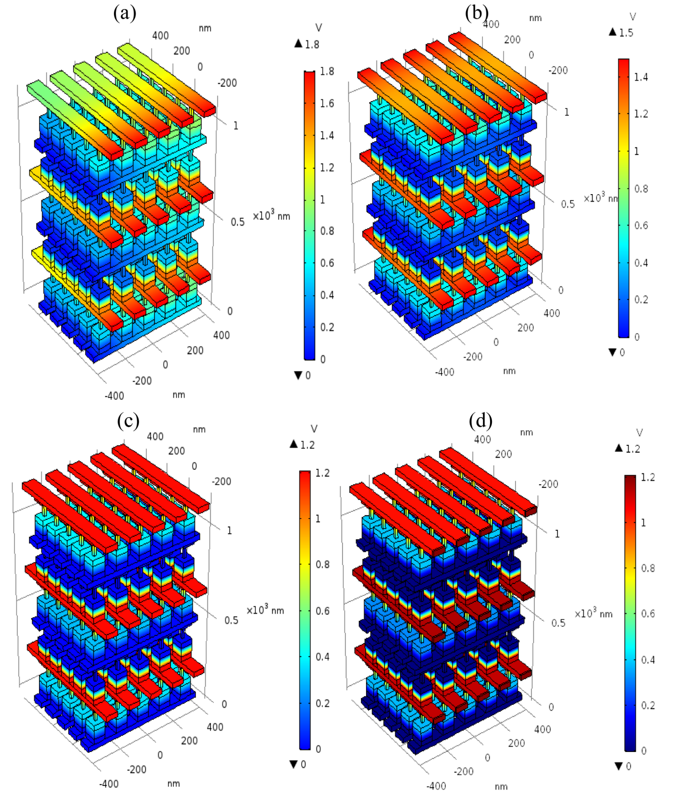

Fig. 6. Computed steady-state voltage distribution in the RRAM *X*-bar structure for the cases in Table III. (a) Case 1. (b) Case 2. (c) Case 3. (d) Case 4.

The computed 3-D steady-state distributions of the voltage and temperature across the 5 × 5 × 5 structure are plotted in Figs. 6 and 7, respectively, for the cases defined in Table III. From Fig. 6, it is evident that the Ni bars (cases 1 and 2) introduce a severe voltage drop so that the voltage imposed across the CF strongly varies from the nearest to the farthest cell from the bias application point. The maximum and minimum voltages V_{CF} computed for each layer are reported in Table IV: for case 1, despite the high bias voltage (1.8 V), the furthest cells to the voltage supplier will not reset, with V_{CF} being below 0.5 V.

As for layers #2 and #4, where the RRAMs are supposed not to reset, the electrical crosstalk is not so relevant, as shown by the low values of the induced voltages reported in Table IV. Note that the results for the passive layers #2 and #4 are similar, as they share the same distance from the heat sink. The use of Cu (case 3) or CNT (case 4) bars may solve the problem: although the bias voltage is reduced to 1.2 V, all the cells in the active layers correctly switch, and the difference between the maximum and minimum values of V_{CF} is small.

As for the thermal behavior, Fig. 7 shows that the use of Ni bars (cases 1 and 2) leads to a higher temperature rise compared with Cu (case 3) or CNT bars (case 4). This is also shown in Fig. 8 that plots the transient behavior of the maximum temperature value for the four cases. However, when the voltage drop is too high, the highest temperature may be found on the electrode rather than the filament, as in the case of Ni bars, where many RRAM cells do not switch. The thermal performance of CNT and Cu solutions is comparable:

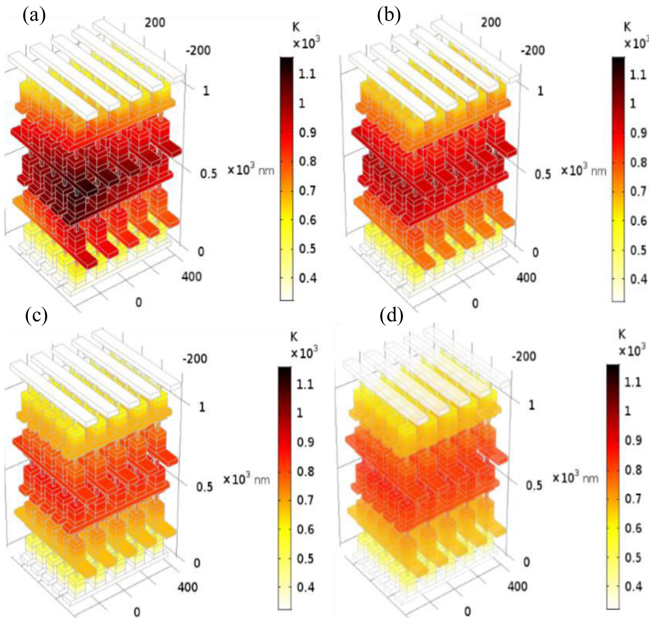

Fig. 7. Computed steady-state temperature distribution in the RRAM *X*-bar structure for the cases in Table III. (a) Case 1. (b) Case 2. (c) Case 3. (d) Case 4.

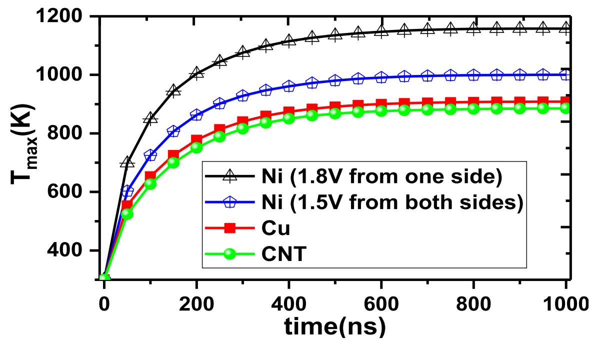

Fig. 8. Maximum temperature computed in the 5 × 5 × 5 *X*-bar structure as a function of time for the considered four cases in Table IV.

in fact, these temperature ranges are within the CNTs' material capability to maintain structural integrity, but not for Cu, being too close to its melting point. Besides, the contact resistances play a crucial role in CNTs (see Section II). For larger structures (hence longer bars), the Cu performance worsens, whereas a better condition occurs for the CNT one since the contact resistance becomes less important due to the effect of ballistic transport (e.g., [27]). It is worth noting also that the ON-state resistance of the RRAM cells significantly affects the steady-state temperature. We have analyzed the case where the on-state resistance was increased by a factor of 10, and we found, as expected, that Tmax is decreased from 575 k to 425 K in a steady state.

Table IV reports the maximum value of the steady-state temperature at the middle point of the CF of the cells of each layer: the inner active layer (#3) suffers from the highest temperature rise, being the farthest from the heatsink. The difference in the values of V_{CF} of layer #3 compared with layers #1 and #5 is due to the higher temperature level reached by the CFs in the inner layers. The thermal crosstalk induces in the cells of passive layers (#2 and #4) temperature values higher than the critical value, T_{crit}. This means that these

TABLE IV
COMPUTED METRICS FOR THE SIGNAL AND THERMAL INTEGRITY ANALYSIS OF THE 5 × 5 × 5 X-BAR STRUCTURE

Layer	Metric	Case 1	Case 2	Case 3	Case 4
#1 (active)	$V_{CF,max}$ [V]	0.96	0.85	0.82	0.73
	$V_{CF,min}$ [V]	0.51	0.74	0.79	0.72
	T_{max} [K]	840	738	662	662
#3 (active)	$V_{CF,max}$ [V]	1.12	0.96	0.87	0.81
	$V_{CF,min}$ [V]	0.67	0.86	0.86	0.80
	T_{max} [K]	1150	1010	904	884
#5 (active)	$V_{CF,max}$ [V]	0.86	0.74	0.8	0.62
	$V_{CF,min}$ [V]	0.36	0.61	0.7	0.61
	T_{max} [K]	618	574	560	540
#2 (passive)	$V_{CF,max}$ [μV]	0	165	-47.8	-38.8
	$V_{CF,min}$ [μV]	-740	-180	-72.8	-46.8
	T_{max} [K]	1000	872	769	767

RRAM cells experience unwanted RESET switching although the electrical crosstalk is negligible and the induced voltage is low. Indeed, a minimum level of voltage is needed only when an isolated RRAM is considered, where the temperature T_{crit} is reached by the self-production of heat, after the application of a suitable voltage level (see Fig. 2). However, while the thermal crosstalk occurs severely at the large integration scale, the studied unipolar RRAM device and, in general, thermochemical memories could be integrated into 3-D x-bar structures only if the thermal crosstalk is alleviated. This requires, for instance, using advanced cooling solutions.

Although many applications (e.g., neuromorphic and computer vision) benefit from recently demonstrated RRAM device characteristics and other memories (e.g., low energy/latency and low variation), they always need a high density of crossbar structures. The main issues analyzed here do not actually come from the single-device behavior but rather from the integration scheme (bias, interconnects, and so on). Therefore, even though other thermally induced memory devices are considered, these issues must be addressed as well. The issues tackled in this article are proportional to the density of integration, rather than to the specific property of the single cell.

IV. CONCLUSION

The signal and thermal integrity analysis of RRAM *X*-bar arrays has been performed, by using a full 3-D electrothermal model. To lower its computational cost, an equivalent step-voltage has been introduced to study the real switching due to pulse trains.

The structure so far proposed (with nickel bars) shows major reliability issues: voltage drop, an increase of temperature, and thermal crosstalk. Possible solutions based on an alternative biasing scheme, with the voltage applied at both Ni bar ends, have been shown to mitigate the signal integrity issues but not the thermal one. Alternative solutions, based on new bar materials, are shown to be effective: both copper and CNTs may solve the signal integrity issues and lower the thermal issues. However, the Cu solution may not be reliable as the size of the memory increases, given the high-temperature values. On the contrary, the CNT performance is expected to improve

for larger memory arrays, where the effects of the resistance at the CNT/Ni contacts are less relevant.

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