

# Corrections to “Low-Voltage IGZO TFTs Using Solution-Deposited OTS-Modified Ta<sub>2</sub>O<sub>5</sub> Dielectric”

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**Abstract**—Unfortunately, there are a few typographical errors in the above article. First, (4) is incomplete and the corrected formula is given here. Second, the unit of the interfacial trap density ( $N_{it}$ ) is corrected in three places. Third, the caption of Fig. 6 is corrected to accurately reflect the device structure. The corrections have no influence on the discussion and conclusions of the paper.

**Index Terms**—Anodization, indium gallium zinc oxide (IGZO), low-voltage thin-film transistors (TFTs), self-assembled monolayer (SAM), tantalum pentoxide.

THERE are a few typographical errors in our paper [1]. First, (4) that allows calculation of the interfacial trap density ( $N_{it}$ ) should be written as [2], [3]

$$N_{it} = \left( \frac{SS \log(e)}{kT/q} - 1 \right) \frac{C_G}{q^2} \quad (4)$$

where  $C_G$  is the gate capacitance density,  $q$  is the electron charge,  $k$  is Boltzmann’s constant,  $T$  is the temperature, and  $SS$  is the subthreshold swing. The  $N_{it}$  values given in [1] were calculated using the abovementioned formula and are correct.

Second, the unit of  $N_{it}$  in [1, p. 4] should be  $\text{cm}^{-2} \text{eV}^{-1}$ . Accordingly,  $N_{it}$  was calculated to be  $4.1 \times 10^{12} \text{cm}^{-2} \text{eV}^{-1}$ ,  $4.4 \times 10^{12} \text{cm}^{-2} \text{eV}^{-1}$ , and  $2.1 \times 10^{12} \text{cm}^{-2} \text{eV}^{-1}$  for devices A, B, and C, respectively.

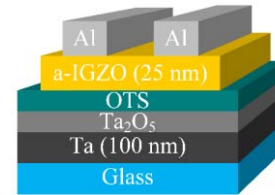


Fig. 6. 3-D schematic of the fabricated Ta/Ta<sub>2</sub>O<sub>5</sub>/OTS/IGZO/Al TFTs using SAM-modified Ta<sub>2</sub>O<sub>5</sub> gate dielectric.

Third, the description of the device structure in the caption of Fig. 6 is not accurate and is different from the description of the device structure used in the text. Fig. 6 with the correct caption is shown here.

The corrections have no influence on the discussion and conclusions of the paper.

## REFERENCES

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