Thermoelectric Property Requirements for On-Chip Cooling of Device Transients

Lakshmi Amulya Nimmagadda and Sanjiv Sinha

***Abstract*— Power dissipation in semiconductor devices peak over short durations with scales much shorter than the thermal time constant. The typical heat sink is too far away from the junction hotspot to provide effective temporal cooling over such durations. Here, we theoretically explore on-chip Peltier cooling over short (∼100 ms) durations, as a potential solution for managing transients near the junction. Choosing a simple unipolar Peltier device, we evaluate the thermoelectric property requirements for achieving net cooling using a steady Peltier current. Net cooling occurs when the peak transient temperature rise is reduced in the presence of an operating thermoelectric device in comparison with that in its absence. When the substrate is bulk silicon, a large power factor (>50 mW/mK^2) and thermal conductivity (>100 W/mK) are required for net cooling. The requirement is less stringent and the impact more promising in wide-bandgap electronics with low conductivity substrates, where Peltier cooling reduces the impact of interface thermal resistance. This study points out materials research priorities for on-chip Peltier cooling and paves the way for effective realization of transient thermal management in proximity to the junction.**

***Index Terms*— Device transients, hotspot cooling, Peltier cooling, temperature rise, thermoelectric.**

I. Introduction

MINIATURIZATION and 3-D integration trends in electronics have led to increased spatial nonuniformity in on-chip heating and higher localized heat fluxes, which is a key focus for current thermal management [1]–[3]. An emerging aspect of thermal management is temporal variations in localized heat fluxes. For instance, in mobile applications, power dissipation increases to peak levels in short durations that are much shorter than the thermal time constant. This leads to temporal changes in hotspot intensities where the time scale is too short for system-level cooling to be effective during the dissipation time scales. Here, we explore whether an on-chip thermoelectric cooler (TEC) may be more useful in temporal thermal management of hotspots over short (∼100 ms) time durations. Since TECs can be integrated directly on the chip, they can be in closer proximity to device hotspots than off-chip solutions. In prior work, theory and experiments have explored TECs for steady-state hotspot management and demonstrated the temperature reduction of ∼5 K [4]–[6]. However, the problem of controlling a transient temperature rise has not been explored in detail.

Past theoretical work on transients in the TEC operation considered the effect of transient Peltier currents in the presence of a steady hot-side temperature [7]–[10]. They mainly studied the impact of transients on the drive (Peltier) current. Distinct from this, here, we consider the situation where the heat load varies over time. We identify an optimal Peltier current that maximizes cooling and seek to understand the influence of electrical conductivity (σ), thermal conductivity (k), and the Seebeck coefficient (S) on transient cooling. In a further departure from past work, we consider operating the TEC as a cooler (and not a refrigerator), where the Peltier heat flows from the hot to the cold side augmenting Fourier heat conduction, rather than opposing it. In refrigeration, a low value of k reduces the backflow of Fourier heat from the hot side (heat sink) to the cold side (source) and is thus preferred. The cooling considered here increases with an increase in k. Thus, embedding a Peltier device need not necessarily increase the junction thermal resistance. The commonly used thermoelectric material figure of merit (Z) obviously cannot be used as a criterion for comparing materials in this case [11], [12]. Along similar lines, Adams *et al.* [12] recently demonstrated experimentally the necessity of high thermoelectric power factor and high k for steady-state Peltier cooling.

This article is organized as follows. In Section II, we describe the geometry of the device under simulation and provide details of the computational model, such as the governing equations and boundary conditions. Section III details the differences in optimizing the operating current for steady versus transient TEC operation. Section IV discusses the results from the model and describes the effect of S, σ, and k on transient cooling. We identify quantitative requirements on S, σ, and k to achieve a net transient cooling in silicon versus a sapphire die and discuss benefits of transient on-chip Peltier cooling. This work provides insights into transient

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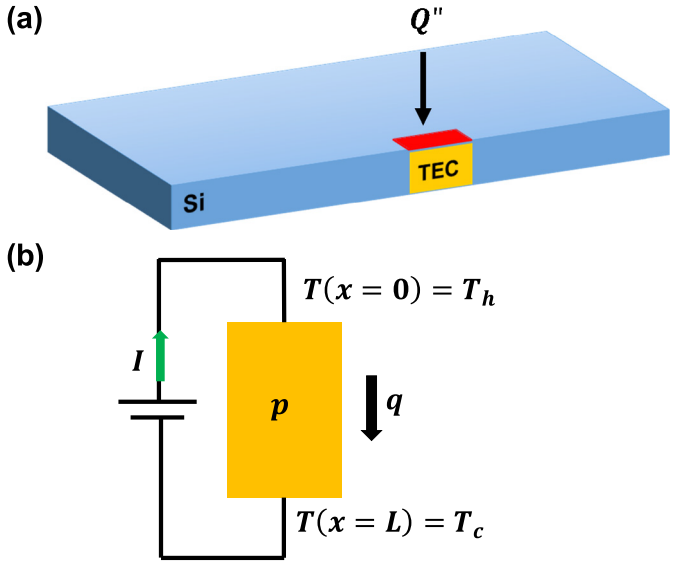

Fig. 1. (a) Cross-sectional view of the geometry considered in the analysis. A silicon die with a hotspot at the center receives a heat flux, Q''. A p-type TEC, depicted in yellow, is located directly below the hotspot to provide effective cooling. (b) Schematic of the TEC showing current flow I and heat flow q from the hot side to the cold side.

management of device hotspots using an embedded TEC module.

II. Transient Peltier Cooling of a Pulsed Hotspot

We consider the situation where a device hotspot undergoes a sudden (pulsed) change in heat flux due to a power burst and analyze the impact of a Peltier cooler that is placed under the hotspot for managing the transient temperature rise. The device geometry consists of a silicon die of 1 cm × 1 cm × 200 μm with a hotspot of 0.5 mm × 0.5 mm located at the center, as shown in Fig. 1(a). A single-leg TEC with the dimensions of 0.5 mm × 0.5 mm × 150 μm is located underneath the hotspot. For the purpose of this article, we consider a unipolar TEC. A practical realization is more likely to involve a bipolar TEC where the device can be powered from a single side. However, we can obtain similar physical insight from considering the simpler case of a unipolar TEC.

We start our analysis assuming the material properties of p-type superlattice Bi_2Te_3/Sb_2Te_3 with $S = 238$ μV/K, $\sigma = 10^5$ S/m and $k = 1.2$ W/mK. The reason for our choice is that this material has been used in previous work by Bulman *et al.* [13] for demonstrating high cooling fluxes using thin-film thermoelectric modules. The change in the material properties with temperature is assumed to be negligible, given the temperature range of interest. A 0.1-s wide square pulse of heat with a maximum flux of 10^7 W/m^2 is applied at the hotspot. The pulse is turned on at $t = 0$ s and turned off at $t = 0.1$ s. After 0.1 s, a steady background heat flux of 10^5 W/m^2 is applied from $t = 0.1$ s to $t = 1$ s. The numbers correspond to typical values in commercial microprocessors. In a practical scenario, a hotspot may experience peak loads in the form of several sharp pulses over very short durations [1]. In the absence of such proprietary heat dissipation information, we chose a peak value of 10^7 W/m^2 and a pulsewidth of 0.1 s to account for an average over individual sharp pulses.

The transient problem described earlier is simulated in COMSOL Multiphysics using the finite-element method. The physics of thermoelectric cooling of the hotspot is modeled as described in [14]. The transient heat diffusion equation solved in the computational domain is given by

$$\rho C_P \frac{\partial T}{\partial t} + \nabla \cdot \mathbf{q} = Q \tag{1}$$

where ρ is the density, C_P is the specific heat, T is the temperature, $\mathbf{q}$ is the heat flow rate, and Q is the volumetric heat source. For electric transport modeling, we enforce current conservation through the following equation:

$$\nabla \cdot \left(\mathbf{J} + \frac{\partial \mathbf{D}}{\partial t} \right) = 0 \tag{2}$$

where $\mathbf{J}$ is the electric current density vector and $\mathbf{D}$ is the electric flux density. The heat diffusion and current conservation equations are coupled together to include thermoelectric effects by considering the following constitutive equations:

$$\mathbf{q} = T[S]\mathbf{J} - [k]\nabla T \tag{3}$$

$$\mathbf{J} = [\sigma] \cdot (\mathbf{E} - [S] \cdot \nabla T) \tag{4}$$

$$\mathbf{E} = -\nabla V \tag{5}$$

where $\mathbf{E}$ is the electrical field intensity, V is the electrical potential, $[S]$ is the Seebeck coefficient matrix, $[k]$ is the thermal conductivity matrix, and $[\sigma]$ is the electrical conductivity matrix of the thermoelectric material. Combining (1)–(5) results in the coupled equations used for modeling thermoelectric effect. The transient heat diffusion equation alone is solved in the region consisting of the silicon die without the TEC. Simultaneously, the coupled equations representing thermoelectric effects are solved self-consistently in the TEC region.

The entire geometry is considered to be at an initial temperature of 300 K. The effective heat transfer coefficient on the heat sink side in a chip package is around 720 W/m^{2}K [15]. The added resistance of heat sink reduces the effective heat transfer coefficient further at the bottom of the die. Hence, the bottom surface of the silicon die is assumed to lose heat with an effective heat transfer coefficient of $h = 300$ W/m^{2}K at an ambient temperature of 300 K. The TEC is electrically biased such that current flows from the hot side of the TEC to the cold side. All the other surfaces of the silicon die and the TEC are thermally and electrically insulated. The current through the TEC and the heat pulse are turned on at $t = 0$ s, and the transient temperature response of hotspot is determined over a time duration of 1 s. We further use this computational model to quantify the cooling effect as a function of the material properties S, σ, and k.

III. Optimal Current of Operation

Fig. 1(b) shows the direction of heat and current flow for the TEC embedded in the silicon die. Under steady-state conditions, the TEC maintains constant hot- and cold-side temperatures, T_h and T_c. The optimum current that maximizes the heat flux (cooling) through the TEC at $x = 0$ is given as $I = ST_h/R$, where R is the electrical resistance of the TEC [16]. For the transient problem, however, both T_h and the heat

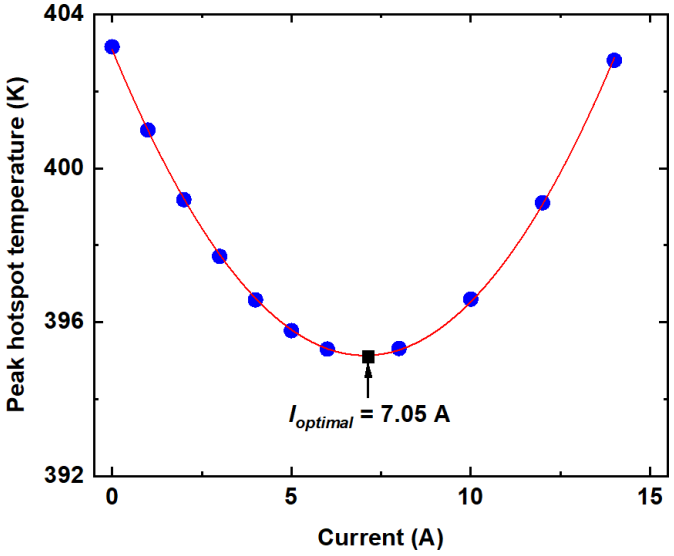

Fig. 2. Peak temperature response of hotspot with an embedded TEC as a function of operating current for the TEC module made of superlattice Bi_2Te_3/Sb_2Te_3 whose $S = 238$ μV/K, $\sigma = 10^5$ S/m, and $k = 1.2$ W/mK. The curve represents a parabola whose minimum is the optimal operating current.

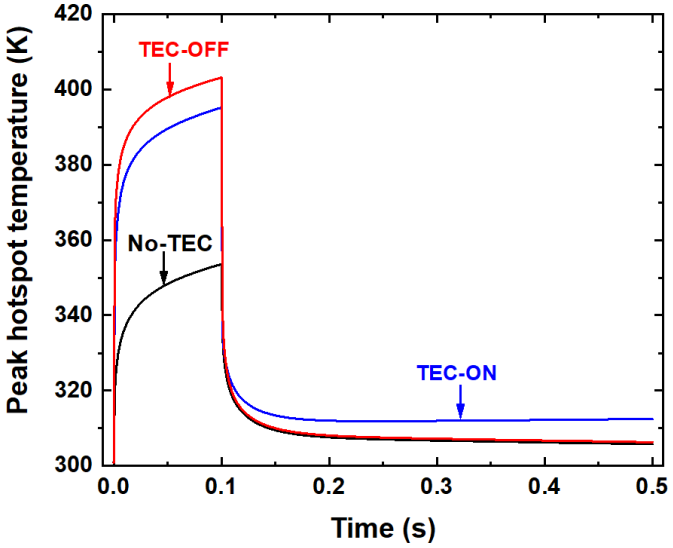

Fig. 3. Hotspot temperature as a function of time for a heat pulse starting at $t = 0$ s with a pulsewidth of 0.1 s for cases with no-TEC, TEC with no operating current (TEC-OFF), and TEC with optimal operating current (TEC-ON). The material of the TEC is superlattice Bi_2Te_3/Sb_2Te_3 with $S = 238$ μV/K, $\sigma = 10^5$ S/m and $k = 1.2$ W/mK.

flux at $x = 0$ are functions of time. Thus, it is not apparent what the optimization condition and the consequent optimal operating current should be. To our knowledge, an analytical solution has never been explored in the literature. However, it is unlikely whether any closed-form expression can be derived for an optimal current in this case. Analytical work on this topic remains a target for a future study.

Here, we solve for the optimal current numerically by computing the hotspot temperature under different operating currents and identifying the current that achieves the lowest peak hotspot temperature. Fig. 2 shows the variation of the peak hotspot temperature as a function of the operating current for a TEC made of superlattice Bi_2Te_3/Sb_2Te_3. The minimum hotspot temperature is obtained at an operating current of $I = 7.05$ A in this case. The optimal operating current is a complicated function of material properties (S, σ, and k) and the transient heat flux profile. Generally, increasing S and σ supports a higher optimal current and increased cooling. For example, increasing S from 238 to 350 μV/K shifts the optimal current to 9.51 A. Increasing σ by one order of magnitude nearly doubles the optimal current.

IV. Results

As mentioned in Section II, we consider Bi_2Te_3/Sb_2Te_3 superlattice as our baseline material. Using the computational model, we determined the transient temperature response in the silicon die for three different cases: 1) no-TEC; 2) TEC-ON and 3) TEC-OFF. The first case provides a baseline comparison when a TEC is absent. This is the standard situation when heat flow from the hotspot is via Fourier heat diffusion alone through the silicon die. All boundary conditions and initial conditions are identical across the three cases. Adding an on-chip TEC to the die leads to cases 2 and 3. When the TEC is ON, heat flow takes place due to the thermoelectric effect in addition to the Fourier conduction. When the TEC is OFF, heat flows only due to Fourier conduction, but the TEC may add a thermal resistance compared to case 1. For thermoelectric cooling to be effective, switching the TEC ON should reduce the hotspot temperature below that with no TEC present. We include the TEC-OFF case as an intermediate case to better understand the impact of k of the TEC material in relation to that of silicon.

Fig. 3 shows the peak temperature of the hotspot as a function of time for the three cases discussed earlier. Compared with the base case of a silicon die without any TEC, there is an increase in the hotspot temperature when the TEC is introduced into the silicon die but kept passive. This arises from the typically low thermal conductivity of the TEC material in relation to that of silicon that it replaces. When the TEC is switched from the OFF state to the ON state using an optimal operating current, the hotspot temperature reduces by as much as $\sim$10 K. However, the TEC-ON case still shows a higher hotspot temperature in comparison with the no-TEC case. This is due to the relatively high thermal conductivity of silicon that is difficult to beat using the typical power factors of common TE materials. A subtle result is that the temperature is higher for the TEC-ON case than that for no-TEC and TEC-OFF cases once the heat flux diminishes. This is due to the Peltier current being kept steady at the level optimal for the higher heat flux.

In Section II, we established that a higher thermoelectric power factor $S^2\sigma$ and thermal conductivity k result in higher TEC cooling power at steady state. We now consider the effect of increasing $S^2\sigma$ and k on the lowering of the transient hotspot temperature. In particular, we seek to quantitatively identify the respective $S^2\sigma$ and k at which net cooling becomes feasible. We performed a parametric sweep by varying S from 238 to 500 μV/K, σ from 10^5 to 10^7 S/m, and k from 1.2 to 100 W/mK. These ranges correspond to experimentally known ranges of these properties near room temperature.

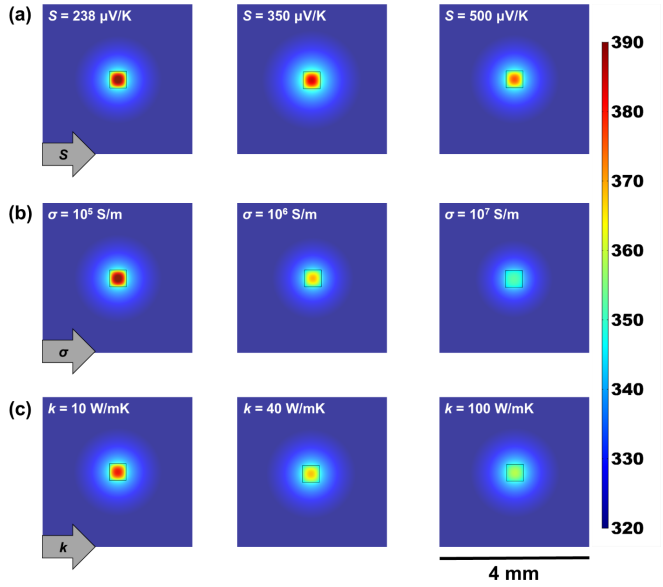

Fig. 4. Temperature distribution in the silicon die with (a) increase in Seebeck coefficient for $S = 238\ \mu$V/K, $S = 350\ \mu$V/K, and $S = 500\ \mu$V/K at $\sigma = 10^5$ S/m and $k = 1.2$ W/mK, (b) increase in electrical conductivity for $\sigma = 10^5$ S/m, $\sigma = 10^6$ S/m, and $\sigma = 10^7$ S/m at $S = 238\ \mu$V/K and $k = 1.2$ W/mK, and (c) increase in thermal conductivity for $k = 10$ W/mK, $k = 40$ W/mK, and $k = 100$ W/mK at $\sigma = 10^5$ S/m and $S = 238\ \mu$V/K. The square cross section at the center is the hotspot.

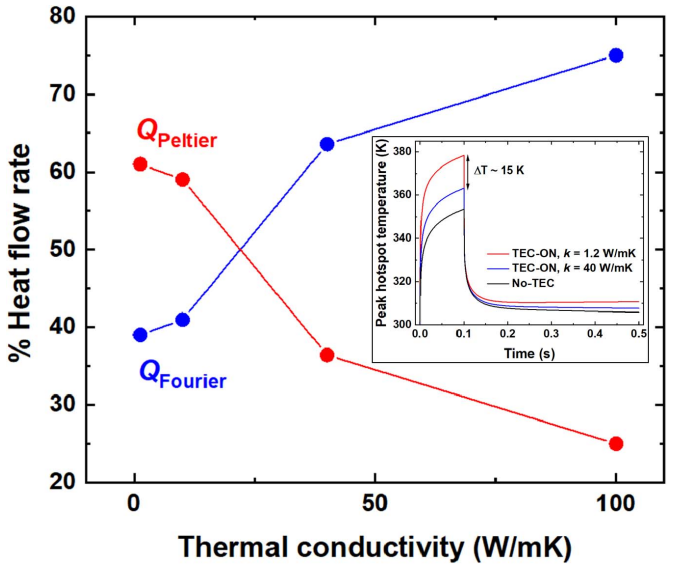

Fig. 5. Percentage of Peltier heat flow rate and Fourier heat flow rate through the TEC as a function of thermal conductivity k of the TEC. The other thermoelectric properties are kept constant at $S = 500\ \mu$V/K and $\sigma = 10^5$ S/m. Inset: peak hotspot temperature as a function of time for a heat pulse starting at $t = 0$ s with a pulsewidth of 0.1 s for no-TEC case and TEC-ON case with different TEC thermal conductivities, $k = 1.2$ W/mK and $k = 40$ W/mK. The peak hotspot temperature reduces by ~15 K.

For example, the Seebeck coefficient is around 200 μV/K for the common Bi_2Te_3 alloys [17] and increases to 500 μV/K for certain thin-film perovskites, such as La-doped $SrTiO_3$ at room temperature [18], [19]. The electrical conductivity for thermoelectric materials varies from 10^5 S/m for Bi_2Te_3 alloys [17] to 10^7 S/m for magnon-drag metals, such as cobalt [20]. The thermal conductivity ranges from 1 W/mK for typical Bi_2Te_3 alloys [17] to 100 W/mK for doped Si [21] and cobalt [20].

While we account for accurate volumetric heat capacities of individual materials, we do not specifically analyze the impact of heat capacity. The reason is twofold. The volumetric heat capacities of dense solids are mostly within the same order of magnitude. Second, the effect of volumetric heat capacity depends on the length of the TEC. For the geometry under consideration, the hot side of TEC experiences a temperature change of 1 K when TEC volumetric heat capacity changes from Bi_2Te_3 to Co.

Fig. 4 shows the 2-D contours of the transient temperature distribution at the hot side of the silicon die and compares the effect of increasing S, σ, and k individually. The superposed square indicates the region of the 0.5 mm × 0.5 mm hotspot. When any one of S, σ, or k is increased keeping the other properties constant, we observe a considerable reduction in the maximum hotspot temperature. Lateral spreading of heat outside the hotspot region, gauged by the radial temperature distribution, is comparable in all situations, suggesting that the dominant heat flow is into the plane of the paper (through the Peltier device underneath the hotspot). Within the possible range of increase, σ has a greater effect on cooling than S. However, we note that the very high conductivity of 10^7 S/m represents a unique and rare case [12] and is not generally feasible. Increase in k is equally effective in lowering temperatures and appears more feasible in terms of available materials.

Fig. 5 shows the changing contributions of Fourier and Peltier heat to the total heat flow rate from the hotspot as thermal conductivity increases. Here, $S = 500\ \mu$V/K and $\sigma = 10^5$ S/m are held constant, and a range of k from 1.2 to 100 W/mK is considered. We expect the peak temperature to decrease when k increases. However, the magnitude is substantial, for example, a decrease by 15 K [see Fig. 5 (inset)] as k increases from 1.2 to 40 W/mK. The contribution of heat flow due to the Fourier conduction in relation to the Peltier effect increases inside the TEC. For example, at the end of the heat pulse ($t = 0.1$ s), the contribution of Peltier heat flow rate (STI) to total heat flow rate drops from 61% to 25% and the contribution of Fourier heat flow increases from 39% to 75% as k increases from 1.2 to 100 W/mK.

Fig. 6 shows the impact of both thermoelectric power factor and thermal conductivity on net cooling. For Peltier cooling to make sense net cooling, ΔT, defined as the difference between the peak temperatures in the absence of the TEC and that with a TEC switched ON, should be positive. The crossover (null) point represents the combination of $S^2\sigma$ and k that yields net cooling. At $k = 100$ W/mK, a high value for thermal conductivity (that corresponds to cobalt or silicon doped to ~10^{19} cm^{-3}), the power factor requirement is still quite high at ~50 mW/mK^2. In comparison, the peak power factor at 300 K is ~16 mW/mK^2 for cobalt. A lower thermal conductivity material, such as the commonly used Bi_2Te_3, would fare worse with an improbable power factor requirement of 500 mW/mK^2. The typical power factor for Bi_2Te_3 is comparable to and only slightly higher than that of doped silicon. In addition, parasitic losses related to electrical and

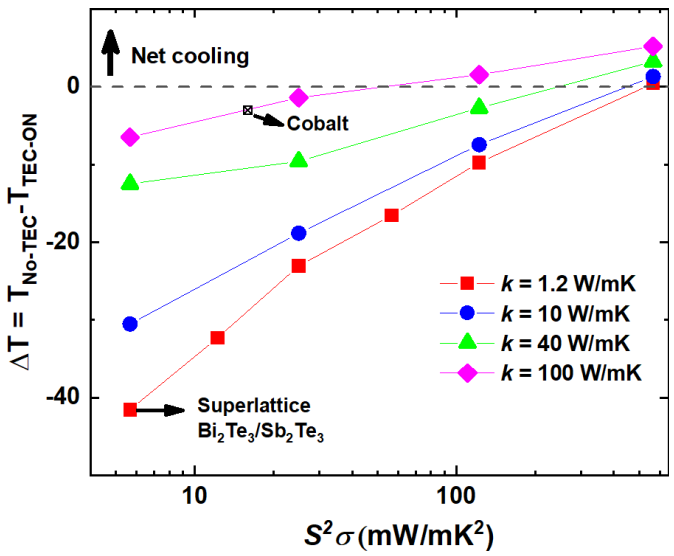

Fig. 6. Net cooling of hotspot defined as the difference in peak hotspot temperatures, $\Delta T = T_{\text{No-TEC}} - T_{\text{TEC-ON}}$, as a function of thermoelectric power factor $S^2\sigma$ and thermal conductivity k of the TEC.

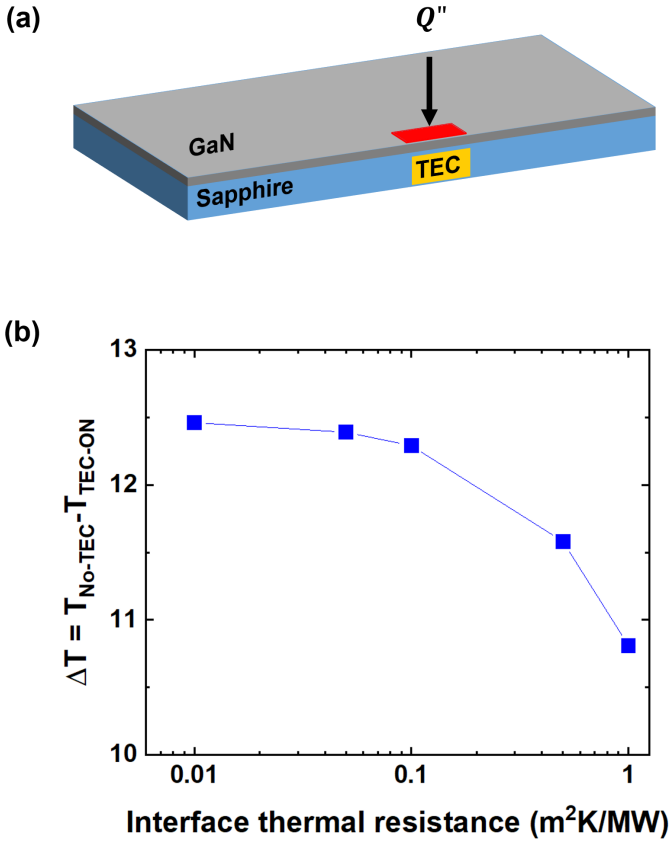

Fig. 7. (a) Cross-sectional view of the geometry with 1 cm × 1 cm × 200 μm sapphire substrate, 1 cm × 1 cm × 20 μm GaN layer, and embedded TEC. The geometry is similar to that shown in Fig. 1 (a) with an added GaN layer. (b) Net cooling as a function of interface thermal resistance between GaN and sapphire. The properties of the TEC considered are $S^2\sigma = 16$ mW/mK^2 and $k = 100$ W/mK.

thermal contact resistances can further affect this crossover point. In prior work on Bi_2Te_3 devices, a suggested range of thermal contact resistance is 2–4.5 m^{2}K/MW [22]. Increasing the thermal contact resistance between the TEC and the silicon die from 0 to 2 and 4.5 m^{2}K/MW increases hotspot temperature in the TEC-ON case by ∼1.1 and ∼2.4 K, respectively. We estimate a nontrivial shift on the order of 10 mW/mK^2 in the crossover point of $S^2\sigma$ for net cooling, highlighting the significance of engineering thermal contacts. While parasitic Joule heating in metal contacts and lead wires are expected to be present, we estimate these to be negligible when compared to the heat generated in the TEC [23].

The spatial location and size of the TEC also affect cooling. When the TEC is spatially offset from the hotspot, cooling potential may be severely compromised. Increasing the cross-sectional area of the TEC reduces the electrical resistance and increases the optimal current. The overall impact is undesirable since peak temperature increases due to replacing silicon with a low thermal conductivity material without a corresponding gain in Peltier heat flow.

Power bursts can be both shorter and longer than what we have considered so far. For similar power dissipation occurring over longer (∼1–10 s) durations, achieving a net cooling is obviously more difficult with the crossover point shifting to even higher values of $S^2\sigma$. In this case, the Peltier device may, however, be operated in short burst modes with more complex current profiles than the step function considered in this work. In the case of shorter pulsewidths (∼1 ms), a similar solution strategy described in Section III can be applied to obtain optimal operating current and determine crossover point of $S^2\sigma$ for a given k value.

From the earlier discussion, the requirement of very high power factors, beyond what has been realized in typical thermoelectric materials, presents an unlikely scenario for achieving beneficial Peltier cooling in bulk silicon dies. The key reason for this is the high thermal conductivity of silicon. This poses the question of whether devices on low thermal conductivity substrates, such as sapphire ($k = 35$ W/mK) or on thermally resistive architectures such as in heterogeneous or 3-D integration, could potentially benefit from on-chip Peltier cooling. To explore this, we consider the chip shown in Fig. 7(a). The geometry consists of a 1 cm × 1 cm × 20 μm gallium nitride (GaN) ($k = 130$ W/mK) layer on a sapphire substrate ($k = 35$ W/mK) of 1 cm × 1 cm × 200 μm [24]. The TEC is embedded in the sapphire substrate and the device hotspot is located on top of the GaN layer. The dimensions of the hotspot and the TEC, boundary conditions, initial conditions, and the computational model employed in COMSOL are identical to the model described in Section II. Cobalt is chosen as the material of the TEC with $S^2\sigma = 16$ mW/mK^2 and $k = 100$ W/mK [20]. We find the net cooling to be ∼12 K in this case out of which ∼9 K corresponds to Fourier conduction and ∼3 K corresponds to Peltier cooling. In a silicon die, for comparison, we found an excess heating of ∼4 K for the same TEC. The interface thermal resistance between the device layer and the substrate is known to vary substantially due to process conditions. Fig. 7(b) shows how the net cooling ΔT is affected as the interface thermal resistance varies from 0.01 to as high as 1 m^{2}K/MW [25]. There is a negligible impact on cooling for resistance in the range of 0.01–0.1 m^{2}K/MW. We note that

typical values of interface resistance achieved under controlled processing lie in the range 0.01–0.04 m^2K/MW [24], where on-chip cooling seems particularly effective.

V. Conclusion

In summary, we investigated the possibility of on-chip Peltier cooling for transient thermal management in close proximity to hotspots. We identified that high S, σ, and k favor greater cooling although, within the possible ranges of each property, the impact of increase is unequal with greater impact from increased electrical and thermal conductivities. Our computational analysis showed that $S^2\sigma > 50$ mW/mK^2 combined with $k > 100$ W/mK is necessary to achieve net cooling in a silicon die. A typical thermoelectric material, such as Bi_2Te_3, will be ineffective in transient Peltier cooling. Rather, higher electrical conductivity materials, such as materials with magnon drag like cobalt, nickel [20], or electron correlation effects like $CePd_3$ [12] or $YbAl_3$ [26], may possess the better combination of properties but may also present challenging integration problems. Our analysis on GaN/sapphire substrate showed that limitations on $S^2\sigma$ of the TEC to achieve net cooling are more relaxed in substrates of low k. On-chip transient Peltier cooling thus appears more feasible in wide-bandgap semiconductor devices or in heterogeneous integration. The main impediment is the requirement for high power factors on the order of 10 mW/mK^2. With the relaxation of requirement for low thermal conductivity, it may be possible for materials research to discover candidates with exceptionally high power factors.

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References

[1] R. Viswanath, V. Wakharkar, A. Watwe, and V. Lebonheur, "Thermal performance challenges from silicon to systems," Intel Corp., Santa Clara, CA, USA, Tech. Rep. 3, 2000. [Online]. Available: http://citeseerx.ist.psu.edu/viewdoc/summary?doi=10.1.1.14.8322

[2] S. V. Garimella *et al.*, "Thermal challenges in next-generation electronic systems," *IEEE Trans. Compon. Packag. Technol.*, vol. 31, no. 4, pp. 801–815, Dec. 2008, doi: 10.1109/TCAPT.2008.2001197.

[3] R. Prasher, "Nano and micro technology-based next-generation package-level cooling solutions," *Intel Technol. J.*, vol. 9, no. 4, pp. 285–296, Nov. 2005, doi: 10.1535/itj.0904.03.

[4] I. Chowdhury *et al.*, "On-chip cooling by superlattice-based thin-film thermoelectrics," *Nature Nanotechnol.*, vol. 4, no. 4, pp. 235–238, Apr. 2009, doi: 10.1038/nnano.2008.417.

[5] A. Bar-Cohen and P. Wang, "Thermal management of on-chip hot spot," *J. Heat Transf.*, vol. 134, no. 5, May 2012, Art. no. 051017, doi: 10.1115/1.4005708.

[6] A. Shakouri and Y. Zhang, "On-chip solid-state cooling for integrated circuits using thin-film microrefrigerators," *IEEE Trans. Compon. Packag. Technol.*, vol. 28, no. 1, pp. 65–69, Mar. 2005, doi: 10.1109/TCAPT.2005.843219.

[7] G. J. Snyder, J.-P. Fleurial, T. Caillat, R. Yang, and G. Chen, "Supercooling of peltier cooler using a current pulse," *J. Appl. Phys.*, vol. 92, no. 3, pp. 1564–1569, Aug. 2002, doi: 10.1063/1.1489713.

[8] R. Yang, G. Chen, A. R. Kumar, G. J. Snyder, and J.-P. Fleurial, "Transient cooling of thermoelectric coolers and its applications for microdevices," *Energy Convers. Manage.*, vol. 46, nos. 9–10, pp. 1407–1421, Jun. 2005, doi: 10.1016/j.enconman.2004.07.004.

[9] A. Miner, A. Majumdar, and U. Ghoshal, "Thermoelectromechanical refrigeration based on transient thermoelectric effects," *Appl. Phys. Lett.*, vol. 75, no. 8, pp. 1176–1178, Aug. 1999, doi: 10.1063/1.124634.

[10] Q. Zhou, Z. Bian, and A. Shakouri, "Pulsed cooling of inhomogeneous thermoelectric materials," *J. Phys. D, Appl. Phys.*, vol. 40, no. 14, pp. 4376–4381, 2007, doi: 10.1088/0022-3727/40/14/037.

[11] M. Zebarjadi, "Electronic cooling using thermoelectric devices," *Appl. Phys. Lett.*, vol. 106, no. 20, May 2015, Art. no. 203506, doi: 10.1063/1.4921457.

[12] M. J. Adams, M. Verosky, M. Zebarjadi, and J. P. Heremans, "Active peltier coolers based on correlated and magnon-drag metals," *Phys. Rev. A, Gen. Phys.*, vol. 11, no. 5, May 2019, Art. no. 054008, doi: 10.1103/physrevapplied.11.054008.

[13] G. Bulman *et al.*, "Superlattice-based thin-film thermoelectric modules with high cooling fluxes," *Nature Commun.*, vol. 7, no. 1, pp. 1–7, Apr. 2016, doi: 10.1038/ncomms10302.

[14] E. E. Antonova and D. C. Looman, "Finite elements for thermoelectric device analysis in ANSYS," in *Proc. 24th Int. Conf. Thermoelectrics (ICT)*, Clemson, SC, USA, 2005, pp. 215–218, doi: 10.1109/ict.2005.1519922.

[15] P. Wang, B. Yang, and A. Bar-Cohen, "Mini-contact enhanced thermoelectric coolers for on-chip hot spot cooling," *Heat Transf. Eng.*, vol. 30, no. 9, pp. 736–743, Aug. 2009, doi: 10.1080/01457630802678391.

[16] D. M. Rowe, "General principles and basic considerations," in *Thermoelectrics Handbook: Macro to Nano*, 1st ed. Boca Raton, FL, USA: CRC Press, 2018, ch. 1, sec. 1.4, pp. 1-6–1-7, doi: 10.1201/9781420038903.

[17] R. Venkatasubramanian, E. Siivola, T. Colpitts, and B. O'Quinn, "Thin-film thermoelectric devices with high room-temperature figures of merit," *Nature*, vol. 413, no. 6856, pp. 597–602, Oct. 2001, doi: 10.1038/35098012.

[18] B. Jalan and S. Stemmer, "Large seebeck coefficients and thermoelectric power factor of La-doped $SrTiO_3$ thin films," *Appl. Phys. Lett.*, vol. 97, no. 4, Jul. 2010, Art. no. 042106, doi: 10.1063/1.3471398.

[19] T. Okuda, K. Nakanishi, S. Miyasaka, and Y. Tokura, "Large thermoelectric response of metallic perovskites: $Sr_{1-x}La_xTiO_3$ ($0 < x < 0.1$)," *Phys. Rev. B, Condens. Matter*, vol. 63, no. 11, Jan. 2001, Art. no. 113104, doi: 10.1103/physrevb.63.113104.

[20] S. J. Watzman *et al.*, "Magnon-drag thermopower and Nernst coefficient in Fe, Co, and Ni," *Phys. Rev. B, Condens. Matter*, vol. 94, no. 14, Oct. 2016, Art. no. 144407, doi: 10.1103/physrevb.94.144407.

[21] M. Asheghi, K. Kurabayashi, R. Kasnavi, and K. E. Goodson, "Thermal conduction in doped single-crystal silicon films," *J. Appl. Phys.*, vol. 91, no. 8, pp. 5079–5088, Apr. 2002, doi: 10.1063/1.1458057.

[22] A. Bar-Cohen and P. Wang, "On-chip hot spot remediation with miniaturized thermoelectric coolers," *Microgr. Sci. Technol.*, vol. 21, no. S1, pp. 351–359, Aug. 2009, doi: 10.1007/s12217-009-9162-4.

[23] L. W. da Silva and M. Kaviany, "Micro-thermoelectric cooler: Interfacial effects on thermal and electrical transport," *Int. J. Heat Mass Transf.*, vol. 47, nos. 10–11, pp. 2417–2435, May 2004, doi: 10.1016/j.ijheatmasstransfer.2003.11.024.

[24] A. Sarua *et al.*, "Thermal boundary resistance between GaN and substrate in AlGaN/GaN electronic devices," *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3152–3158, Dec. 2007, doi: 10.1109/ted.2007.908874.

[25] H.-K. Lyeo and D. G. Cahill, "Thermal conductance of interfaces between highly dissimilar materials," *Phys. Rev. B, Condens. Matter*, vol. 73, no. 14, Apr. 2006, Art. no. 144301, doi: 10.1103/physrevb.73.144301.

[26] D. M. Rowe, V. L. Kuznetsov, L. A. Kuznetsova, and G. Min, "Electrical and thermal transport properties of intermediate-valence $YbAl_3$," *J. Phys. D, Appl. Phys.*, vol. 35, no. 17, pp. 2183–2186, Sep. 2002, doi: 10.1088/0022-3727/35/17/315.