

# Corrections to “Opportunities in Device Scaling for 3-nm Node and Beyond: FinFET Versus GAA-FET Versus UFET”

Uttam Kumar Das<sup>1</sup>, Graduate Student Member, IEEE, and Tarun Kanti Bhattacharyya

IN THE above article [1], there was a typo in Fig. 14. The units for current density should be “ $J[A*cm^{-2}]$ .” The corrected figure is presented here.

## REFERENCES

- [1] U. K. Das and T. K. Bhattacharyya, “Opportunities in device scaling for 3-nm node and beyond: FinFET versus GAA-FET versus UFET,” *IEEE Trans. Electron Devices*, vol. 67, no. 6, pp. 2633–2638, Jun. 2020.

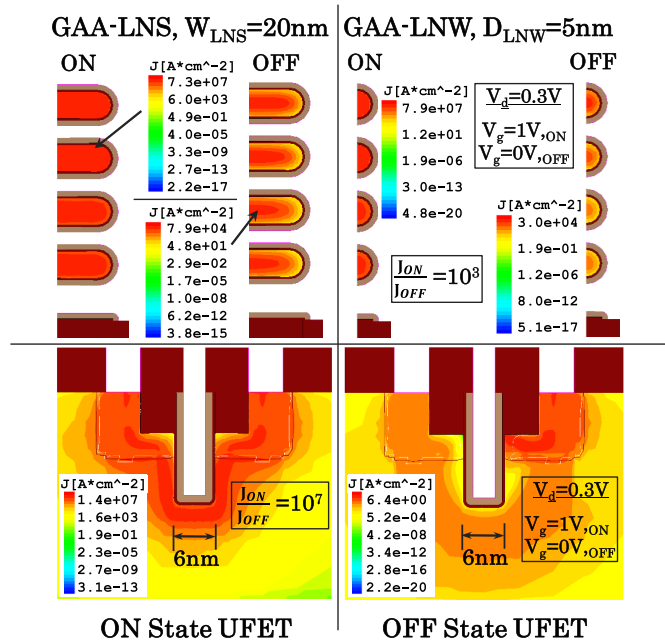


Fig. 14. Electron current density ( $J$ ) in the channel regions with a minimum gate foot-print having 6 nm (UFET width is 20 nm).

Manuscript received June 11, 2020; accepted June 22, 2020. Date of current version July 23, 2020. (Corresponding author: Uttam Kumar Das.)

The authors are with the Advanced VLSI Design Laboratory (AVLSI), Department of Electronics and Electrical Communication Engineering (EECE), IIT Kharagpur, Kharagpur 721302, India (e-mail: uttamece.jgec@gmail.com).

Color versions of one or more of the figures in this article are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TED.2020.3004959