Mixed Hot-Carrier/Bias Temperature Instability Degradation Regimes in Full $\{V_G, V_D\}$ Bias Space: Implications and Peculiarities

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***Abstract*—Characterizing mixed hot-carrier/bias temperature instability (BTI) degradation in full $\{V_G, V_D\}$ bias space is a challenging task. Therefore, studies usually focus on individual degradation mechanisms, such as BTI and hot-carrier degradation (HCD). However, a simple superposition of these mechanisms at an arbitrary $\{V_G, V_D\}$ combination often fails to predict the cumulative damage. We experimentally acquired a large data set covering the full bias space of a pMOSFET which allows us to obtain detailed degradation and recovery maps. Our models for describing oxide and interface defects provide physical insights into the underlying mechanisms and a possible interplay between the degradation modes. Additionally, we perform a dedicated experiment to reveal the implications of different stress regimes onto the various types of defects by switching BTI and HCD stress conditions. The results clearly reveal the conceptual limits of the assumption of independent degradation regimes.**

***Index Terms*—Bias temperature instability (BTI), defect modeling, full bias map, hot-carrier degradation (HCD), mixed-mode stress, reliability.**

I. Introduction

ASSESSING the reliability of a technology typically focuses on idealized device degradation modes, such as bias temperature instability (BTI) and hot-carrier degradation (HCD). Each of these degradation modes is usually assessed in a certain bias space regime, see Fig. 1 (red and blue regions), and is characterized around their respective worst case stress condition. Their interplay within intermediate operating conditions (green and purple regions in Fig. 1), however, is normally, neglected, despite its importance in modern complementary metal–oxide–semiconductor (CMOS) digital circuits. For example, field-effect transistors (FETs) in a logic gate experience a broad range of bias combinations during switching between logic levels.

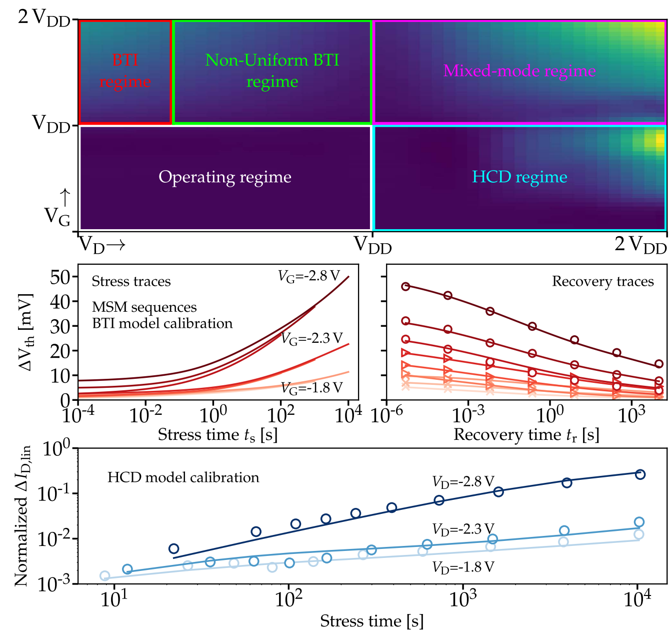

Fig. 1. Top panel: schematic representation of the full $\{V_G, V_D\}$ bias space together with the various degradation regimes. Middle and Bottom panels: the calibration of the models used for describing BTI and HCD shows a very good agreement with experimental traces.

So far, only a limited number of mainly experimentally driven studies have focused on the interplay between different degradation modes and the implications onto the various types of defects. However, they have revealed interesting new details and have concluded that an independent description of the degradation mechanisms leads to incorrect extrapolations. In recent publications [1]–[3] it has been shown that the charging dynamics of individual oxide defects can significantly

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change depending on their spatial position and the applied drain bias. These findings support and complement studies on large-area devices [2], [4]–[9] where it was found that the recoverable component disproportionally reduces with increasing drain voltage. Furthermore, *imec* reported in a series of publications [10]–[13] that nonequilibrium dynamics, such as impact ionization (II), are a crucial component for the understanding of degradation in full bias space and that different degradation modes can indeed access the same defect types. Last but not least, Tyaginov *et al.* [14] investigated the consequences of prestressing devices onto the degradation kinetics by taking into account the stress history of the device.

In this article, we investigate the degradation characteristics of pMOSFETs in full $\{V_G, V_D\}$ bias space, both experimentally and from a modeling point of view using our physical frameworks to describe oxide and interface defects. We use the idealized degradation regimes for BTI and HCD to calibrate our models and subsequently extend the simulations toward the full bias space by explicitly taking into account nonequilibrium transport dynamics. Our modeling approach properly captures the measured trends for all bias conditions within $\{V_G, V_D\}$ space. Additionally, an experiment where we switched BTI and HCD stress conditions reveals puzzling results which can be fully explained by our simulation approach.

II. Experimental Setup

Production quality pMOSFETs with a gate length of $L_G = 100$ nm and a 2.2 nm plasma nitrided gate oxide with an operating condition of $V_{DD} = -1.5$ V have been used for this article. To obtain complete degradation maps, we characterized the devices in a broad range of $\{V_G, V_D\}$ bias space larger than the operating condition V_{DD}. The measurements are based on an extended measure–stress–measure technique [15] where the threshold voltage has been extracted using an ultrafast measurement setup with a delay after a stress of 10^{-6} s. Using ΔV_{rm} as a measure to quantify the amount of degradation allows to continuously monitor the degradation during recovery without applying additional stress. Stress and recovery data have been recorded up to a total time of 10^4 s at a temperature of $T = 398$ K. The recovery was measured at a constant current of 20 μA for $V_D = -1.5$ V, which corresponds to a gate bias around the threshold voltage of the device, $V_G \sim -0.4$ V.

III. Model Calibration

As a first and essential step toward understanding and modeling the physical mechanisms responsible for the created degradation in each region of the bias map, we need to calibrate our models for BTI and HCD. To ensure well-calibrated model parameters possessing predictive quality and no interplay between oxide defects due to BTI and interface states due to HCD, we chose the respective worst case condition for each degradation mode, namely $V_G > V_{DD}$, $V_D = 0$ V for BTI and $V_G \sim 0.5 V_D$ (measurements of $I_{sub,max}$ yield $V_G = 0.53 V_D$) for HCD. Additionally, the dc current characteristics of the fresh device must be properly represented by the simulation framework [16], [17] to ensure a correct field distribution inside the device, see the Appendix.

To model the effect of **BTI** and the responsible mechanism of charge detrapping in **oxide defects**, we used the well-established four-state nonradiative multiphonon model (NMP) [18]–[21]. As shown in Fig. 1 (middle panel) the NMP model is able to accurately describe the experimental data sets for $V_G = -1.8$ V$/-2.3$ V$/-2.8$ V and $t_{stress} = 0.1$ ks/1 ks/10 ks. The extracted model parameters are in full agreement with previous studies and in particular the frequently reported defect band in SiON of about 0.8 eV below the Si valence band [20], [22], [23]. We want to emphasize that for all subsequent simulations we used the same unique parameter set, see the Appendix for more details.

On the other hand, describing **HCD** and the creation of **interface defects** due to the interaction of energetic carriers with interfacial Si–H bonds is based on our newly developed physical framework [24]. This model assumes a resonance state accessible, as was already proposed by the group of Hess [25], [26], for electrons (and holes) which upon electronic relaxation excites phonon modes of the silicon-hydrogen complex and eventually triggers bond dissociation. For electrons, the resonance is around 3.5 eV above the Si conduction band, whereas for holes this state is about 0.5 eV deeper at 4 eV in the valence band. Fig. 1 (Bottom panel) shows good agreement between simulated and experimental degradation traces and demonstrates the quality of the model.

IV. Results

The measurement results for the degradation and the respective recovery map in full $\{V_G, V_D\}$ bias space are shown in Fig. 2. The maximum threshold voltage drift is extracted as the first measurement point in the recovery trace after 10 ks of stress, and $V_{th,max}$ recovery is defined as the change of the drift after a subsequent 10-ks recovery cycle. One can see a strong degradation in the mixed mode as well as in the HCD regime with ΔV_{th} values being three times higher than for the BTI mode. Furthermore, the stress and recovery data clearly reveal that the transition from the HCD to the mixed-mode regime is very sensitive to the applied gate bias, as can be seen for $V_D = -2.8$ V in Fig. 2, which will be discussed in the following. Combining both maps in Fig. 2, on the other hand, shows that almost 70% of the degradation due to BTI recovers within 10 ks. Increasing V_D, however, yields a decreasing recovery-to-degradation ratio toward the mixed-mode regime where less than 10% of the damage is recovered within the relaxation phase. In the case of pure HCD, which is attributed to a more permanent degradation showing annealing effects only at elevated temperatures, see [27], [28], the recoverable component is almost completely absent and thus negligible.

In order to assess the behavior of BTI, HCD, and its interplay in the full bias space, we performed simulations at the 55 measurement points shown in Fig. 2. As we have shown in [29], carrier energy distribution functions (EDFs) play an important role not only for HCD [30]–[32], but also to capture the nonequilibrium dynamics of oxide defects. Primarily the effect of II and the resulting increased concentration of secondary carriers at the source side strongly affect the charging kinetics of traps in the oxide. Thus, we self-consistently solved the bipolar Boltzmann transport equation (BTE) for

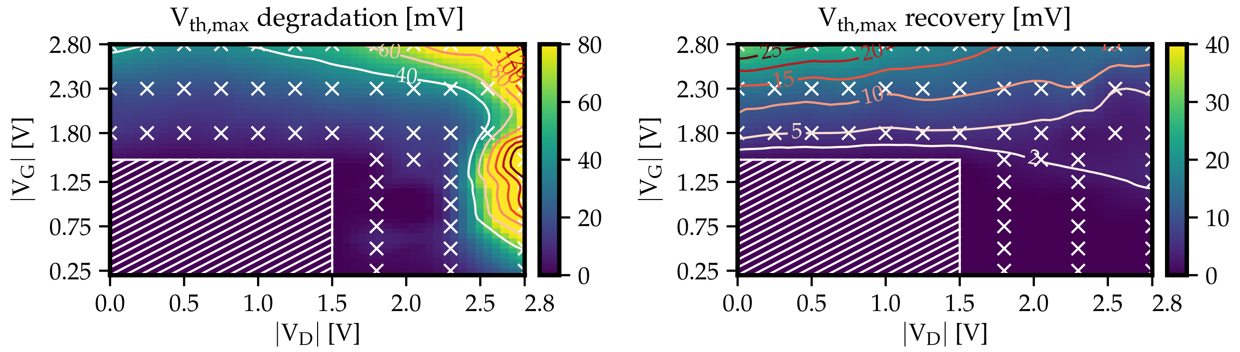

Fig. 2. Experimentally extracted degradation (left) and recovery (right) maps in full bias space outside the operating regime V_{DD}. In total, 55 bias combinations have been measured as indicated by the crosses. The maximum degradation is strongly localized in the vicinity of the HCD regime, whereas the damage in the mixed-mode region is much broader and extends toward the nonuniform BTI area. The recovery map shows a noteworthy contribution only in the BTI regime with a decreasing trend toward the mixed mode and HCD mode. The isolines of ΔV_{th} degradation and recovery provide a better compara bility with the simulation results.

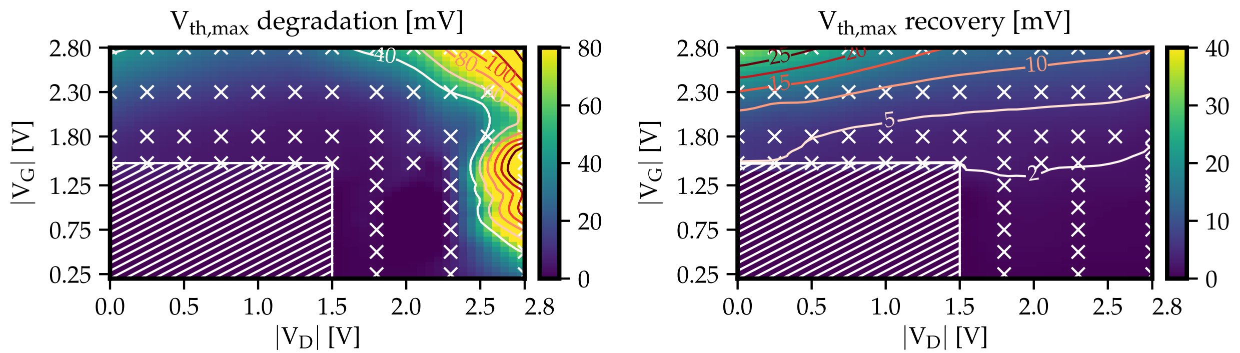

Fig. 3. Simulation results for the bias conditions shown in Fig. 2 taking into account the effect of BTI described by oxide defects and the effect of HCD due to the creation of interface defects. The general trends for degradation as well as recovery are well reproduced by the simulation approach.

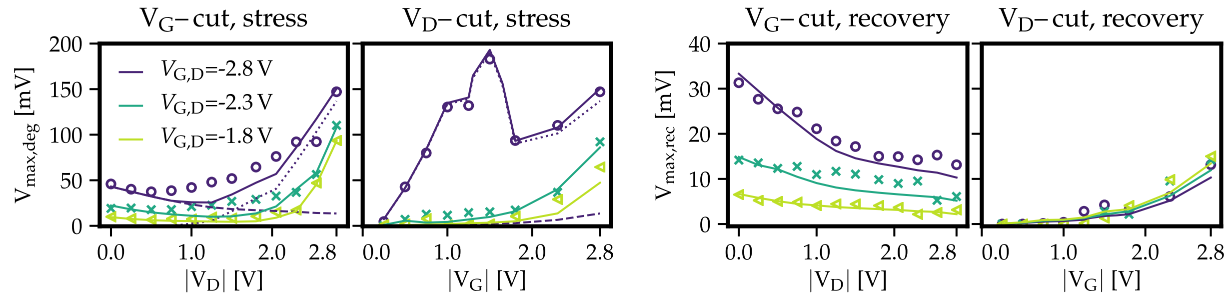

Fig. 4. Cuts along horizontal lines (V_G-cut) and vertical lines (V_D-cut) of the experimental and simulation degradation (left) and recovery (right) maps. Degradation and recovery traces for all $\{V_G, V_D\}$ combinations agree very well with the measurement data. For the most severe stress conditions within each cut the individual contribution of oxide defects (dashed lines) and interface defects (dotted lines) is shown.

all bias conditions using the higher order spherical harmonics expansion simulator SPRING [33], [34]. Phonon and impurity scattering mechanisms as well as II with secondary carrier generation is included within these simulations. However, to introduce a more practical implementation of the full bias space TCAD model for BTI with a reduced complexity, we did not use the nonequilibrium EDFs within the four-state NMP model. Instead, we calibrated the utilized II model [35] within our drift-diffusion setup [16], [17] against the data obtained from solving the BTE to represent hole and electron II rates and thus secondary generated carrier concentrations (CCs). This approximation ensures that the interaction of oxide defects with carriers in the valence as well as the conduction band is properly captured, see [29]. A detailed motivation and validation of this approach can be found in the Appendix.

Simulation results for all $\{V_G, V_D\}$ bias combinations are shown in Fig. 3. The degradation map is in very good agreement with the experimental results, representing the measured trends well in the mixed-mode region and also toward the transitions to HCD and (nonuniform) BTI. Moreover, also the recovery behavior is properly captured, particularly the strong decrease along increasing drain bias conditions.

To better understand and analyze the results, Fig. 4 shows 1-D cuts along increasing V_D and V_G bias conditions. Horizontal cuts (at a fixed V_G) are intuitive to understand: The total degradation in the nonuniform BTI regime initially

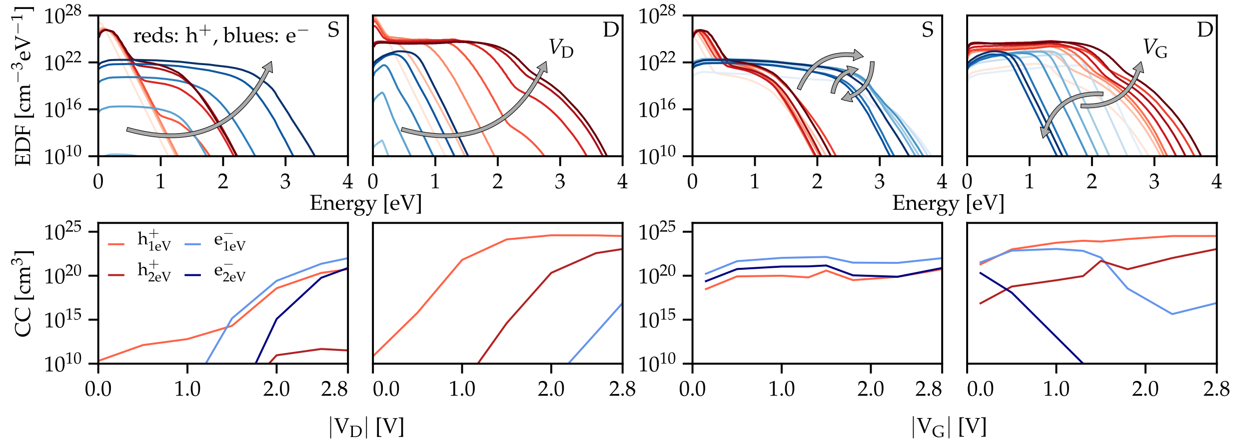

Fig. 5. Carrier energy distribution functions (EDFs) together with the CCs with at least 1 and 2 eV, respectively. Left: hole and electron EDFs and CC along the cut $V_G = -2.8$ V for increasing V_D at the source (S) and drain (D) end of the channel. Right: hole and electron EDFs and CC along the cut $V_D = -2.8$ V for increasing V_G at the source (S) and drain (D) end of the channel.

reduces, mainly due to the decreasing oxide field and the amount of charged traps [2], [4], [5], [29] whereas this trend is reversed for higher drain biases in the mixed-mode stress due to the onset of HCD and the additional damage caused by the creation of interface defects. While the overall degradation characteristics are well represented by the simulations, one feature is not properly captured: The degradation minima are shifted toward higher V_D conditions within our simulations compared to the experimental values. This leads to an underestimated degradation around $V_D = V_{DD}$, which is particularly pronounced for $V_G = -2.8$ V, see Fig. 4. On the other hand, the recoverable component is attributed only to detrapping of oxide defects, and its decreasing trend is properly reproduced by the model approach.

Vertical cuts along constant V_D conditions, on the other hand, reveal a more complex behavior, particularly for $V_D = -2.8$ V. Initially, the total degradation increases toward the worst case HCD stress bias ($V_G = -1.5$ V, $V_D = -2.8$ V), then significantly drops for $V_G = -1.8$ and -2.3 V and subsequently increases again toward $V_G = V_D = -2.8$ V, eventually causing a threshold voltage shift close to $\Delta V_{th,max}$ at the worst case HCD conditions, see Fig. 4. Such a feature is not clearly visible for lower V_D bias conditions due to the suppression of hot-carrier induced damage, see Fig. 1. The simulations show that the degradation along the cut $V_D = -2.8$ V is mainly governed by HCD and the creation of interface states, while oxide defects play only a minor role at severe mixed-mode stress and reduced V_G cuts, see also the recovery traces in Figs. 3 and 4. To understand this behavior in detail, Fig. 5 shows the EDFs at the source and drain side of the channel together with the concentrations of carriers with at least 1 and 2 eV, respectively, for the cuts with $V_G = -2.8$ V (left) and $V_D = -2.8$ V (right). Not surprisingly, for fixed V_G and increasing V_D, holes gain more energy at the drain side and eventually trigger II which leads to a substantial contribution of (energetic) electrons at the source side. This effect has two implications: First, an acceleration and propagation of hot-carrier induced damage along the channel due to energetic secondary generated electrons [30]–[32], see also Fig. 1, and second a modified discharging dynamics of oxide defects caused by the interaction with electrons in the conduction band [29]. The cut along fixed $V_D = -2.8$ V shows a more intricate V_G dependence. For V_G up to -1.5 V the II rate monotonously increases which is reflected in an increasing number of electrons. This can be seen on the drain side in Fig. 5, where the concentration of electrons increases, however, their distribution over the energy changes toward lower values. On the source side, on the other hand, electrons gained a substantial amount of energy which also enhances the respective concentrations with at least 1 and 2 eV. Therefore, the damage in the HCD region, particularly the worst case stress condition which corresponds to $I_{sub,max}$, is caused by a dominant contribution of energetic electrons. However, increasing V_G further actually reduces the effect of II, and thus the created damage. Only at severe mixed-mode stress conditions this trend is again reversed, see Fig. 5, which again leads to an increase in ΔV_{th}, see Fig. 4.

This analysis clearly shows that device degradation in full $\{V_G, V_D\}$ bias space can only be modeled and understood by performing thorough transport simulations and using models based on fundamental physical frameworks.

V. Alternating Degradation Regimes

In order to further investigate the implications of different stress regimes on charge trapping in oxide and the creation of interface defects, we performed experiments with alternating stress conditions followed by a final relaxation phase. In total, we used 14 devices, divided into two groups which have been stressed at a temperature of $T = 443$ K and bias conditions of $V_G = -2.8$ V, $V_D = 0.0$ V (BTI) and $V_G = -0.5$ V, $V_D = -2.8$ V (HCD). The first group of devices was subjected to 10 ks of HCD stress, followed by a 10-ks BTI stress phase and a final relaxation of 10 ks at recovery bias ($V_G = -0.5$ V, $V_D = 0.0$ V). For the second group the BTI and HCD stress sequences have been switched, that is, BTI with a subsequent HCD stress cycle. The measurement results are summarized in Fig. 6 (middle panel). After the HCD stress cycle the first group experiences a threshold voltage drift of $\Delta V_{th} = 40$ mV, which is increased to a shift of $\Delta V_{th} = 170$ mV due to the subsequent BTI stress. Within the relaxation phase the

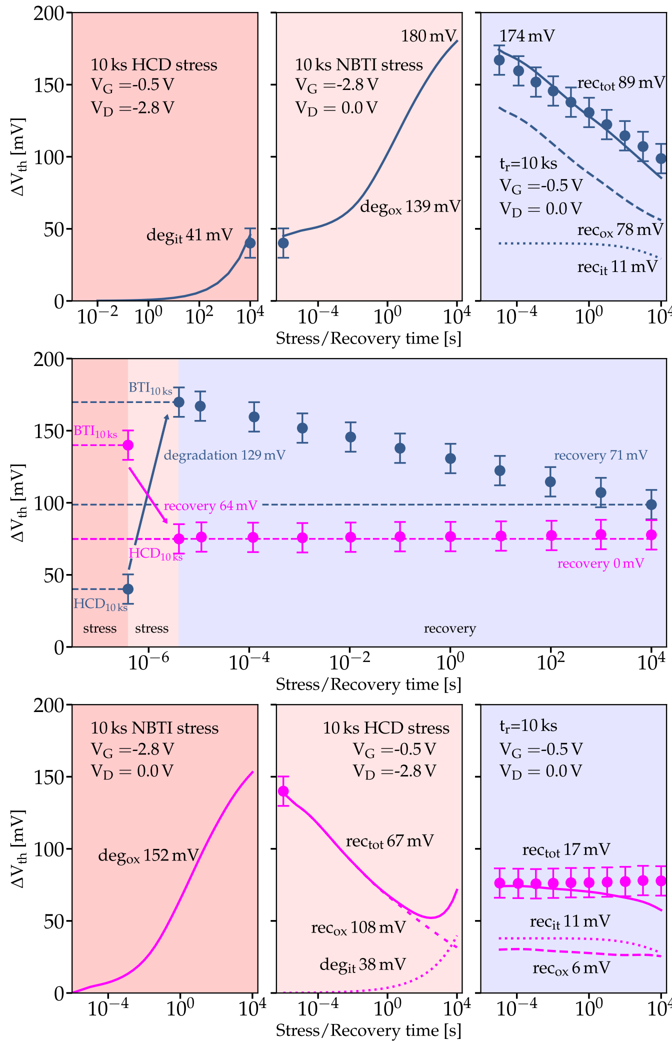

Fig. 6. Experimental and simulation results for the alternating stress conditions experiment. Middle panel: measurement data for seven devices subjected to each sequence. Although HCD→BTI (blue) is intuitive to understand, BTI→HCD (magenta) exhibits an abnormal recovery trend starting from the HCD stress phase. Top panel:simulation results for the first group. In this case, HCD only adds a (permanent) damage whereas BTI follows the well-known behavior. Bottom panels: simulation results for the second group. Although the first BTI cycle behaves as expected, the subsequent HCD stress actually accelerates discharging of oxide traps and simultaneously creates damage due to interface defects.

degradation reduces to $\Delta V_{\rm th} = 98$ mV. Interestingly, if BTI is applied prior to HCD, the first stress phase creates $\Delta V_{\rm th} = 140$ mV of degradation. Even more intriguingly, it seems that a subsequent 10 ks HCD stress does not trigger additional degradation, but rather *decreases* the $\Delta V_{\rm th}$ shift by 65 mV. Additionally, the final relaxation phase does not show any additional recovery effect.

By means of our simulation framework described above we are able to shed light on the mechanisms behind this puzzling phenomenon. The results for the first group of sequences (HCD→BTI→Relaxation) is shown in the upper panels of Fig. 6. The initial HCD stress induces ∼45 mV of degradation, mainly due to the presence of energetic electrons at this specific bias combination, see Fig. 5. The subsequent BTI stress and recovery cycle follows the well-known characteristics of negative bias temperature instability (NBTI), matching the experimental results very well. The accessible oxide defects become charged during the stress phase and subsequently emit the charges again during the following recovery cycle. Thus, one can conclude that for this group of devices, HCD only adds a *preexisting* damage to the device, which slightly perturbs the device electrostatics, but without further implications for oxide defects.

The second stress sequence (BTI→HCD→Relaxation) is shown in the lower panels of Fig. 6. Starting with BTI, the device experiences ∼140 mV of $\Delta V_{\rm th}$ drift. Due to the presence of a *fresh* device without any damage at the interface, this value is slightly higher than for the BTI sequence after HCD for the first group. The following HCD stress sequence reveals an interesting behavior. Contrary to the assumption that only another portion of damage will be added to the predamaged device, the specific HCD condition strongly influences the discharging dynamics of oxide defects. The high concentration of secondary generated electrons along the channel, see Fig. 5, actually accelerates discharging of oxide defects and thus the recovery of BTI damage. However, the competing effect of additional damage due to the creation of interface defects overshadows this mechanism within the experiments and is only accessible by simulations (note that the effect of HCD is slightly reduced due to charged oxide defects perturbing the device characteristics).

Within the final relaxation phase the simulations predict a total recovery of 17 mV, of which only 6 mV are due to discharging of oxide traps. Such a suppressed recovery behavior can be explained by the preceding accelerated discharging phase. However, note that the measurement results are nearly perfectly flat for 10 ks, see Fig. 6. The additional 11 mV recovery, with a strong onset toward longer recovery times, is due to the effect of interface state recovery, as, for instance, proposed by Stesmans [27]. However, as clearly visible in the measurement data for the second group, such a mechanism is apparently absent within our experimentally recorded traces.

VI. Conclusion

We have presented a comprehensive study on the degradation and recovery dynamics of mixed hot-carrier/BTI degradation in full $\{V_{\rm G}, V_{\rm D}\}$ bias space. Our simulation framework uses physical models for the charge transition kinetics of oxide defects as well as the creation of interface defects. Furthermore, our modeling approach explicitly takes nonequilibrium transport effects, such as II and the creation of secondary generated carriers into account, which has two implications: First, *heated* secondary carriers along the channel and on the source side enhance or even dominate HCD. Moreover, they can interact with oxide defects thereby severely distorting their charging kinetics. Our simulation results agree well with the experimental trends and are supported by a detailed analysis which provides insight into the degradation and recovery behavior for various bias regimes.

Additionally, a dedicated experiment where we have alternated BTI and HCD stress conditions reveals peculiarities of their interplay. Alternating the stress order, 10-ks BTI followed by 10-ks HCD or vice versa, resulted in a difference of $\Delta V_{\rm th} = 90$ mV in total degradation. Our simulations showed

that while HCD→BTI is intuitive to understand—HCD simply adds preexisting damage to the subsequent BTI stress—the flipped order possess a hidden feature. When BTI is applied prior to HCD, the high drain bias triggers the creation of secondary carriers which *accelerates* the recovery of oxide defects. However, super-imposed is the creation of interface traps caused by hot-carriers which clouds this effect in the measurements.

The presented work enables a detailed understanding of degradation and recovery processes in full bias space and ultimately stresses the conceptual limits of independent degradation regimes.

Appendix

A. Simulation Benchmark

Here, we motivate our simulation approach described in Section IV. As already discussed in [29], an increased drain bias accelerates the carriers in the channel which results in a *heated* carrier ensemble, described by a nonequilibrium EDF, and the generation of secondary carriers by II. Both, the (energetic) minority and majority carriers in the valence and conduction band, can interact with oxide defects and influence the respective nonradiative multiphonon transition rates given by Grasser [18] and Gös *et al.* [19]

$$k^{V,(C)} = \int_{V,(C)} g_{p,(n)(E)} f_{p,(n)(E)} A_{p,(n)(E)} f_{\text{ls}}(E) dE \quad (1)$$

with g being the density of states, f is the EDF, A accounts for the coupling between band and defect states and is approximated using a Wentzel–Kramer–Brillouin (WKB) factor, and f_{ls} represents the thermal average of the overlaps between initial and final state of the phonon system. As we have concluded in [29], the biggest impact onto the characteristics of oxide defects is due to the presence of secondary generated carriers.

In the following, we use three model variants to validate our approach: The **equilibrium model** $\text{NMP}_{\text{eq.}}$ only accounts for minority carriers (holes) and changes of the electric field and CC across the interface with applied drain bias. To access the interaction with secondary generated electrons we use an **extended model** $\text{NMP}_{\text{eq.+II}}$ where the effect of II is included within our DD-simulations, while the EDFs are approximated using Fermi–Dirac statistics. The computationally most expensive implementation is the full **nonequilibrium model** $\text{NMP}_{\text{neq.}}$ which includes the nonequilibrium EDFs for holes and electrons calculated as a solution of the bipolar BTE. Fig. 7 shows the simulation results for the different model variants for two stress conditions, namely $V_{\text{G}} = -2.8$ V and $V_{\text{D}} = -1.5$ V (Top panels) and $V_{\text{D}} = -2.8$ V (Bottom panels). One can clearly see that the $\text{NMP}_{\text{eq.}}$ model overestimates the degradation, and hence, the recovery due to oxide defects. The other two approaches, $\text{NMP}_{\text{eq.+II}}$ and $\text{NMP}_{\text{neq.}}$, yield similar and consistent results with only minor differences visible in the stress and recovery characteristics. These subtle differences arise due to the nonequilibrium EDFs and the heated carrier ensemble which is considered in the $\text{NMP}_{\text{neq.}}$ model.

Simulations for a single defect further highlight shortcomings of the $\text{NMP}_{\text{eq.}}$ model and validate the extended model scheme. Fig. 8 shows the characteristic capture and emission times of a single oxide defect (with a defect level of $E_T = -0.92$ eV and spatial position of $x_T = 66.5$ nm and $y_T = 1.61$ nm) characterized over a broad range of drain bias conditions. The data are taken from [29] where also a detailed discussion and analysis is presented. It was shown that the $\text{NMP}_{\text{neq.}}$ model properly captures the experimental trend and is able to explain the characteristic quantities for increased V_{D} bias, which is taken as a reference here (solid lines). The simplified extended model approach $\text{NMP}_{\text{eq.+II}}$ still captures the qualitative features of the full nonequilibrium model, in particular, the rapidly decreasing emission time with increasing drain bias. On the other hand, the $\text{NMP}_{\text{eq.}}$ model, which effectively only accounts for the interaction with holes in the valence band (due to the absence of electrons), fails to model the defect behavior and actually predicts an increasing τ_e.

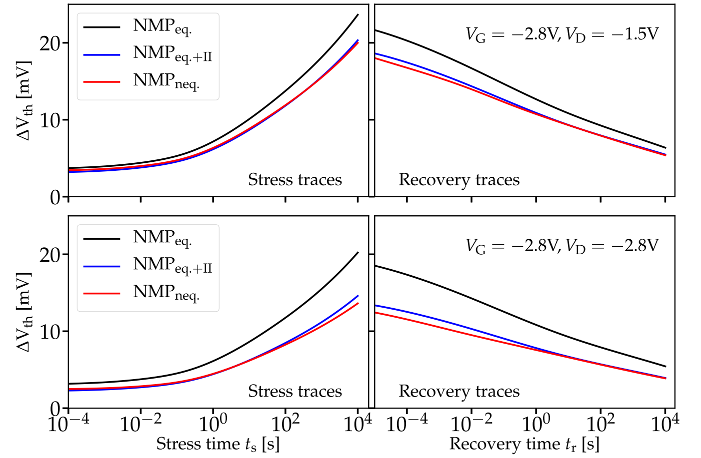

Fig. 7. Benchmark of the three different model realization for two stress conditions.

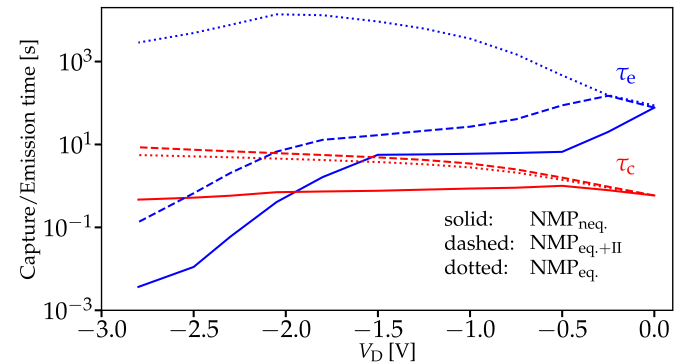

Fig. 8. Comparison of the simulation results obtained with the three models for a single oxide defect. The $\text{NMP}_{\text{neq.}}$ model is taken as a reference, see [29] for a detailed discussion.

The presented simulation results support the validity of the extended model $\text{NMP}_{\text{eq.+II}}$ and indicate that the impact of an increased drain bias onto oxide defects is mainly due to the interaction with secondary generated carriers by II. Finally, Table I shows the parameter set used for the simulations within this article.

B. Additional Measurements

The presented study utilizes the threshold voltage shift ΔV_{th} as a measure to quantify the degradation which allows

TABLE I
PARAMETERS OF THE FOUR-STATE NMP MODEL USED WITHIN THIS ARTICLE [18], [19]. THE POSITIVELY CHARGED STABLE CONFIGURATION 2 IS ALIGNED WITH THE VALENCE BAND AND USED AS A REFERENCE

	Parameter	μ	σ
E_1	trap level in state 1	−0.83 eV	0.33 eV
$E_{1'}$	trap level in state 1′	−0.52 eV	0.42 eV
$E_{2'}$	trap level in state 2′	0.43 eV	0.37 eV
$R_{12'}$	curvature ratio of 1 and 2′	1.1	0.48
$R_{1'2}$	curvature ratio of 1′ and 2	0.84	0.48
$S_{12'}$	relaxation energy 2′ → 1	2.74 eV	0.81 eV
$S_{1'2}$	relaxation energy 2 → 1′	1.68 eV	0.79 eV
$\varepsilon_{11'}$	activation energy 1 → 1′	0.43 eV	0.32 eV
$\varepsilon_{22'}$	activation energy 2 → 2′	1.16 eV	0.36 eV

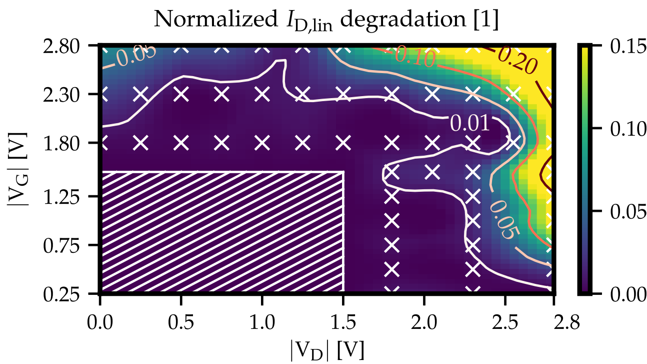

Fig. 9. Degradation map after 10 ks of stress using $I_{D,lin}$ as a measure to quantify the degradation. The results are qualitatively the same compared to the shift of the threshold voltage, see Fig. 2.

us to continuously monitor the device characteristics during recovery. On the other hand, most studies related to HCD focus on the degradation of the drain current, $I_{D,\text{ lin}}$ or $I_{D,\text{ sat}}$. Since the corresponding bias conditions would potentially introduce an additional stress during the recovery cycle and adversely affect the measurement results, we chose to measure ΔV_{th} in this article. However, additional measurements after 10 ks of stress, see Fig. 9, shows that the qualitative behavior during stress is the same when using $I_{D,\text{lin}}$ to quantify the degradation map.

C. Calibration of the Unstressed Devices

Furthermore, as mentioned in Section III, another vital component is a well-calibrated drift-diffusion simulation setup to properly represent the I_D–V_G characteristics of the fresh device. The simulations have been performed using the *GTSFramework* [16] and *minimos-NT* [17]. A drift-diffusion setup in conjunction with the well-calibrated *mobility model of minimos 6* (MM6) [36], [37] has been utilized. It accounts for the temperature dependence of the lattice mobility, the low-field mobility reduction due to ionized impurity scattering and surface scattering as well as the mobility reduction caused by a high field. Additionally, an improved modified local density approximation (IMLDA) [38] has been employed

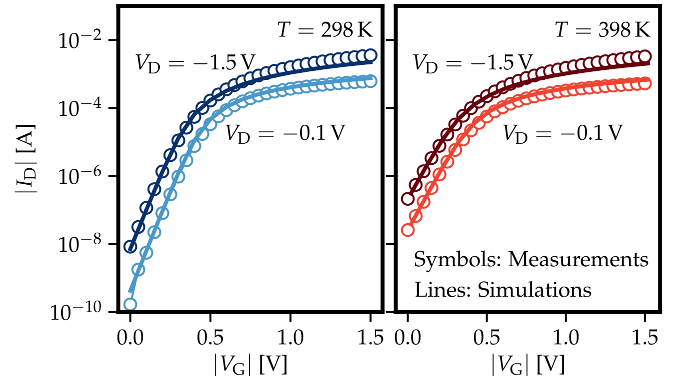

Fig. 10. DC current calibration in the linear and saturation regime for two different temperatures.

to account for the effects of hole inversion layer quantization in a pMOSFET and properly model the formation of a pinch-off region. The results are shown in Fig. 10. All subsequent calculations, such as the EDFs and the evaluation of the models, are based on the calibrated DD simulations.

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