A High Near-Infrared Sensitivity Over 70-dB SNR CMOS Image Sensor With Lateral Overflow Integration Trench Capacitor

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***Abstract*—This article presents a 16-μm pitch CMOS image sensor (CIS) exhibiting a high near-infrared (NIR) sensitivity and a 71.3-dB signal-to-noise ratio (SNR) with a linear response for high-precision absorption imaging. A 1.6-pF lateral overflow integration trench capacitor (LOFITreC) was introduced in each pixel to achieve a very high full well capacity (FWC), and a very low impurity concentration p-type Cz-Si substrate with a low oxygen concentration was employed for improving the NIR sensitivity. The developed CIS operated at a single exposure linear response wide dynamic range (DR) mode and a dual reset voltage mode for high SNR absorption imaging and achieved the maximum 24.3 Me$^-$ FWC, a wide spectral sensitivity from 200 to 1100 nm, and a photodiode quantum efficiency of 89.7%, 78.2%, and 26.7% at 860, 940, and 1050 nm, respectively. Both the spatial resolution and light sensitivity toward the NIR light were further improved by thinning the Si substrate and by applying a negative backside bias. Due to the LOFITreC, a record spatial efficiency of 95 ke$^-$/μm^2 with a 130-dB DR was achieved. As one of the applications of the developed CIS, the NIR absorption imaging toward a noninvasive blood glucose measurement was experimented and a diffusion of 5 mg/dl glucose was clearly visualized at 1050 nm in real time.**

***Index Terms*—Absorption imaging, CMOS image sensor (CIS), lateral overflow integration trench capacitor (LOFITreC), near-infrared (NIR) light, signal-to-noise ratio (SNR).**

I. Introduction

THE sensing technology utilizing a CMOS image sensor (CIS) is expected to be useful in the healthcare, medical, agriculture, automobile fields, and so on as a core technology in the IoT era. For high-precision sensing applications such as the absorption analysis and optical coherence tomography, the signal-to-noise ratio (SNR) shown in (1) is an important factor [1]–[3]

$$\mathrm{SNR} = 20\log_{10}\left(\frac{N_{\mathrm{sig}}}{\sqrt{\sqrt{N}_{\mathrm{sig}}^2 + n_{\mathrm{sys}}^2}}\right) \approx 20\log_{10}\sqrt{N}_{\mathrm{sig}}. \quad (1)$$

Here, N_{sig} is the number of signal electrons and n_{sys} is the input referred number of system noise in the electrons. An over 70-dB or higher SNR is required for high-precision absorption imaging that obtains absorbance in each pixel of the CIS [1], [2]. Under a high light illumination, the total noise is determined by the photon shot noise $(N_{\mathrm{sig}})^{1/2}$ so that over 10 Me$^-$ full well capacity (FWC) is required according to (1). In addition, to be utilized in many fields, a high quantum efficiency (QE) from the ultraviolet (UV) to near-infrared (NIR) waveband is required [4]. In a common four-transistor pixel CIS, the FWC is determined by the smaller one of the FWC of the floating diffusion (FD) formed by the p-n junction capacitance or by the FWC of the photodiode (PD) on the same Si substrate, therefore, the sensitivity and saturation are in a tradeoff relationship. Several CISs with advanced device technologies have been reported to be useful to achieve a high FWC so far, such as the CISs with a lateral overflow integration capacitor (LOFIC) to accumulate the overflow photoelectrons from the PD [4]–[6], organic photoconductive film (OPF) CISs [7], [8] with a large FD capacitance using a high-k metal-insulator-metal (MIM) capacitors [8], [9], and a complementary carrier collection CIS using an Si accumulation layer of the capacitive trench isolation in-pixel as a photocharge storage [10]. Of these, the capacitive trench isolation technology has been actively researched recently [11]–[13]. In addition, in order to achieve a high sensitivity in the NIR waveband, the methods to extend the effective penetration length of the light have been extensively studied [14], [15].

Previously the authors' group has developed a CIS with a 1-pF LOFIC on a very low dopant concentration p-type Si wafer [1]. An over 15 Me$^-$ FWC and a high QE in the NIR waveband were achieved simultaneously. However, the fill factor (FF) is limited to 10% in order to form the

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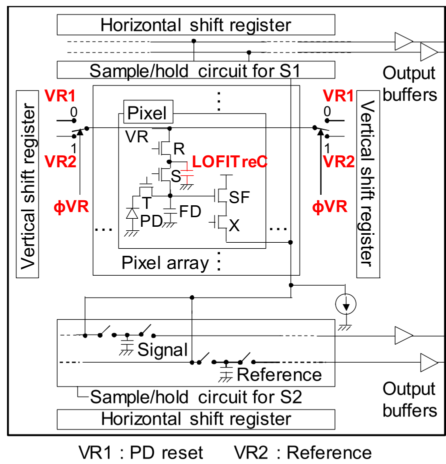


Fig. 1. Circuit block diagram of the developed CIS.

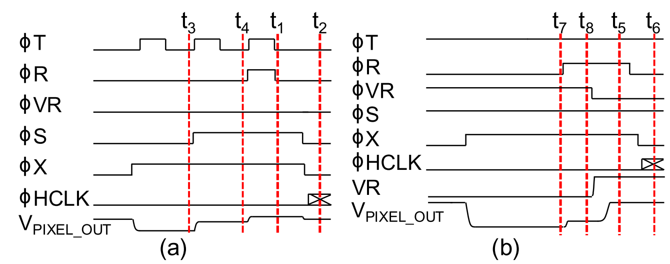


Fig. 2. Operation timing diagrams of the (a) WDR mode and (b) dual VR mode.

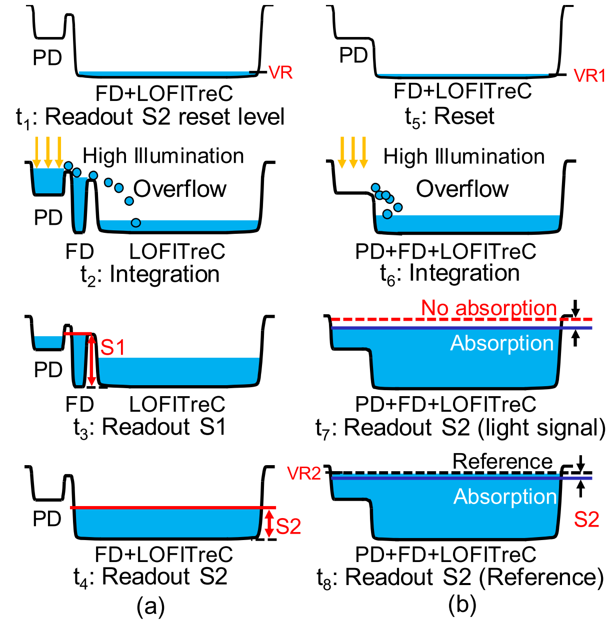


Fig. 3. Potential diagrams of the (a) WDR mode and (b) dual VR mode.

large capacitance area consisting of the MIM and metal-oxide-silicon (MOS) capacitors. In the IEEE International Electron Devices Meeting (IEDM) 2018, a 24.3 Me^- FWC CIS introducing a 1.6-pF lateral overflow integration trench capacitor (LOFITreC) to improve both the FWC and PD sensitivity was reported [16]. For a high-density in-pixel capacitor for the LOFIC, a 3-D-MIM capacitor structure can be an option as well if its leakage current is well suppressed for the usage of the photocharge integration. In this article, the combination of a front-side illumination and a trench capacitor employing high-integrity SiO_2 dielectric film was chosen so as to achieve both the high QE for the UV-visible-NIR waveband and high saturation. In this article, we additionally discuss in detail the NIR sensitivity and further improvement of the NIR sensitivity and spatial resolution by thinning the Si substrate and by applying a negative backside bias. Section II shows the key technologies of this article, Section III shows the measurement results and an application, and the conclusion is in Section IV.

II. Developed CIS With LOFITreC

A. Circuit Architecture and Operation

Fig. 1 shows the circuit block diagram of the developed CIS. The pixel consists of a pinned PD, a transfer gate (T), an FD, a source–follower (SF) driver, a pixel select switch (X), an overflow switch (S), an LOFITreC, and a reset gate (R). In this article, the 1.6-pF LOFITreC is integrated adjacent to the PD. In order to choose the voltage level of the voltage regulator (VR) either from VR1 or VR2, select switches are placed in each row at both the ends of the pixel array. The pulse ϕ VR is used to choose VR1 or VR2. VR1 and VR2 are the PD reset voltage and the reference voltage in the high FWC signal S2, respectively [2]. The sensor has two operation modes, that is, the wide dynamic range (WDR) mode and the dual VR mode. Fig. 2 shows the operation timing diagrams, and Fig. 3 shows the potential diagrams of each operation mode. In the WDR mode, the overflow-photoelectrons from the PD and FD are accumulated in the LOFITreC during the integration period (t_2). The high-sensitivity voltage signal S1 converted at the small capacitance FD in a low light illumination and the high saturation voltage signal S2 converted at FD + LOFITreC in a high light illumination are read out, whereby the WDR performance is achieved under a single exposure. This operation mode is employed to capture the images of low light for emission imaging and objects with a high light contrast. On the other hand, the dual VR mode is introduced to detect a fine difference of the light level under a high light illumination in techniques such as absorption imaging. VR2 is set to an intermediate value between the saturation level and the signal level. The S2 signal is the difference between the signal voltage level after the integration period and the VR2 (t_8). A fine difference of the light level under a high light illumination can be detected accurately by reading out the signal with a high-gain amplifier. Due to the introduction of the VR2, it is not necessary to read the PD reset voltage level VR1. Thus the VR1 can be increased to exceed the linear operational range of the SF in order to increase the FWC. In this mode, T and S are always turned on to further increase the FWC. In addition, the light signal and reference are read out from the same SF, thus fixed-pattern noise due to the pixel SF's threshold voltage variation can be removed.

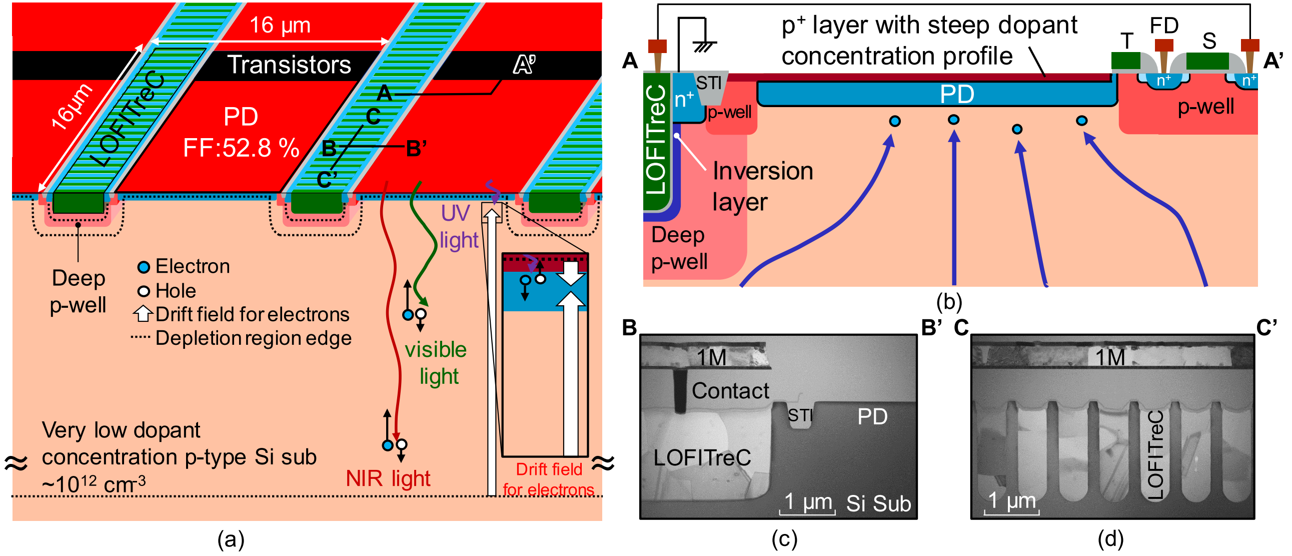


Fig. 4. Pixel cross-sectional diagrams of the (a) pixel array and (b) line A-A′, and cross-sectional TEM images of the (c) line B-B′ and (d) line C-C′.

B. High NIR Sensitivity With LOFITreC

Generally, the PD sensitivity is determined by the internal QE, FF, and micro lens efficiency. The improvement of the internal QE and FF is described in this section. This article aims to achieve a high sensitivity from UV to NIR by leveraging the material capability of the Si for applications used under the atmospheric conditions. The photoelectron current generated in the p-n junction consists of a drift component inside the depletion region and a diffusion component outside the depletion region. The internal QE, η, is shown in (2) [17]

$$\eta = \frac{1-R}{q\Phi_0}(J_{\rm dr} + J_{\rm diff}) = (1-R)\left(1 - \frac{\exp(-\alpha W_D)}{1+\alpha L_n}\right). \quad (2)$$

Here, R is the reflection coefficient, Φ_0 is the incident photon flux per unit area, α is the absorption coefficient, and L_n is the diffusion length of the electrons. In order to increase the internal QE, it is effective to extend the depletion width W_D. Depletion width due to the step p-n junction is expressed by (3) [17]

$$W_D = \sqrt{\frac{2\varepsilon_0\varepsilon_{\rm Si}}{q}\left(\frac{N_A+N_D}{N_A N_D}\right)(V_{\rm bi} - V_D)}. \quad (3)$$

Here, ε_0 is the permittivity of the vacuum, $\varepsilon_{\rm Si}$ is the permittivity of the Si, q is the unit electric charge, N_A and N_D are the acceptor and donor concentrations of the PD, $V_{\rm bi}$ is the built-in voltage, and V_D is the applied bias voltage, which is determined by the pinning voltage of a pinned PD at the beginning of the integration. In our previous works [2], [4], an Si wafer with an n-type substrate and a p-type epitaxial layer of 20-μm thickness and an acceptor concentration of 1.3×10^{15} cm^{-3} was employed. According to (3), the depletion width is about 1.3 μm when $V_D = -1.0$ V (with a pinning voltage of 1.0 V). The light penetration depth in the NIR waveband (>800 nm) is over 10 μm [18], therefore, the NIR light converted under the PD cannot be detected sufficiently. To enhance the QE in the NIR waveband by increasing the depletion width of the PD, a very low dopant concentration Si substrate in the order of 10^{12} cm^{-3}, based on a low oxygen concentration Czochralski-grown (Cz) method, was employed. The developed CIS uses the front-side illumination and metal shields so that the high NIR light illumination does not affect the charge storage floating nodes of the CIS. On the other hand, the cross talk between the pixels increases due to the diffusion component as the NIR light sensitivity improves. To suppress the cross talk, forming an electric field by applying a backside bias has been reported to be useful [19]. As shown later in this article, the NIR resolution was improved by thinning the Si substrate and applying a negative backside bias to form an electric field in the vertical direction to collect the photoelectrons converted in the neutral region under the depletion region. In addition, the surface high concentration p$^+$ layer of the PD with a steep dopant concentration profile was introduced in order to achieve a high sensitivity and high robustness toward the UV light waveband [20]. Consequently, a high QE in the UV-visible-NIR waveband can be obtained. The enlarged cross section diagram around the LOFITreC and PD and the TEM images of the LOFITreC are shown in Fig. 4. Previously the author's group has presented a burst video capturing the global shutter CIS with analog memories composed of a high capacitance density trench MOS capacitor formed aside the pixel array [21]. In this article, the trench MOS capacitor was integrated inside each pixel as the LOFITreC in the low impurity concentration Si substrate. The rectangle-shaped LOFITreCs were integrated densely in parallel as shown in Fig. 4(a) to improve the FF, and the PD sensitivity was improved accordingly. It is possible that the leakage current between the buried n-type layer of the pinned PD and the inversion layer of the LOFITreC occurs because of the low concentration Si substrate. To suppress the leakage current and keep the FF, a deep p-well (DPW) was formed to cover the entirety of the LOFITreC. The concentration of the DPW was optimized in order to obtain a uniform capacitance in the signal range of the LOFITreC. Furthermore,

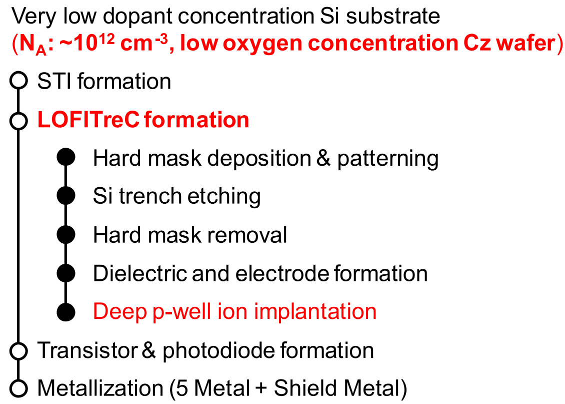


Fig. 5. Process flow of the developed CIS with LOFITreC.

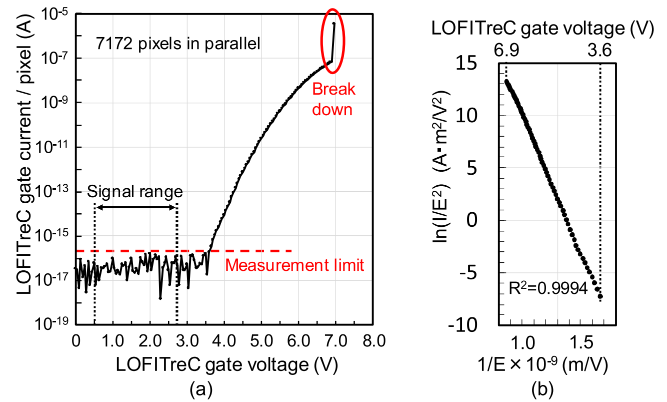


Fig. 6. (a) Current–voltage characteristic. (b) FN plot of a LOFITreC test pattern.

the p-well and DPW form a potential gradient so that the photoelectrons generated deep inside are drifted into the PD. To suppress the leakage current of the charge integration node of the LOFITreC, overflow-photoelectrons from the PD and FD capacitances are accumulated in the n^+-doped poly-Si buried electrode side. The inversion layer induced at the Si substrate-side interface and n^+ layer are connected to the ground.

C. Chip Fabrication

Fig. 5 shows the fabrication process flow of the developed CIS by a 0.18-μm 1-poly-Si 5-Metal layer CMOS process technology with a pinned PD. The Cz wafers were introduced as a cost-effective solution. In order to lower the impurity concentration using the Cz method wafer, a lower oxygen concentration is necessary. It is because oxygen acts as an n-type dopant after a certain thermal budget. Therefore, a low oxygen concentration Cz-Si wafer with about one order of magnitude lower oxygen concentration than usual was used in this prototype. The diameter of the Si wafer was 200 mm. The capacitance density of the LOFITreC was set to 24.3 fF/μm^2 considering the balance of the FWC and FF in this article. It is about five times higher capacitance density than that of a planar MOS capacitor for the same operation voltage. In order to compare the NIR resolution, the Si wafers with two final thicknesses of 600 and 300 μm were prepared. The Si substrate of 300-μm thickness was thinned by using the backside grinding and chemical mechanical polishing. A high concentration p^+ layer and metal electrode were formed on the backside surface, and the negative backside voltage was applied to the backside electrode uniformly over the entire chip. Fig. 6(a) and (b) shows the current–voltage characteristics and its Fowler–Nordheim (FN) plot of the LOFITreC, where 7 172 pixels were connected in parallel for the measurement. A high breakdown voltage and a very low current for the signal voltage range were obtained due to the high-integrity gate oxide film for the LOFITreC. Fig. 7 shows the micrograph of the developed CIS chip with $128^H \times 128^V$ effective pixels. Both the 52.8% FF and 1.6-pF capacitances were achieved due to the high capacitance density LOFITreC. The number of pixels can be increased under the same design.

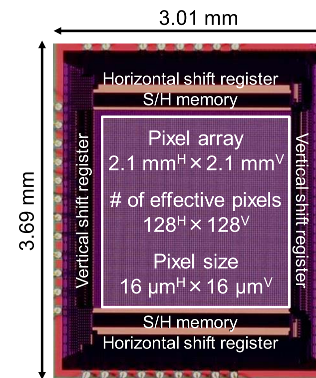


Fig. 7. Micrograph of the developed CIS chip.

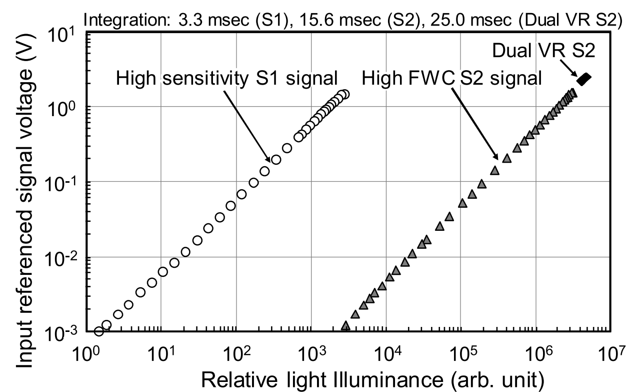


Fig. 8. Measured photoelectric conversion characteristics.

III. Measurement Results and Application

Fig. 8 shows the measured photoelectric conversion characteristics of the developed CIS. The low illumination side shows a high-sensitivity signal S1, and the high illumination side shows a high saturation signal S2 and an S2 signal on the dual VR mode. Using the WDR mode, an over 130-dB dynamic range (DR) with a linear response was obtained under a single exposure. Fig. 9 shows the enlarged view of the S2 signal using the dual VR mode. The first vertical axis shows the number of signal photoelectrons converted by the capacitance value of the LOFITreC and signal amplitude, and the second

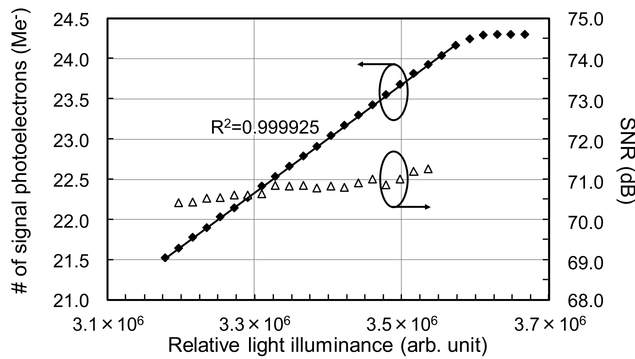


Fig. 9. Measured number of signal photoelectrons and SNR as a function of light illuminance for the S2 signal on the dual VR mode.

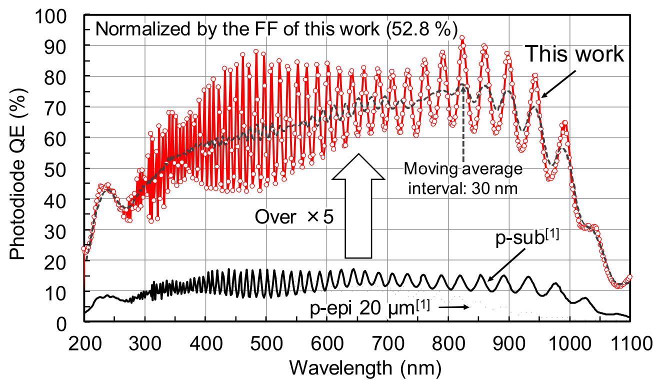


Fig. 10. Measured PD QE.

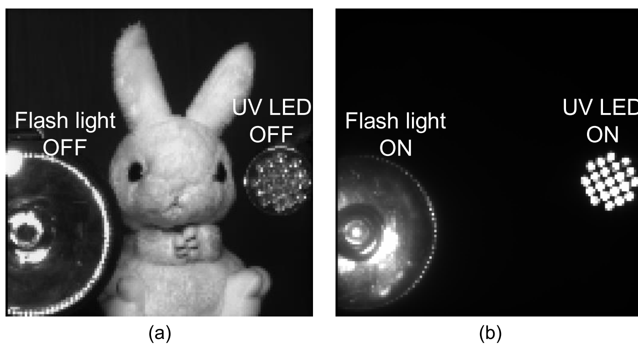
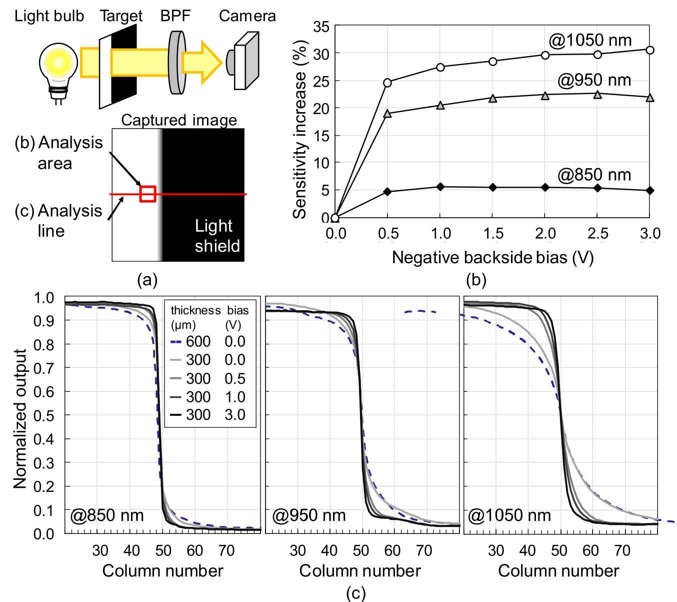


Fig. 11. Sample images by the (a) S1 signal and (b) S2 signal captured at 256 fps.

vertical axis shows the SNR. Under a high light illumination, a 24.3 Me⁻ FWC with a high linearity and over 70-dB SNR were obtained across the signal range due to the linearity of the LOFITreC. The readout noise of the S2 signal was 2.85 e⁻, and the thermal (kTC) noise of the LOFITreC was 508 e⁻. The dark current shot noise was much smaller than the kTC noise. The captured images on the dual VR mode are shown later in this article. Fig. 10 shows the measured PD QE of this article and of our previous works as references [1]. The measurement step of the wavelength and the bandwidth at each wavelength were 2 and 1 nm, respectively. Here, the measured QE was normalized by the FF of this article (52.8%). The dotted line shows the moving average of the measured



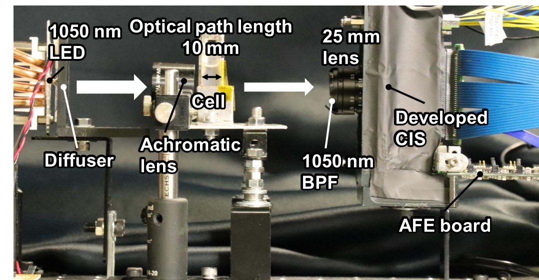


Fig. 12. ESF measurement (a) setup, (b) sensitivity increase, and (c) resolution improvement as a function of the negative backside bias toward the NIR light. In (c), the vertical axis is the signal output extracted from the acquired image. The larger output value, the brighter.

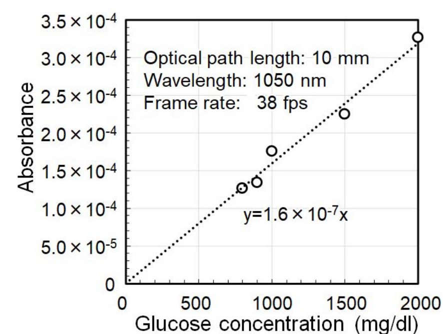


Fig. 13. Measurement setup of the glucose absorption imaging.

Glucose concentration (mg/dl)	Absorbance

Fig. 14. Absorbance as a function of glucose concentration.

PD QE over the 30-nm window. A high QE for the 200–1100-nm-wide wavebands, especially for the NIR region, was obtained with over five times improvement by increasing the FF due to the LOFITreC. For the NIR waveband, a PD QE of 89.7%, 78.2%, and 26.7% was achieved at 860, 940, and 1050 nm, respectively, for the perpendicular incidence. The moving average QE was 76.8%, 69.9%, and 25.3% at each wavelength. The wavelengths of 860 and 940 nm

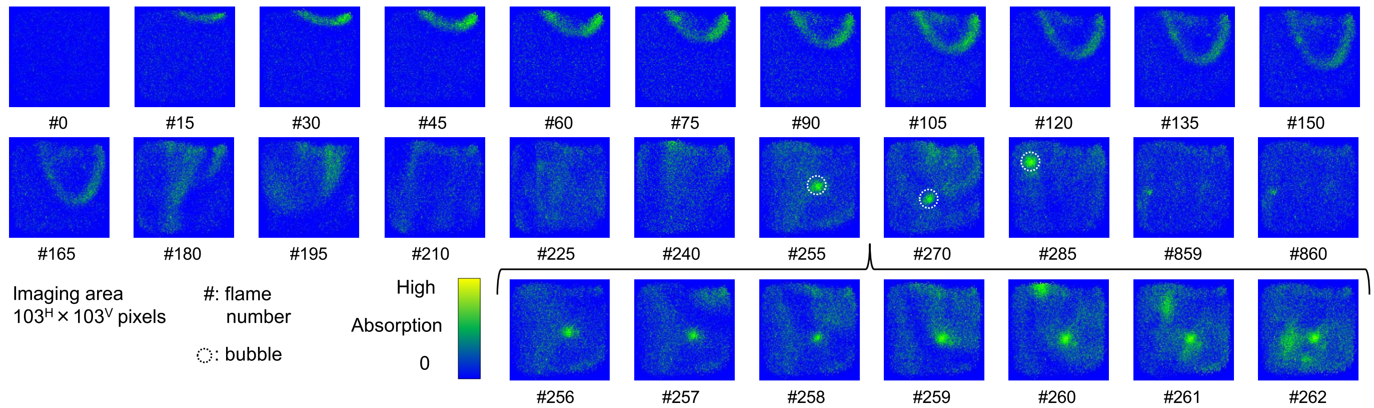


Fig. 15. Diffusion and convection of 5 mg/dl glucose in the saline solution visualized by an over 71-dB absorption imaging at 1050 nm captured with 30 fps.

are important as they are less affected by the background light and used for the time-of-flight applications and other applications. Here, the beats in the spectral sensitivity occur due to the interference of the intermetal dielectric layer on the PD composed of SiO_2 and SiN on the top as a passivation layer. Their thicknesses are 6450 and 190 nm, respectively. The half-width of the transmittance beats are 16–18 nm and 22–26 nm in 800–900 nm and 900–1100 nm, respectively, and they are well agreed as the calculated values. The light transmittance can be tuned by adjusting the thickness of the dielectric layer depending on the sensor application. The PD QE is equal to the internal QE when the transmittance of the dielectric layer above the PD is 1. Consequently, Fig. 10 indicates that the internal QE of the developed PD is higher than the upper envelope curve of the obtained data. Fig. 11 shows the sample images of a flash light, a UV LED (peak: 382 nm, full width at half-maximum: 12 nm,) and a stuffed animal captured at 256 fps with a F# 4.0 lens. The flash light includes an NIR light. Fig. 11(a) and (b) were captured by the high-sensitivity signal S1 under the background light and the high-saturation signal S2 while the flash light and the UV LED were tuned on, respectively. The results show that the developed CIS exhibits a sufficient resolution and single-shot WDR with a wide spectral response. In order to evaluate a spatial resolution index in the NIR waveband, the edge spread function (ESF) measurements were conducted as shown in Fig. 12. The measurement setup is shown in Fig. 12(a). A light bulb including the NIR light was used as the light source, and the edge pattern was irradiated with the uniform light through a diffuser. The bandpass filters (BPFs) of 850, 950, and 1050-nm were used when capturing the images. Fig. 12(b) shows the NIR light sensitivity as a function of the negative backside bias. Fig. 12(c) shows the negative backside bias dependence of the signal output for each wavelength. The resolution in the NIR waveband was improved by thinning the low impurity concentration Si substrate, and both the sensitivity and resolution were further improved by applying the negative backside bias. When the negative backside bias is applied, the leakage current occurs between the front-side p-wells and p-type substrate. The leakage current is about 3 mA with 3-V negative backside bias. A structure to suppress the leakage current is under development, however, the leakage current does not affect the total power consumption of the developed chip.

TABLE I
PERFORMANCE SUMMARY OF THE DEVELOPED CIS

Parameter		Value
Process technology		0.18 μm 1-poly-Si 5-Metal CMOS with pinned PD
Power supply voltage		3.3 V
Die size		3.01 mm^H×3.69 mm^V
# of effective pixels		128^H×128^V
Pixel size		16 μm^H×16 μm^V
Fill factor		52.8 %
Maximum frame rate		685 fps @20 MHz
Capacitance of FD		2.3 fF
Capacitance of LOFITreC		1.6 pF
Full well capacity	High sensitivity S1	15.7 ke^- (61.3 $e^-/\mu m^2$)
	High saturation S2	10.2 Me^- (39.8 $ke^-/\mu m^2$)
	Dual VR S2	24.3 Me^- (94.9 $ke^-/\mu m^2$)
Dynamic range		130 dB
Maximum SNR		71.3 dB
Spectral sensitivity range		200 nm-1100 nm
Photodiode quantum efficiency (Moving average over 30 nm window)		89.7 % (76.8 %) @860 nm 78.2 % (69.9 %) @940 nm 26.7 % (25.3 %) @1050 nm

As an application of the developed CIS, a glucose absorption imaging for the noninvasive blood glucose measurement was experimented by over 71-dB SNR on the dual VR mode. Recently, the number of patients with diabetes has increased rapidly [22]. Accordingly, the demand is increasing for devices that can measure blood glucose in real time without pain. In order to measure the blood glucose from very low to high levels with high precision, the resolution of 5 mg/dl is considered to be required [1]. Fig. 13 shows the experimental setup of the glucose absorption imaging as a fundamental step toward the noninvasive blood glucose measurement. A quartz cell with an optical path length of 10 mm, a physiological saline solution simulating blood, a 1050-nm LED as a light source, and a 1050-nm BPF were employed. Here, the wavelength 1050 nm corresponds to an absorption peak of glucose in the spectral response of Si. Fig. 14 shows the absorbance as a function of glucose concentration measured by the developed CIS. The calibration curve was successfully obtained by the developed system. Fig. 15 shows the captured absorption images when 5-mg/dl glucose aqueous

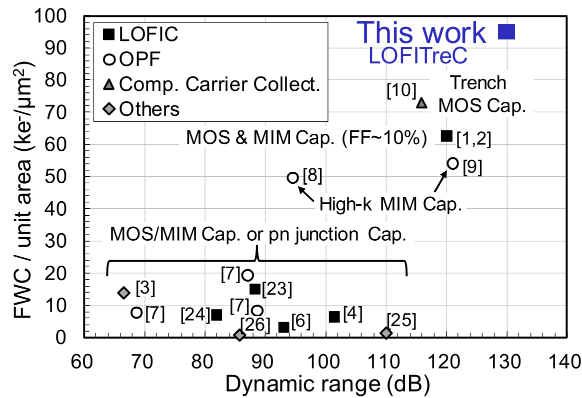


Fig. 16. FWC/unit area as a function of DR with other linear response CISs.

solution was dropped into the cell with the physiological saline solution with 30 fps. The drop, diffusion, and convection of the glucose aqueous were clearly visualized on the dual VR mode. Based on the captured images, the concentration can be extracted accurately by removing the inhibiting substances such as bubbles in this case. The glucose measurement with the real blood glucose using the developed CIS will be the next step. The developed CIS is expected to be useful for other applications such as the blood flowmeter, liquid or gas concentration imaging by utilizing its high SNR, and wide spectral sensitivity performances.

Table I shows the performance summary of the developed CIS. Fig. 16 shows the FWC per unit area as a function of the DR, compared to other linear response CISs [1]–[4], [6]–[10], [16], [23]–[26]. A record area signal density of 95 ke$^-$/μm^2 with a 130-dB DR was achieved.

IV. Conclusion

This article reported a high NIR sensitivity and an over 70-dB SNR CIS with a LOFITreC on a low impurity concentration Si substrate. The developed CIS achieved a 24.3 Me$^-$ FWC and a wide spectral sensitivity range from 200 to 1100 nm. A diffusion of 5-mg/dl glucose in the physiological saline solution was clearly visualized at 1050 nm on the dual VR mode. The developed CIS is promising for the IoT sensing application in many fields such as healthcare, medical, agriculture, automobile fields, and so on.

References

[1] Y. Fujihara *et al.*, “A multi spectral imaging system with a 71dB SNR 190-1100nm CMOS image sensor and an electrically tunable multi bandpass filter,” *ITE Trans. Media Technol. Appl.*, vol. 6, no. 3, pp. 187–194, 2018.

[2] Y. Aoyagi, Y. Fujihara, M. Murata, H. Shike, R. Kuroda, and S. Sugawa, “A CMOS image sensor with dual pixel reset voltage for high accuracy ultraviolet light absorption spectral imaging,” *Jpn. J. Appl. Phys.*, vol. 58, no. SB, Mar. 2019, Art. no. SBBL03.

[3] G. Meynants *et al.*, “700 frames/s 2 MPixel global shutter image sensor with 2 Me-full well charge and 12μm pixel pitch,” in *Proc. IISW*, 2015, pp. 409–412.

[4] S. Nasuno, S. Wakashima, F. Kusuhara, R. Kuroda, and S. Sugawa, “A CMOS image sensor with 240 μV/e-conversion gain, 200ke-full well capacity and 190-1000nm spectral response and high robustness to UV,” *ITE Trans. Media Technol. Appl.*, vol. 4, no. 2, pp. 116–122, 2016.

[5] S. Sugawa *et al.*, “A 100dB dynamic range CMOS image sensor using a lateral over flow integration capacitor,” in *IEEE ISSCC Dig. Tech. Papers*, 2005, pp. 352–353.

[6] S. Adachi, W. Lee, N. Akahane, H. Oshikubo, K. Mizobuchi, and S. Sugawa, “A 200-μV/e$^-$ CMOS image sensor with 100-ke$^-$ full well capacity,” *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 823–830, Apr. 2008.

[7] M. Mori *et al.*, “Thin organic photoconductive film image sensors with extremely high saturation of 8500 electrons/μm^2,” in *Proc. Symp. VLSI Tech.*, Jun. 2013, pp. 22–23.

[8] K. Nishimura *et al.*, “An 8K4K-resolution 60fps 450ke$^-$-saturation-signal organic-photoconductive-film global-shutter CMOS image sensor with in-pixel noise canceller,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2018, pp. 82–83.

[9] M. Takase *et al.*, “An over 120 dB wide-dynamic-range 3.0 μm pixel image sensor with in-pixel capacitor of 41.7 fF/um^2 and high reliability enabled by BEOL 3D capacitor processs,” in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2018, pp. 71–72.

[10] F. Lalanne, P. Malinge, D. Hérault, C. Jamin-Mornet, and N. Virollet, “A 750 K photocharge linear full well in a 3.2 μm HDR pixel with complementary carrier collection,” *Sensors*, vol. 18, no. 2, p. 305, Jan. 2018.

[11] A. Tournier *et al.*, “A HDR 98dB 3.2μm charge domain global shutter CMOS image sensor,” in *IEDM Tech. Dig.*, Dec. 2018, pp. 229–232.

[12] Y. Kumagai *et al.*, “Back-illuminated 2.74μm-Pixel-Pitch global shutter CMOS image sensor with charge-domain memory achieving 10k e-saturation signal,” in *IEDM Tech. Dig.*, Dec. 2018, pp. 237–240.

[13] F. Kaklin, J. M. Raynor, and R. K. Henderson, “High voltage generation using deep trench isolated photodiodes in a back side illuminated process,” in *IEDM Tech. Dig.*, Dec. 2018, pp. 743–746.

[14] J. Solhusvik *et al.*, “A 1392$\times$ 976 2.8 μm 120 dB CIS with per-pixel controlled conversion gain,” in *Proc. IISW*, 2017, p. 30.

[15] I. Oshiyama *et al.*, “Near-infrared sensitivity enhancement of a back-illuminated complementary metal oxide semiconductor image sensor with a pyramid surface for diffraction structure,” in *IEDM Tech. Dig.*, Dec. 2017, pp. 397–400.

[16] M. Murata *et al.*, “A 24.3Me$^-$full well capacity CMOS image sensor with lateral overflow integration trench capacitor for high precision near infrared absorption imaging,” in *IEDM Tech. Dig.*, Dec. 2018, pp. 225–228.

[17] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. Hoboken, NJ, USA: Wiley, 2006.

[18] M. A. Green and M. J. Keevers, “Optical properties of intrinsic silicon at 300 k,” *Progr. Photovolt., Res. Appl.*, vol. 3, no. 3, pp. 189–192, 1995.

[19] K. Stefanov, A. Clarke, J. Ivory, and A. Holland, “Design and performance of a pinned photodiode CMOS image sensor using reverse substrate bias,” *Sensors*, vol. 18, no. 2, p. 118, Jan. 2018.

[20] R. Kuroda *et al.*, “A highly ultraviolet light sensitive and highly robust image sensor technology based on flattened Si surface,” *ITE Trans. Media Technol. Appl.*, vol. 2, no. 2, pp. 123–130, 2014.

[21] M. Suzuki *et al.*, “An over 1Mfps global shutter CMOS image sensor with 480 frame storage using vertical analog memory integration,” in *IEDM Tech. Dig.*, Dec. 2016, pp. 212–215.

[22] *IDF Diabetes Atlas*, Int. Diabetes Fed., Brussels, Belgium, 2017.

[23] Y. Sakano *et al.*, “224-ke saturation signal global shutter CMOS image sensor with in-pixel pinned storage and lateral overflow integration capacitor,” in *Proc. Symp. VLSI Circuits*, Jun. 2017, pp. 250–251.

[24] S. Sakai, Y. Tashiro, R. Kuroda, and S. Sugawa, “A 2.8 μm pixel-pitch 55 ke-full-well capacity global-shutter complementary metal oxide semiconductor image sensor using lateral overflow integration capacitor,” *Jpn. J. Appl. Phys.*, vol. 52, no. 4S, Dec. 2013, Art. no. 04CE01.

[25] M. Kobayashi *et al.*, “4.5 A 1.8erms$^-$temporal noise over 110dB dynamic range 3.4μm pixel pitch global shutter CMOS image sensor with dual-gain amplifiers, SS-ADC and multiple-accumulation shutter,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 74–75.

[26] B. Fowler *et al.*, “Wide dynamic range low light level CMOS image sensor,” IISW, Bengaluru, India, White Paper 48, 2009.