Consistent Surface-Potential-Based Modeling of Drain and Gate Currents in AlGaN/GaN HEMTs

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***Abstract*—In this article, the gate current in AlGaN/GaN high-electron mobility transistors is modeled in a surface potential-based compact model. The thermionic emission, the Poole–Frenkel emission, and the Fowler–Nordheim tunneling are the dominant mechanisms for the gate current in the forward- and reverse-bias regions. These conduction mechanisms are modeled within the framework of the ASM-GaN compact model, which is a physics-based industry-standard model for GaN HEMTs, hence yielding a consistent model for the drain and gate currents. The proposed model captures the gate voltage, drain voltage, temperature, and gate-length dependencies of the gate current. The results of dc gate-leakage measurements of two GaN HEMT, differing only in terms of gate length, over a wide range of temperature, showing these current-conduction mechanisms, are presented, and the proposed model is validated accordingly. The developed gate current model, implemented in Verilog-A, is in excellent agreement with the experimental data.**

***Index Terms*—Compact model, Fowler–Nordheim (FN) tunneling, GaN high-electron mobility transistor (HEMT), gate leakage current, Poole–Frenkel (PF) emission, thermionic emission (TE).**

I. Introduction

THE GaN-based high-electron mobility transistors (HEMTs) have been proven to possess significantly superior characteristics in comparison to other III/V material systems. One of the more significant properties of GaN is the high value of the critical electric field. This allows for GaN HEMT devices to attain a much higher RF power density. In other words, compared against other III/V or silicon-based devices, GaN HEMTs are able to achieve the same level of output power for a much smaller device size.

There, however, remain several challenges in the design of GaN HEMTs, among which is excessive gate leakage [1]–[3], as it impacts the performance of the device and circuits [4]. For instance, high gate leakage or, as reported by some authors, the effects leading to high gate leakage (such as surface defect charges), results in a significant reduction in the breakdown voltage and increase in the noise figure [5], [6]. It also impacts circuits with high load impedance at the gate terminal or circuits in which the dc gate current can significantly charge a capacitor [7]. Moreover, the performance of both digital and analog circuits can get affected by the noise associated with the gate current [5], [8]. These concerns showcase the importance of accurate modeling of the gate leakage, which mostly has either been ignored in compact models for GaN HEMTs or been implemented empirically.

A compact model is a concise mathematical description of the terminal characteristics of a device as a function of the input conditions. In the ASM GaN compact model, this mathematical relationship is developed from device physics, starting with the fundamental device physics governed by Schrfördinger's and Poisson's equations in the quantum well of the GaN HEMT [9]. In this model, the terminal device characteristics are functions of the surface potential ψ, which, in turn, is a function of the input bias, device geometry, and temperature. The functional forms are derived based on the relevant device physics.

In [4], a surface-potential-based model for gate leakage is developed within the framework of the ASM-GaN compact model [10], [11], presenting analytical models for the thermionic emission (TE) and Poole–Frenkel (PF) emission mechanisms that are dominant mechanisms for the gate current in the forward- and reverse-bias regions, respectively. In this work, we shall present an alternative, yet simpler and more accurate, surface-potential-based model for gate current, taking into account several temperature and electric-field dependencies, which are absent in [4], and also the presence of the Fowler–Nordheim (FN) mechanism, which is not modeled in [4], which is a second mechanism that can dominate in the reverse-bias condition.

The model developed in this work is within the framework of the ASM-GaN compact model, which is a physics-based

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industry-standard model for GaN HEMTs, which showcases as a promising tool for improving the accuracy and versatility of today's RF and power GaN-based circuit simulations. In addition to the core modeling of dc-IV and intrinsic capacitances, in the ASM-GaN compact model, flicker noise, thermal noise [12], [13], trapping [11], and a capacitance model in the presence of different combinations of gate and source field plates [14], [15] are also modeled. In this work, we shall develop an accurate, yet simple, surface-potential-based model for the gate-leakage current. The developed model begins with the calculation of the surface potential at the source and drain sides of the device channel, which then enters the calculation of both the drain and gate currents. Hence, the model gives consistent solutions for the drain and gate currents.

This article is organized as follows. Section II presents the structures of the devices under test and the results of measurements performed on these devices. Section III presents the developed model for the gate current. Section IV presents and discusses the results of the proposed model, showing the excellent fit of the model to the measurement results. Finally, Section V draws conclusions.

II. HEMT Structures and Measurement Results

This article reports the measurement and modeling results of two AlGaN/GaN Schottky HEMTs grown on 200-mm p-Si substrates by MOCVD, with no applied surface passivation, with the schematic shown in Fig. 1, and of the following geometries:

1) gate lengths L of 5 and 2.5 μm;
2) gate width $W = 50\,\mu$m;
3) thickness T_{BAR} of the AlGaN layer = 21 nm;
4) length L_{GS} of the gate–source access region = 2 μm;
5) length L_{GD} of the gate–drain access region = 2.5 μm;
6) number of gate fingers NF = 2.

The dc gate current (I_G)–gate–source voltage (V_{GS}) characteristic and the drain current (I_D)–gate–source voltage (V_{GS}) (transfer) characteristic of the devices under test were measured at various temperatures. The results are shown in Figs. 2–5, with the following details.

1) The temperature dependence of the gate current is depicted in the measurement results of Fig. 2, which shows the I_G–V_{GS} characteristic of the device with gate length $L = 5\,\mu$m in both the linear and semilogarithmic scales, at the drain–source voltage $V_{\mathrm{DS}} = 0$ V, at four different ambient temperatures T = 25 °C, 100 °C, 150 °C, and 200 °C.
2) The gate-length dependence of the gate current is depicted in the measurement results of Fig. 3, which shows the measured I_G–V_{GS} characteristics of the device with $L = 5\,\mu$m and the device with $L = 2.5\,\mu$m in both the linear and semilogarithmic scales, at T = 25 °C, at drain-to-source voltages ranging from $V_{\mathrm{DS}} = 0$ to 3 V.
3) The $\partial I_G/\partial V_{\mathrm{GS}}$–$V_{\mathrm{GS}}$ characteristic of the device with $L = 5\,\mu$m is shown in the measurement results of Fig. 4, which shows this characteristic at T = 25 °C, at drain-to-source voltages ranging from $V_{\mathrm{DS}} = 0$ to 3 V.

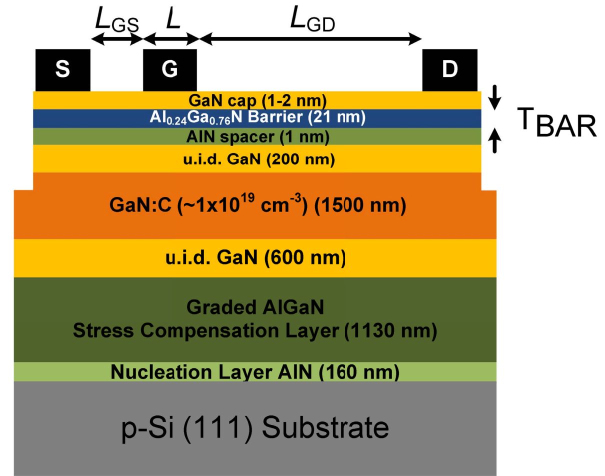

Fig. 1. Schematic of the AlGaN/GaN HEMT under test.

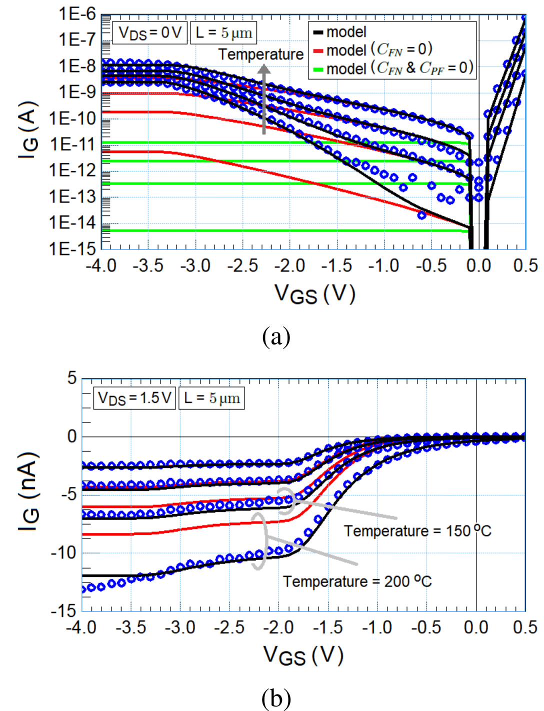

Fig. 2. Measured (symbol) and simulated (line) gate current (I_G)–gate–source voltage (V_{GS}) characteristics for the device with gate length $L = 5\,\mu$m at four different ambient temperatures T = 25°C, 100°C, 150°C, and 200°C, at the drain–source voltage (a) V_{DS} = 0 V in the semilogarithmic scale (b) V_{DS} = 1.5 V in a linear scale. Simulation results are also shown for V_{DS} = 0 V when the parameter C_{FN} in (35) is set to 0, yielding zero FN current, and when the parameters C_{FN} and C_{PF} in (19) are set together to 0, yielding zero FN and PF currents, and for V_{DS} = 1.5 V when the parameter C_{FN} is set to 0, showing that the PF current becomes a main contributor to the gate current at high temperatures.

4) The transfer characteristic of the I_D–V_{GS} characteristic of the device with $L = 5\,\mu$m is shown in Fig. 5, which shows this characteristic (along with the I_G-V_{GS} characteristic) in the semilogarithmic scales at T = 25 °C.

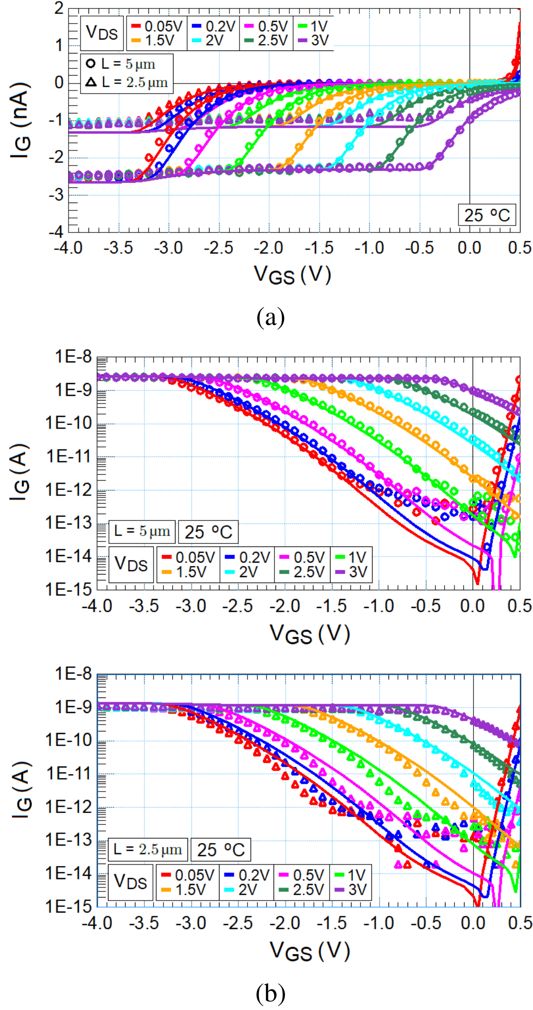

Fig. 3. Measured (symbol) and simulated (line) gate current (I_G)–gate–source voltage (V_{GS}) characteristics for the device with gate length $L = 5$ μm and the device with gate length $L = 2.5$ μm in (a) linear scale and (b) semilogarithmic scale, at ambient temperatures $T = 25°$C, and drain–source voltages V_{DS} ranging from 0.05 to 3 V.

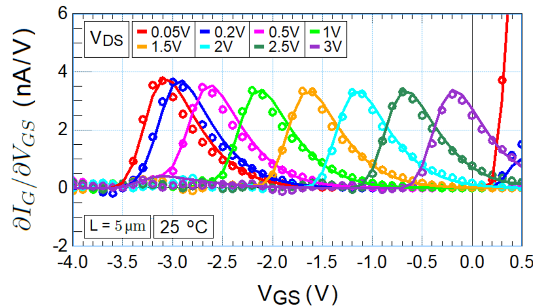

Fig. 4. Measured (symbol) and simulated (line) $\partial I_G/\partial V_{GS}$–$V_{GS}$ characteristics for the device with gate length $L = 5\mu$m, at ambient temperature $T = 25°$C, and drain–source voltages V_{DS} ranging from 0 to 5 V, with a step size of 1 V.

III. Gate-Current Model

The reverse-bias gate current is mainly governed by the PF emission and FN tunneling [16] at medium-to-high reverse bias, whereas TE plays a vital role in the forward-bias region [1], [2], [4], [16], [17]. These current components

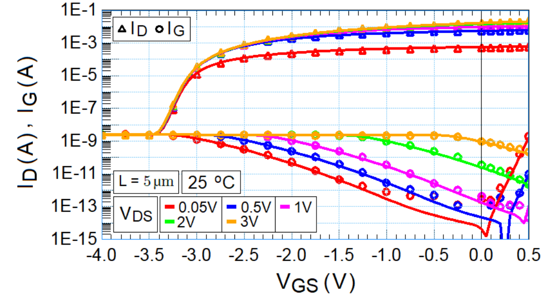

Fig. 5. Measured (symbol) and simulated (line) gate current (I_G)–gate–source voltage (V_{GS}) and drain current (I_D)–V_{GS} characteristics in the semilogarithmic scale, at ambient temperature $T = 25°$C, and drain–source voltages V_{DS} ranging from 0.05 to 3 V.

together attribute the gate current for a wide bias range. In this section, we shall develop an accurate model for these three components of the gate current within the framework of the ASM-GaN compact model.

A. TE Model

In a Schottky contact, TE is the dominant conduction mechanism in the forward-bias range. The current density–voltage characteristics of a Schottky contact (or diode) is given by [18]

$$J_{\mathrm{TE}} = J_{\mathrm{TE0}}(\exp[V/(\eta V_{\mathrm{th}})] - 1) \tag{1}$$

where V is the applied voltage, η is the ideality factor, and $V_{\mathrm{th}} = K_B T$ is the thermal voltage, where K_B is Boltzmann's constant and T is the temperature, and J_{TE0} is the reverse saturation current density and is given by

$$J_{\mathrm{TE0}} = A^* T^2 \exp(-q\phi_{\mathrm{TE}}/V_{\mathrm{th}}) \tag{2}$$

where ϕ_{TE} is the Schottky barrier height and A^* is the effective Richardson's constant, which is given by [18]

$$A^* = 4\pi q m^* k_B^2/h^3 \tag{3}$$

where h is Planck's constant, k_B is Boltzmann's constant, and m^* is the electronic effective mass in the AlGaN barrier.

In a GaN HEMT, the applied voltage varies along the channel, from the source end of the channel toward the drain end of the channel. To accurately model the TE current, a distributed network of the Schottky diodes is needed. This can be achieved by modeling the intrinsic region of the GaN HEMT as a series of transistors and associating with each transistor a Schottky diode, which is modeled by integrating (1) along the channel length and width of each transistor. In [4], this complex structure is simplified by integrating (1) along the channel length and width to obtain the TE current I_{TE}. The gate-to-source and gate-to-drain TE current components, denoted, respectively, as I_{TES} and I_{TED}, are then implemented using the 60:40 partitioning scheme, i.e., $I_{\mathrm{TES}} = 0.6\, I_{\mathrm{TE}}$ and $I_{\mathrm{TED}} = 0.4\, I_{\mathrm{TE}}$. An alternative, but simpler, model is to consider two diodes: one for the gate-to-source TE current and another for the gate-to-drain TE current. The two current components, denoted, respectively, as I_{TES} and I_{TED}, are obtained by integrating J_{TE} over the gate length

and width, setting the applied gate voltage to, respectively, the intrinsic gate-to-source voltage $V_{G_iS_i}$ and the intrinsic gate-to-drain voltage $V_{G_iD_i}$. The resulting TE current components are

$$I_{\mathrm{TE}(S,D)} = \frac{1}{2}\mathrm{NF}WLJ_{\mathrm{TE0}}\left[\exp\left(\frac{V_{G_i(S_i,D_i)}}{\eta V_{\mathrm{th}}}\right) - 1\right] \tag{4}$$

where NF is the number of fingers. The prefactor 0.5 in (4) accounts for the fact that ideally at $V_{\mathrm{DS}} = 0$ V and $I_{\mathrm{TES}} = I_{\mathrm{TED}} = I_{\mathrm{TE}}/2$.

To account for the simplifications encountered in the above-mentioned calculations, we introduce the following enhancements in the model. First, the gate-to-source voltage $V_{G_iS_i}$ and the gate-to-drain voltage $V_{G_iD_i}$ in (4) are replaced with the following effective voltages:

$$V_{\mathrm{GS,eff}} = \beta_S V_{G_iS_i} + (1-\beta_S)V_{G_iD_i} \tag{5}$$
$$= V_{G_iD_i} + \beta_S V_{D_iS_i} \tag{6}$$
$$V_{\mathrm{GD,eff}} = \beta_D V_{G_iS_i} + (1-\beta_D)V_{G_iD_i} \tag{7}$$
$$= V_{G_iD_i} + \beta_D V_{D_iS_i} \tag{8}$$

where the model parameter $0 \le \beta_S \le 1$, hence $V_{G_iD_i} \le V_{\mathrm{GS,eff}} \le V_{G_iS_i}$, and the model parameter $0 \le \beta_D \le 1$, hence $V_{G_iD_i} \le V_{\mathrm{GD,eff}} \le V_{G_iS_i}$. Note that introducing these emperical parameters result in $V_{G_iD_i}$ dependence of the gate-to-source leakage current and $V_{G_iS_i}$ dependence of the gate-to-drain leakage current. Second, the Schottky barrier height ϕ_{TE} at the drain side of the channel is slightly altered with respect to the one at the source side of the channel as

$$\phi_{\mathrm{TES}} = \phi_{\mathrm{TE}} \tag{9}$$
$$\phi_{\mathrm{TED}} = \phi_{\mathrm{TE}} + \Delta\phi \tag{10}$$

where ϕ_{TES} and ϕ_{TED} are the source- and drain-side Schottky barrier heights and $\Delta\phi$ is a model parameter. Note that this modification of the Schottky barrier height also accounts for possible nonidealities in the structure of the GaN HEMT, which can affect the Schottky barrier height along the channel.

Our analysis of the measured characteristics of the devices under test shows, in agreement with the results reported in the literature [17], [19], that accurate modeling of these characteristics requires inclusion of temperature dependence for the Schottky barrier height ϕ_{TE} and the ideality-factor parameter η as

$$\phi_{\mathrm{TE},T} = \phi_{\mathrm{TE}} + K_{\phi_{\mathrm{TE}}}(T/T_n - 1) \tag{11}$$
$$\eta_T = \eta + K_\eta(T/T_n - 1) \tag{12}$$

where T_n is the nominal temperature and $K_{\phi_{\mathrm{TE}}}$ and K_η are the model parameters.

B. PF Model

The TE current over the Schottky barrier is too small to explain the observed excess gate leakage current in AlGaN/GaN HEMTs. This excess leakage current is, rather, attributed either partially or completely to the leakage path in III-nitride semiconductors resulting from the presence of threading dislocations in the AlGaN barrier. The conductive nature and the carrier-capture radius of each individual dislocation depend on factors such as types and distribution of dislocations and III/V ratios during epitaxial growth [1], therefore, it is difficult to incorporate the impact of threading dislocations into a gate leakage model. The combined effect of dislocations is, rather, modeled as a continuous band of conductive states (or a continuum of states). The gate leakage in the reverse bias condition is then modeled as the flow of the electrons that are emitted from trap states onto this continuum of states, from the gate contact toward the channel through the AlGaN barrier [1], as shown in Fig. 6. The flow of electrons is caused by the vertical electric field $E_\perp$ in the AlGaN layer resulting from the application of the gate voltage. In addition to causing the flow of electrons, the electric field in the AlGaN layer also enhances the emission of the electrons from the trap states onto the continuum of states. This mechanism is called the PF mechanism.

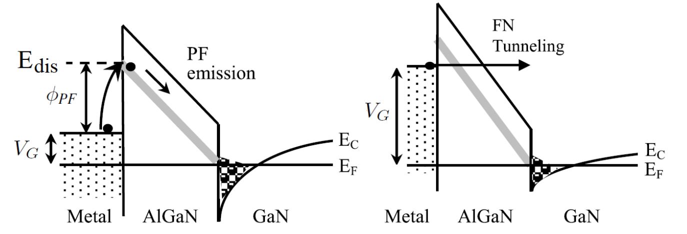

Fig. 6. Conduction band edge diagram of AlGaN/GaN HEMT for medium reverse gate voltage [16]. The left-hand-side energy band diagram describes the physical mechanism of the PF emission at a medium applied gate bias. The trap state is assumed to be very close to the metal Fermi level, and the energy level associated with the continuum of states, denoted as E_{dis} and marked in gray, is at a height ϕ_{PF} from the metal Fermi level, which varies with the electric field. The right-hand-side figure describes the FN tunneling process.

The relation between current density (J_{PF}) and electric field ($E_\perp$) in the PF conduction is given by [18]

$$J_{\mathrm{PF}} = E_\perp C_{\mathrm{PF}} \exp\left(-q\phi_{\mathrm{PF}}/V_{\mathrm{th}}\right) \tag{13}$$

where C_{PF} is a model parameter and

$$\phi_{\mathrm{PF}} = \phi_{\mathrm{PF0}} - \sqrt{qE_\perp/(\pi\tilde{\epsilon})} \tag{14}$$

where ϕ_{PF0} is the zero-electric-field barrier height, and $\tilde{\epsilon}$ is the high-frequency dielectric permitivity of the AlGaN layer and is given by

$$\tilde{\epsilon} = \kappa\epsilon \tag{15}$$

where κ is a model parameter. As can be noticed, the potential barrier ϕ_{PF} decreases with increase in electric field.

The calculation of the PF current I_{PF} begins with calculating the electric $E_\perp$ as [2]

$$E_\perp = [q\sigma_p - C_g(V_{G0} - \psi)]/\epsilon \tag{16}$$

where σ_p is the sum of the piezoelectric polarization charge in the barrier and the difference between spontaneous polarization charge in the barrier and the buffer, C_g is the gate capacitance per unit area ($=T_{\mathrm{BAR}}/\epsilon$, where T_{BAR} is the AlGaN thickness), and V_{G0} is the gate overdrive, which equals the difference between the applied gate voltage and the

work-function difference (in volt) between the gate contact and the AlGaN layer V_{OFF}

$$V_{G0} = V_G - V_{\mathrm{OFF}}. \quad (17)$$

This expression for electric field accounts for the presence of the strong polarization field within the AlGaN barrier and the screening effect of the 2-D electron gas (2-DEG) as well as the ionized surface states.

The two PF current components, denoted, respectively, as I_{PFS} and I_{PFD}, are obtained, following the same modeling approach as that of the TE current by considering two PF current sources: the gate-to-source PF current source and the gate-to-drain PF current source are obtained by integrating J_{PE} over the gate length and width, setting the applied gate voltage to, respectively, the intrinsic gate-to-source voltage $V_{G_iS_i}$ and the intrinsic gate-to-drain voltage $V_{G_iD_i}$, hence yielding the following relations for the vertical electric fields at the source and drain ends of the channel $E_{\perp,S}$ and $E_{\perp,D}$

$$E_{\perp,(S,D)} = [q\sigma_p - C_g(V_{G_i(S_i0,D_i0)} - \psi_{(S_i,D_i)})]/\epsilon \quad (18)$$

where $V_{G_iS_i0} = V_{G_iS_i} - V_{\mathrm{OFF}}$ and $V_{G_iD_i0} = V_{D_iS_i} - V_{\mathrm{OFF}}$. The source- and drain-side surface potentials ψ_{S_i} and ψ_{D_i} are obtained directly from the ASM-GaN compact model. The surface potential ψ_{D_i} is calculated using the same formulation as that of ψ_{S_i}, with the $V_{G_iD_i}$ in place of $V_{G_iS_i}$, which is needed to calculate ψ_{S_i}. The two PF current components I_{PFD} and I_{PFS} are then given by

$$I_{\mathrm{PF}(S,D)} = \frac{1}{2}\mathrm{NF}WLE_{\perp,(S,D)}C_{\mathrm{PF}}\exp\left(-\frac{\phi_{\mathrm{PF}(S,D)}}{V_{\mathrm{th}}}\right) \quad (19)$$

where

$$\phi_{\mathrm{PF}(S,D)} = \phi_{\mathrm{PF0}} - \sqrt{qE_{\perp,(S,D)}/(\pi\tilde{\epsilon})}. \quad (20)$$

To account for the simplifications encountered in the above-mentioned calculations, we introduce the following enhancements in the model. First, the gate-to-source voltage $V_{G_iS_i}$ and the gate-to-drain voltage $V_{G_iD_i}$ used in the calculation of the vertical electric fields $E_{\perp,(S,D)}$, given by (18), are replaced with the effective voltages given by (6) and (8), and the surface potentials ψ_{S_i} and ψ_{D_i} are replaced with the effective surface potentials given by

$$\psi_{S_i,\mathrm{eff}} = \beta_S\psi_{S_i} + (1-\beta_S)\psi_{D_i} \quad (21)$$
$$\psi_{D_i,\mathrm{eff}} = \beta_D\psi_{S_i} + (1-\beta_D)\psi_{D_i} \quad (22)$$

where the model parameter $0 \leq \beta_S \leq 1$ and $0 \leq \beta_D \leq 1$ are the same ones used in (6) and (8). Second, following the same enhancement in the Schottky barrier height implemented in the TE model, here also, we modify the source and drain barrier heights for electron emission from the trap states to the continuum of states as

$$\phi_{\mathrm{PFS0}} = \phi_{\mathrm{PF0}} \quad (23)$$
$$\phi_{\mathrm{PFD0}} = \phi_{\mathrm{PF0}} + \Delta\phi \quad (24)$$

where $\Delta\phi$ is the same OFF set potential used in (10). Third, the work-function difference V_{OFF} used in (17) is slightly altered as

$$\widetilde{V}_{\mathrm{OFF}} = V_{\mathrm{OFF}} + \Delta V_{\mathrm{OFF}} \quad (25)$$

where ΔV_{OFF} is a model parameter.

Our analysis of the measured characteristics of the devices under test shows that accurate modeling of these characteristics requires inclusion of temperature dependence for the barrier height ϕ_{PF0} as

$$\phi_{\mathrm{PF0},T} = \phi_{\mathrm{PF0}} + K_{\phi_{\mathrm{PF}}}(T/T_n - 1) \quad (26)$$

where $K_{\phi_{\mathrm{PF}}}$ is a model parameter.

Equation (18) yields nonzero vertical electric fields at zero biasing condition, i.e., at $V_{\mathrm{GS}} = V_{\mathrm{DS}} = 0$ V. Consequently, (19) yields nonzero PF current at zero biasing condition. Unless there exists a balancing conduction mechanism, the above-mentioned formulation results in a nonphysical situation at zero biasing condition. In [2] and [4], a trap-assisted tunneling mechanism has been considered as the balancing mechanism, which balances out the PF current at zero biasing condition. One can alternatively attribute this nonphysical behavior to the "phenomenological" modeling of the combined effect of dislocations in the AlGaN layer as a continuum of conductive states. Irrespective of the origin of this nonphysical behavior, we shall consider the following recalculation of the two components of the PF current to overcome this problem from the perspective of compact modeling

$$I_{\mathrm{PF}(S,D)} \rightarrow \xi_{(S,D)}(I_{\mathrm{PF}(S,D)} - I_{\mathrm{PF}(S0,D0)}) \quad (27)$$

where I_{PFS0} and I_{PFS0} are the gate-to-source and gate-to-drain PF currents calculated at zero biasing condition, and ξ_S and ξ_D are given by

$$\xi_{(S,D)} = \exp[\min(V_{G_i(S_i,D_i)}, 0)/V_{\mathrm{th}}] - 1 \quad (28)$$

where $\min(V_{G_i(S_i,D_i)}, 0)$ refers to taking the minimum of $V_{G_i(S_i,D_i)}$ and 0 V. Subtraction of $I_{\mathrm{PF}(S0,D0)}$ ensures zero PF current at zero biasing condition, at all temperatures, and multiplication by $\xi_{(S,D)}$ ensures zero first and higher derivatives of the PF with respect to V_{GS} and V_{GD} at zero biasing condition, at all temperatures.

C. FN Model

As the gate voltage becomes more negative, the electric field across the AlGaN barrier increases. At a critical electric field E_c, when the barrier width at the metal Fermi level becomes $<d_c$, the electrons at the metal Fermi level tunnel through the AlGaN barrier, as shown in Fig. 6, yielding an additional component for the gate current, namely, the FN current. The J_{FN}–E dependence of FN tunneling is given by [18]

$$J_{\mathrm{FN}} = q\mu n_{\mathrm{FN}}E_{\perp} \quad (29)$$

where q is the electron charge, μ is the electron drift mobility in the AlGaN layer, $E_{\perp}$ is the vertical electric field in the AlGaN layer, and n_{PF} is the electron density resulting from the FN mechanism and is given by

$$n_{\mathrm{FN}} = D\Delta E_{\perp}\exp(-B/\Delta E_{\perp}) \quad (30)$$

where D is a constant

$$\Delta E_{\perp} = E_{\perp} - E_c \quad (31)$$
$$B = 8\pi\sqrt{2m^*(\phi_{\mathrm{FN}})^3}/(3qh) \quad (32)$$

where m^* is the electronic effective mass in the AlGaN barrier, h is Planck's constant, and ϕ_{FN} is the effective barrier height and can be estimated using the relation

$$E_c \approx \phi_{\mathrm{FN}}/d_c \tag{33}$$

where the critical barrier width d_c is the barrier width at which the FN process initiates and is a few nanometers. Combining (29) and (30)

$$J_{\mathrm{FN}} = E_{\perp} C_{\mathrm{FN}} \Delta E_{\perp} \exp\left(-B/\Delta E_{\perp}\right) \tag{34}$$

where $C_{\mathrm{FN}} = q\mu D$ is a model parameter.

Following the same modeling approach as that of the TE and PF currents, we consider two FN current sources: the gate-to-source FN current source and the gate-to-drain FN current source. These two current components, denoted, respectively, as I_{FNS} and I_{FND}, are obtained by integrating J_{FN} over the gate length and width, setting the applied gate voltage to, respectively, the intrinsic gate-to-source voltage $V_{G_i S_i}$ and the intrinsic gate-to-drain voltage $V_{G_i D_i}$, yielding the following relations for I_{FNS} and I_{FND}:

$$I_{\mathrm{FN}(S,D)} = \frac{1}{2}\mathrm{NF}WLE_{\perp,(S,D)} \times C_{\mathrm{FN}} \Delta E_{\perp,(S,D)} \exp\left(\frac{-B}{\Delta E_{\perp,(S,D)}}\right). \tag{35}$$

The vertical electric fields $E_{\perp,(S,D)}$ are calculated in the same way as for the calculation of the two components of the PF current. Following the same enhancement implemented in the potential barrier heights used in the TE and PF models, here also, we modify the effective barrier height ϕ_{FN} as

$$\phi_{\mathrm{FNS}} = \phi_{\mathrm{FN}} \tag{36}$$

$$\phi_{\mathrm{FND}} = \phi_{\mathrm{FN}} + \Delta\phi. \tag{37}$$

Our analysis of the measured characteristics of the devices under test shows that accurate modeling of these characteristics requires inclusion of temperature dependence for the effective barrier height ϕ_{FN} as, in agreement with the results reported in the literature [16]

$$\phi_{\mathrm{FN},T} = \phi_{\mathrm{FN}} + K_{\phi_{\mathrm{FN}}}(T/T_n - 1) \tag{38}$$

where $K_{\phi_{\mathrm{FN}}}$ is a model parameter. Note that with this relation, the critical electric field E_c, given by (33), also becomes temperature-dependent.

In order to ensure zero FN current and zero first and higher derivatives of the FN current with respect to V_{GS} and V_{GD} at zero biasing condition, at all temperatures, we recalculate the two FN components, in a similar manner as we did for the two components of the PF current, as

$$I_{\mathrm{FN}(S,D)} \rightarrow \xi_{(S,D)}\left(I_{\mathrm{FN}(S,D)} - I_{\mathrm{FN}(S0,D0)}\right) \tag{39}$$

where I_{FNS0} and I_{FNS0} are the gate-to-source and gate-to-drain PF currents calculated at zero biasing condition, and ξ_S and ξ_D are given by (28).

TABLE I
TE MODEL PARAMETERS

	Description	Value
A^*	Effective Richardson's constant (A cm^{-2} K^{-2})	26.4
ϕ_{TE}	Schottky barrier height at 25 °C (eV)	0.94
$K_{\phi TE}$	Temperature parameter for ϕ_{TE} (eV)	0.43
$\Delta\phi$	Potential offset relating the source-side ϕ_{TE}, ϕ_{TES}, to the drain-side ϕ_{TE}, ϕ_{TED} (eV)	46e-3
η	Ideality factor for the TE current	1.41
K_η	Temperature parameter associated with η	-0.5
β_S	Weighting factor used in the calculation of the effective gate-to-source potential	0.7
β_D	Weighting factor used in the calculation of the effective gate-to-drain potential	0

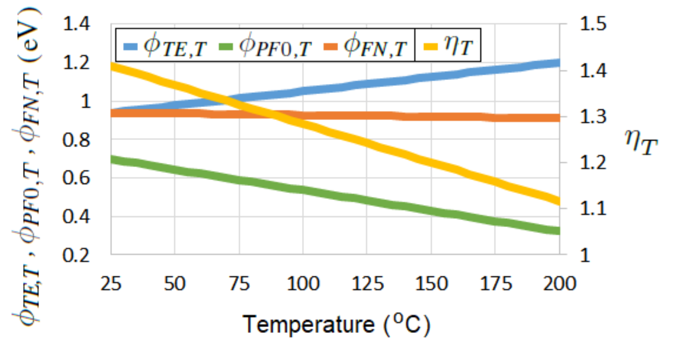

Fig. 7. Variations, with temperature, of the Schottky barrier height $\phi_{\mathrm{TE},T}$ and the ideality factor η_T used in the TE model, the barrier height for electron emission from the trap state to the continuum of states, $\phi_{\mathrm{PF0},T}$, used in the PF model, and the effective barrier height, $\phi_{\mathrm{FN},T}$, used in the FN model.

IV. SIMULATION RESULTS AND DISCUSSION

The extracted parameters for the TE current are tabulated in Table I. Using the theoretical value for the effective Richardson's constant (=26.4 A cm^{-2} K^{-2}, corresponding to an electronic effective mass of $0.22m_0$, where m_0 is the electron mass), the extracted value for the Schottky barrier height at T = 25 °C, ϕ_{TE}, is 0.94 eV, which is close to the values reported in the literature [1], [4], [20], [21]. As shown in Fig. 7, $\phi_{\mathrm{TE},T}$, given by (11), increases with increase in temperature, from 0.94 eV at T = 25 °C to 1.19 eV at T = 200 °C, hence shows a 27.7% increase in its value over this temperature range. On the contrary, the ideality factor η_T, given by (12), shows, as also shown in Fig. 7, a 20.9% decrease in its value over the same temperature range. These trends have already been reported in the literature [17], [19]. The excellent fit of the proposed model to the measured gate current under forward-bias condition is shown in Figs. 2(a) and 3.

As can be noted from Table I, the extracted values for the parameters $0 \leq \beta_S, \beta_D \leq 1$ in (6) and (8), used in the model for the TE current, are 0.7 and 0, respectively, which ideally are 1 and 0, respectively. In order to show the effect of the parameter β_S, which deviates from the ideal value, we simulated the model for the device with gate length $L = 5\,\mu$m at V_{DS} = 0.5 V, at T = 25 °C, setting this parameter to 0 and 1. The results are shown in Fig. 8.

The extracted parameters used in the calculation of the vertical electric field in the AlGaN barrier are tabulated

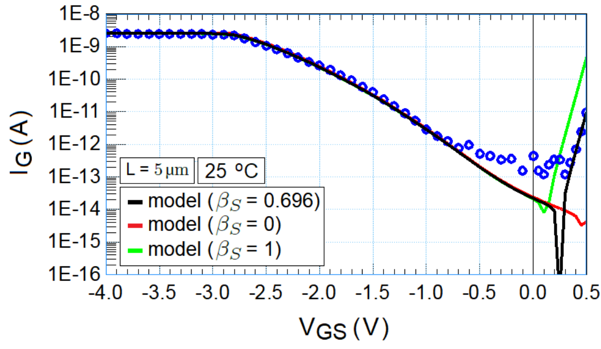

Fig. 8. Measured (symbol) and simulated (line) gate current (I_G)–gate–source voltage (V_{GS}) characteristics in the semilogarithmic scale for the device with gate length $L = 5$ μm at the drain-to-source voltage $V_{DS} =$ 0.5 V, at ambient temperature $T = 25°$C. Simulation results are shown when the parameter β_S in (6) is set to 0 and 1.

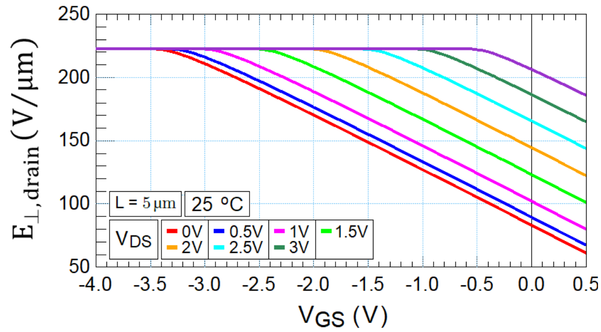

Fig. 9. Variation of the simulated vertical electric field at the drain side of the channel $E_{\perp,D}$ with the gate-to-source voltage V_{GS} at the ambient temperature $T = 25°$C, at the drain-to-source voltages V_{DS} ranging from 0 to 3 V.

TABLE II
PARAMETERS USED IN THE CALCULATION OF THE VERTICAL ELECTRIC FIELD IN THE AlGaN BARRIER

	Description	Value
σ_p	Polarization charge density (cm^{-2})	2.33e13
ΔV_{OFF}	Correction parameter for V_{OFF} used in the calculation in the surface potential (V)	-0.21

in Table II. The extracted value for the polarization charge σ_p is 2.33×10^{13} cm^{-2}, which is in the same range of values reported in the literature [1], [4], [17]. From (18), σ_p enters in the calculation of the vertical electric fields at the source and drain sides of the channel $E_{\perp,(S,D)}$. Fig. 9 shows the variation in the simulated $E_{\perp,D}$ with V_{GS} at 25 °C at various drain-to-source voltages.

The extracted parameters for the PF current are tabulated in Table III. The extracted value for the zero-electric-field barrier height for electron emission from the trap state to the continuum of states, ϕ_{PF0}, at temperature $T = 25$ °C is 0.7 eV, which is in the range in the same range of values reported in the literature [16]. Assuming the trap state to be very close to the metal Fermi level, the continuum of states is at a height equal to $\phi_{\mathrm{PF0}} = 0.7$ eV at $T = 25$ °C from the metal Fermi level. Fig. 7 shows the variation of $\phi_{\mathrm{PF0},T}$, given by (26), with

TABLE III
PF MODEL PARAMETERS

	Description	Value
ϕ_{PF0}	Zero-electric-field barrier height for the electron emission from the trap states to the continuum of states at 25 °C (eV)	0.7
$K_{\phi_{PF}}$	Temperature parameter associated with ϕ_{PF} (eV)	-0.64
C_{PF}	The constant in the equation of J_{PF} (A V^{-1}m^{-1})	19.9e-15
κ	Parameter relating the high-frequency and DC dielectric permitivity of the AlGaN barrier	0.3

TABLE IV
FN MODEL PARAMETERS

	Description	Value
ϕ_{FN}	Effective barrier height (eV)	0.94
$K_{\phi_{FN}}$	Temperature parameter associated with ϕ_{FN} (eV)	-48.3e-3
C_{FN}	The constant in the equation of J_{FN} (A V^{-2})	11.7e-9
d_c	Critical barrier width (m)	8.5e-9

temperature. As can be noted, $\phi_{\mathrm{PF0},T}$ shows a 54% decrease in its value over the temperature range from 25 °C to 200 °C.

The extracted parameters for the FN current are tabulated in Table IV. To fit the model to the measured data, we set the effective barrier height used in the FN model equal to the Schottky barrier height, as these two barrier heights are expected to be in close match [16], yielding a critical barrier width of 8.5 nm. This critical electric barrier width corresponds, using (38), to a critical electric field of $E_c =$ 110.6 MV/cm at $T = 25$ °C. The variation of $\phi_{\mathrm{FN},T}$, given by (38), with temperature is shown in Fig. 7. As can be noted from Fig. 7, $\phi_{\mathrm{FN},T}$ shows a 3% decrease in its value over the temperature range from 25 °C to 200 °C.

The excellent fit of the proposed model to the measured gate current under forward- and reverse-bias conditions is shown in Figs. 2–5. Fig. 3 shows the scalability of the model with the gate length, further confirming that the two contributing mechanisms in gate leakage in the reverse-bias condition are the PF emission and FN tunneling mechanisms through the AlGaN barrier, as opposed to leakage current, which can also occur through the AlGaN surface along the source and drain access regions, as reported in [22]–[24], in which case the electric field depends on the potential differences between the gate and source/drain terminals and the lengths of the access regions. Fig. 4 shows that the model gives zero derivative of the gate current with respect to V_{GS} and V_{GD} at zero biasing condition at 25 °C (the model gives similar results at higher temperatures), and Fig. 5 shows the consistent modeling of the drain and gate currents. Note form Fig. 5 that both the gate and drain currents saturate at the same gate-to-source voltage, corresponding to the saturation of the vertical electric field in the AlGaN barrier, as shown in Fig. 9. Note further from Fig. 4 that at gate-to-source voltages less than the threshold voltage, i.e., $V_{\mathrm{GS}} < -3$ V, $I_D = I_G$, implying, as expected, that in the OFF-state, the gate leakage is the only contributor to the drain current.

In order to show the contribution of the FN current, we simulated the I_G–V_{GS} characteristic for the device with gate length $L = 5$ μm at $V_{\mathrm{DS}} = 0$ V, at various ambient temperatures,

ranging from $T = 25$ °C to 200 °C, disabling the FN current by setting the parameter C_{FN} in (35) to 0. The results are shown in Fig. 2(a). In order to show the contribution of the PF current, we then simulated the same I_G–V_{GS} characteristic, disabling, this time, both the FN and the PF currents by setting the parameter C_{FN} and the parameter C_{PF} in (19) to 0. The results are also shown in Fig. 2(a). Finally, we simulated the I_G–V_{GS} characteristic for the device with gate length $L = 5\ \mu$m at $V_{DS} = 1.5$ and 3 V, setting the parameter C_{FN} to 0. The results are shown in Fig. 2(b). Fig. 2(b) shows that the PF current becomes a main contributor to the gate current at high temperatures.

V. Conclusion

An accurate surface-potential-based model for the gate current has been presented. This model, which is developed within the framework of the industry-standard ASM-GaN compact model, accounts for the dominant mechanisms for the gate current, namely, the TE, PF emission, and FN tunneling. The model has been validated with the experimental data for different temperature conditions and gate and drain voltages and for a different device gate length. The extracted parameters of these conduction mechanisms are in good agreement with the reported values in the literature.

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