# InAs Channel Inset Effects on the DC, RF, and Noise Properties of InP pHEMTs

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***Abstract*— GaInAs/InAs composite channels in InP-based pHEMTs enable wideband and/or low-noise performances because of their superior carrier transport properties. To date, the influence of the InAs inset design details on transistor performance has not been parametrized in the literature. We present a systematic study of the effects of the InAs channel inset thickness on transistor characteristics and cutoff frequencies versus temperature, and on the noise performance at 300 K. The epitaxial layer structures considered here incorporate 2 to 5-nm InAs insets in a fixed total composite channel thickness. All layers exhibit excellent electron mobilities (from 40 200 to 54 800 cm$^2$/Vs at 77 K). Thicker InAs insets improve both the current gain cutoff frequency ($f_T$) and the maximum oscillation frequency ($f_{MAX}$). However, they also result in higher gate leakage currents and increased channel impact ionization. 50-nm gate length pHEMTs with a 5-nm InAs inset feature the highest simultaneous $f_T/f_{MAX} \geq 390/675$ (455/800) GHz at 300 (15) K for a low-noise bias but exhibit the poorest minimum noise figure $NF_{MIN}$. Whereas higher $f_T$ (and/or $f_{MAX}$) values have traditionally been associated with improved noise performances, this is no longer the case.**

***Index Terms*— Direct current (DC), GaInAs, InAs channel, InP high electron mobility transistors (HEMTs), noise figure, radio frequency (RF).**

## I. Introduction

InP-BASED high electron mobility transistors (HEMTs) offer outstanding channel transport properties for high-speed, high-gain, and low-noise applications. They enable essential circuit blocks, such as low-noise receivers in telecommunications, imaging, and spectroscopy applications [1]. They are considered the best option for low-noise amplifiers, where the key emphasis does not only lie on speed and gain but also noise performance at both room and cryogenic temperatures [2].

In the pursuit of higher device operating frequencies, the careful optimization of transistor size and the reduction of parasitics plays a key role [3]–[5], as does the improvement of transport properties in the 2-D electron gas. InAs insets in indium-rich GaInAs channels evolved toward larger conduction band offsets and better carrier confinement [6]. Combined refinements in low-parasitics process architectures and layer epitaxy enabled record transconductances and short-circuited current-gain cutoff frequencies ($f_T$) [7]–[9], as the two quantities are linked according to the following equation [10]:

$$f_T = \frac{g_m}{2\pi} \frac{1}{(C_{GS}+C_{GD})\left(1+\frac{R_S+R_D}{R_{DS}}\right)+g_m C_{GD}(R_S+R_D)} \quad (1)$$

$$NF_{MIN} = 10\log\left(1+2\pi \cdot K_f \cdot f \cdot C_{GS} \cdot \sqrt{\frac{R_G+R_S}{g_m}}\right). \quad (2)$$

With higher cutoff frequencies, one would also anticipate improved noise properties according to the classical Fukui equation (2) [11], where $K_f$ is an empirical fitting parameter qualitatively associated with the "quality of transport" in the HEMT channel [11], and the remaining variables have their usual meaning (see the equivalent circuit model in Fig. 5).

More recent works on HEMT noise performance associated lower noise figures with $f_{MAX}$ improvements [2], [12]. This article shows that, among other findings, HEMT technology reached a development stage where further improvements in both $f_T$ and $f_{MAX}$ can, in fact, lead to a *degradation* in noise performance.

In this article, we systematically characterize the effects of 2 to 5-nm InAs channel insets incorporated in a 9.5-nm composite channel (with a constant total channel thickness and otherwise identical layer design) on the room temperature and cryogenic direct current (DC)/radio frequency (RF) device characteristics, as well as on the 300-K noise performance. Impact ionization is found to increase noise at low frequencies by adding to gate leakage and at high frequencies by adding channel noise.

## II. Device Fabrication

The epitaxial layer structures used in this study were grown by molecular beam epitaxy (MBE) on 2-inch semi-insulating InP substrates. In order to perform meaningful comparisons, all four epitaxial structures were identical with the exception of the InAs inset thickness in the channel, as illustrated in Fig. 1. The total composite channel thickness (GaInAs + InAs) was kept constant at 9.5 nm in all cases. The top AlInAs barrier thickness (4 nm) and its silicon delta-doping with a 2-nm spacer were also identical for all samples. Table I shows

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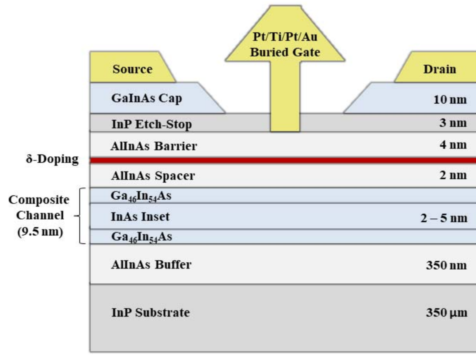


Fig. 1. Schematic cross section of the fabricated InP-HEMTs.

TABLE I
HALL MEASUREMENTS AT ROOM TEMPERATURE AND 77 K

| Temp. | Epitaxial Structure | $\mu$ (cm²/V·s) | $N_S$ (10¹² cm⁻²) | $R_S$ (Ω/□) |
|---|---|---|---|---|
| RT | 2nm InAs inset | 11,900 | 2.37 | 221.2 |
| | 3nm InAs inset | 13,500 | 2.63 | 175.3 |
| | 4nm InAs inset | 14,600 | 2.80 | 152.6 |
| | 5nm InAs inset | 15,100 | 2.87 | 143.9 |
| 77 K | 2nm InAs inset | 40,200 | 3.17 | 49.1 |
| | 3nm InAs inset | 49,600 | 3.25 | 38.8 |
| | 4nm InAs inset | 54,000 | 3.36 | 34.4 |
| | 5nm InAs inset | 54,800 | 3.36 | 33.9 |

Hall measurements (without cap layers) carried out at room and liquid nitrogen temperatures for the epitaxial structures detailed in Fig. 1.

the results of Van der Pauw measurements at room temperature and 77 K with the $n^+$ GaInAs cap removed. The increasing mobilities observed with thicker InAs inserts indicate high-quality epitaxial growths. The wider inserts lead to an apparent increase in modulation doping efficiency expressed by higher $N_S$ values.

The device fabrication process was identical and simultaneous for the four epitaxial layers considered here. Ohmic contacts were formed by an evaporated Ge/Au/Ni/Au metal stack with subsequent rapid thermal annealing. Device isolation by wet chemical etching followed. Next, a two-step electron beam gate lithography process was performed to define the gate. First, the gate foot region was defined in the first exposure of a single layer of polymethyl methacrylate (PMMA) followed by the selective removal of the $n^+$ GaInAs cap layer. The T-gate electrode was formed with two separate exposures of a multilayer photoresist stack to define the gate foot and head separately and deposition of a Pt/Ti/Pt/Au metal stack. The gates were sunk 8 nm through the InP etch-stop and into the AlInAs barrier at 250 °C as per [10] and passivated with a 15-nm $Al_2O_3$ layer by atomic layer deposition (ALD). Careful measurements using focused ion-beam (FIB) cross sections on all structures confirmed a 50-nm gate footprint, as shown in Fig. 2. Finally, a Ti/Au overlay metallization was e-beam evaporated to complete the device fabrication.

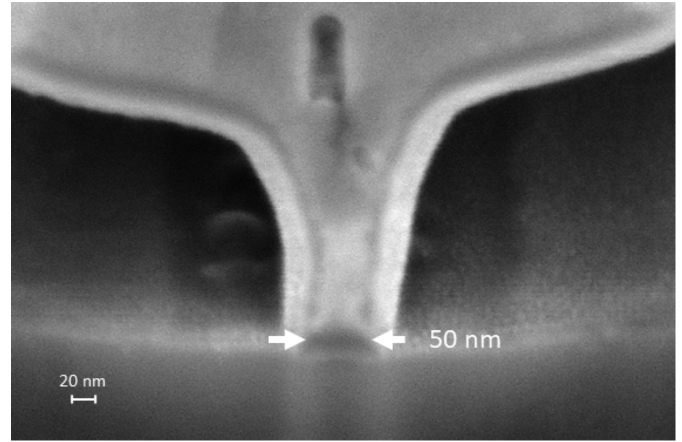


Fig. 2. Cross-sectional FIB image of the fabricated gates with a gate footprint $L_G$ of 50 nm.

## III. RESULTS

DC measurements were performed with an HP4156B semiconductor parameter analyzer for representative 2 × 50 $\mu$m pHEMTs with $L_G$ = 50 nm. As shown in Fig. 3, a thicker InAs channel insert improves the maximum DC output current $I_{DS}$ and the maximum DC transconductance $g_M$, but it also increases the gate leakage current $I_{GS}$ and shifts the threshold voltage $V_{th}$ negatively. The observed $V_{th}$ shifts are due to the carrier sheet density $N_S$ increases with the InAs inset thickness in the channel recorded in Table I.

RF measurements were carried out from 0.2 to 40 GHz with a PNA-X N5247A vector network analyzer using a line-reflect-reflect-match (LRRM) calibration and an off-wafer impedance standard substrate. In order to subtract pad parasitics from the measured S-parameters, on-wafer OPEN and SHORT pads with the same geometry as the device pad were used. Fig. 4(a) shows the extracted $f_T$ with the iterative de-embedding method [13] as a function of the drain current, $I_{DS}$, at drain bias voltages $V_{DS}$ of 0.5 and 0.75 V, for the four considered InAs channel insets. Following the same approach, the extracted $f_{MAX}$ for a $V_{DS}$ of 0.5 V is represented in Fig. 4(b). Additionally, the 5-nm InAs inset transistor microwave performance biased at $I_{DS}$ = 17.5 mA and $V_{DS}$ = 0.5 V is plotted in Fig. 4(c).

The gradual increase in $f_T$ with the InAs inset thickness in the channel was further studied by extracting small-signal equivalent circuit model (Fig. 5, [14], [15]) for each case, as presented in Table II. The extraction reveals that the $f_T$ improvement with thicker InAs inset is mainly attributed to an improved intrinsic small-signal transconductance $g_m$. Device capacitances vary little or decrease slightly with InAs inset thickness, providing a minor contribution to the rise in $f_T$ according to (1). Table II shows that under low-noise biasing conditions, the experimental $f_T$ and $f_{MAX}$ increase continuously with the InAs inset thickness—$f_T$ increases from 339 to 392 GHz (+15%) while $f_{MAX}$ rises from 411 to 678 GHz (+65%). Similar behaviors can be observed in the DC and RF measurements carried out at a cryogenic temperature, as shown in Figs. 6 and 7.

Additionally, the extracted small-signal equivalent circuit parameters at 15 K show the same trends as at room temperature. Fig. 8 shows the rise in both the intrinsic small-signal transconductance $g_m$ and the maximum DC transconductance $g_M$ for a thicker InAs inset thickness for room temperature, 77 and 15 K.

The improved $f_T$ and $f_{MAX}$ values and the reduced resistances would globally suggest improved noise figures with thicker InAs insets. However, the thicker InAs insets lead to a clear increase in gate leakage $I_{GS}$ during transistor operation

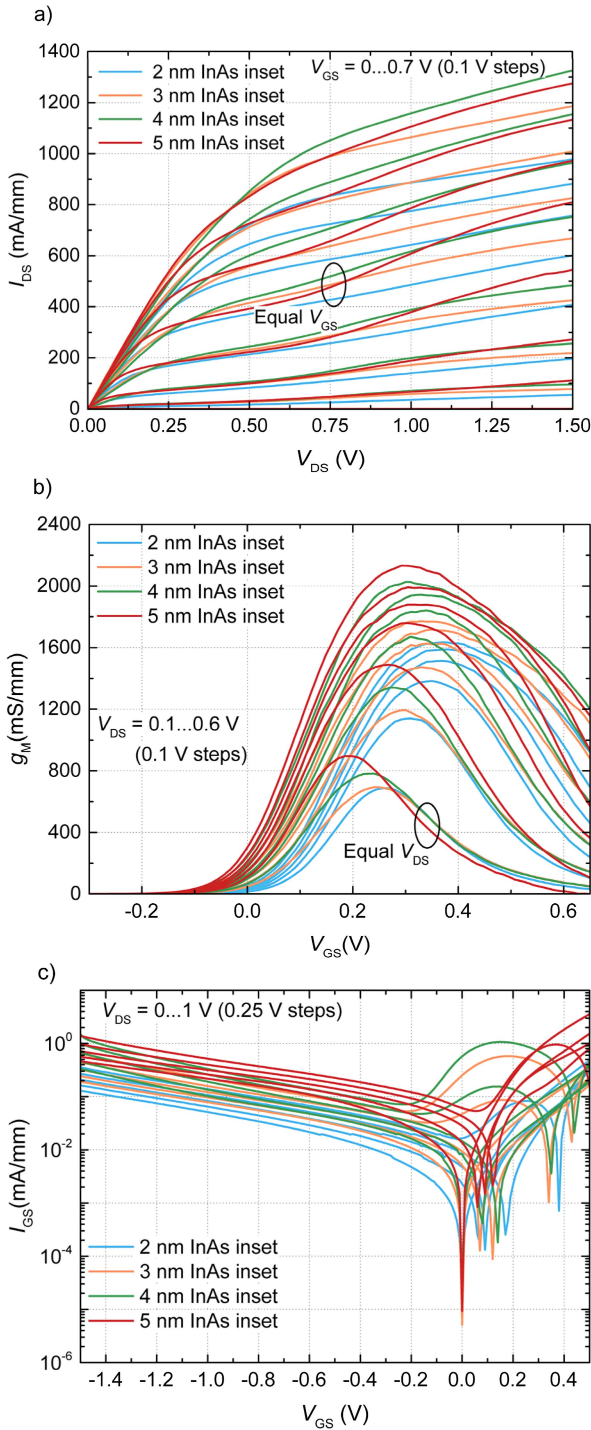


Fig. 3. (a) DC output, (b) transconductance, and (c) gate current characteristics of the fabricated 50-nm gate (2 × 25) $\mu$m devices measured at 300 K.

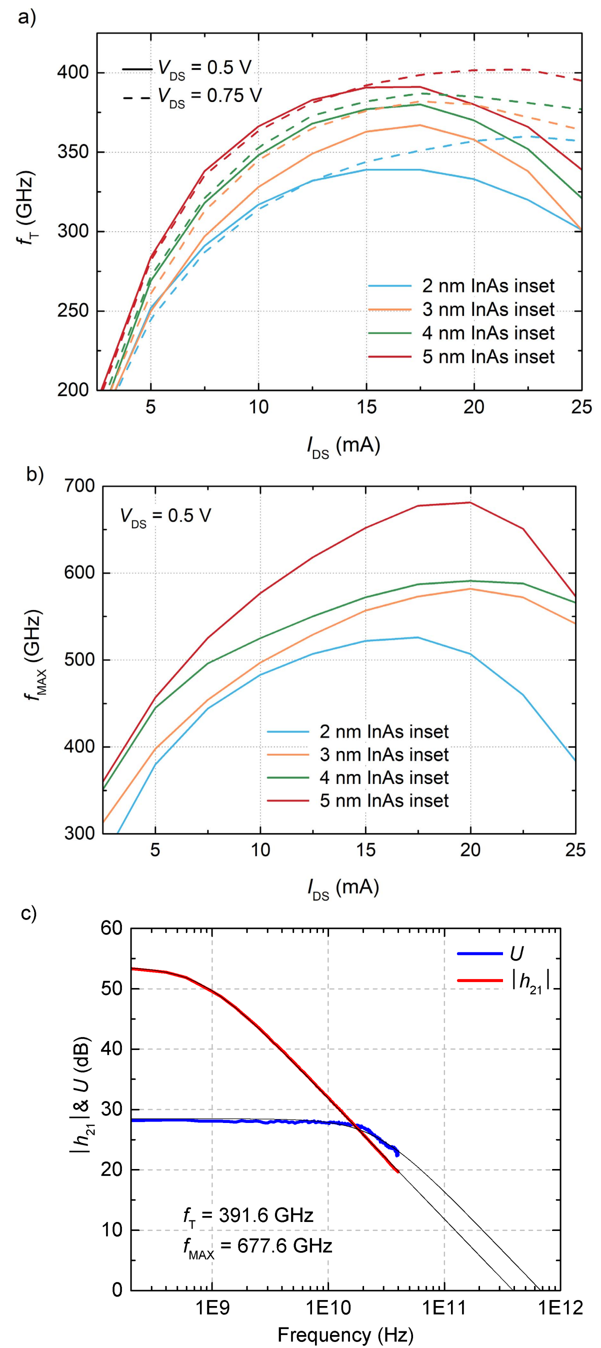


Fig. 4. (a) Short-circuit current gain cutoff frequency $f_T$ versus $I_{DS}$ at $V_{DS}$ = 0.5 V and $V_{DS}$ = 0.75 V for 50-nm gate (2 × 25) $\mu$m devices measured at 300 K. (b) Maximum oscillation frequency $f_{MAX}$ versus $I_{DS}$ at $V_{DS}$ = 0.5 V for same devices. (c) Representative deembedded extrapolation of $|h_{21}|^2$ and Mason's maximum unilateral gain $U$ for a 5-nm InAs inset device with equal geometry biased at $V_{DS}$ = 0.5 V and $I_{DS}$ = 17.5 mA.

(×6.9 rise between the 2 and 5-nm insets at $V_{DS}$ = 0.5 V and $I_{DS}$ = 17.5 mA, as shown in Table II).

The noise performance of our composite InAs/GaInAs channel HEMTs was characterized using the cold-source method [16]. The minimum noise figure $NF_{MIN}$ was measured from 8 to 40 GHz utilizing an HP 346C K01 noise source and an MT984AU impedance tuner from Maury Microwave. $NF_{MIN}$ degrades with increasing InAs inset thickness, as shown in Fig. 9, where only the limiting 2 and 5-nm inset cases are shown for clarity; the 2-nm InAs inset provides an $NF_{MIN}$ = 0.6 dB at 30 GHz while the 5-nm inset is significantly worse at 0.9 dB.

Results for the 3 and 4-nm insets are intermediate to the values shown in Fig. 9. Wider InAs insets show a higher noise at low frequencies, which is consistent with the observed higher gate leakage current levels. The $NF_{MIN}$ frequency

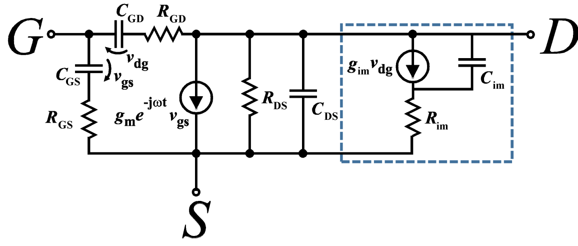


Fig. 5. Intrinsic small-signal equivalent circuit model [14] it including the model extension (boxed in blue) is used to capture the inductive behavior in $S_{22}$ in the presence of impact ionization and quantify impact ionization [15]. Extrinsic elements not shown.

TABLE II
EXTRACTED EXTRINSIC AND INTRINSIC SMALL-SIGNAL MODELING PARAMETERS AT 300 K

| | 2 nm InAs inset | 3 nm InAs inset | 4 nm InAs inset | 5 nm InAs inset |
|---|---|---|---|---|
| $R_G$ (Ω) | 0.89 | 0.89 | 0.89 | 0.89 |
| $R_D$ (Ω) | 1.01 | 0.89 | 0.99 | 0.92 |
| $R_S$ (Ω) | 1.04 | 0.91 | 0.80 | 1.01 |
| $C_{GD}$ (fF) | 11.4 | 11.1 | 11.9 | 11.8 |
| $C_{GS}$ (fF) | 29.0 | 28.6 | 26.1 | 27.9 |
| $C_{DS}$ (fF) | 10.1 | 9.9 | 9.3 | 9.4 |
| $R_{GS}$ (Ω) | 9.3 | 7.9 | 6.4 | 6.5 |
| $R_{DS}$ (Ω) | 95.7 | 93.8 | 86.9 | 91.3 |
| $R_{GD}$ (Ω) | 9.0 | 8.3 | 9.7 | 7.9 |
| $g_m$ (mS) | 81.5 | 88.5 | 94.9 | 102.1 |
| $f_{T,calc.}$ (GHz) | 300 | 333 | 370 | 379 |
| $f_{T,meas.}$ (GHz) | 339 | 367 | 380 | 392 |
| $f_{MAX}$ (GHz) | 411 | 473 | 532 | 678 |
| $I_{GSmeas}$ (μA) | 28.7 | 42.9 | 82.2 | 198.6 |

Example parameter extraction and $f_{T,calculated}$, $f_{T,measured}$, $f_{MAX}$ and $I_{GS}$ values of 50 nm gate (2 × 25) μm devices biased at $V_{DS}$ = 0.5 V and $I_{DS}$ = 17.5 mA.

dependence parametrized by $K_f$ in (2) also becomes progressively stronger with wider InAs insets: Table II shows that the 2 and 5-nm insets have the same gate and source resistances $R_G$ and $R_S$ and that the $NF_{MIN}$ frequency dependence is stronger in the 5-nm inset despite a significantly higher transconductance $g_m$, implying an increased $K_f$ with wider InAs insets. In the literature, $K_f$ is associated with the quality of transport in the channel—while the low-field mobility increases with InAs inset thickness (Table I), impact ionization levels also become stronger due to the decreasing effective channel energy gap. This can be seen from their stronger kink effect in the $I_{DS}$–$V_{DS}$ characteristics [Fig. 3(a)]. The increased bell-shaped gate leakage current characteristic [15] associated with impact ionization generated holes shown in Fig. 3(c) for $-0.2 < V_{GS} < 0.4$ V also becomes more dominant for wider InAs insets. Higher impact ionization levels in wider InAs insets also manifest themselves in microwave scattering parameter measurements as increasingly strong inductive features in the output reflection coefficient $S_{22}$ [15]. The measured S-parameters were fit to the ionization model of Reuter *et al.* [15] to quantify the extent of impact ionization as a function of bias for all the considered structures. The so-called impact ionization transconductance parameter $g_{im}$ quantifying the ionization increase in drain current is shown in Fig. 10 for $V_{DS} = 0.5$ and 0.75 V. It is striking that no impact ionization effects are visible in the 2-nm InAs inset below 25 mA at $V_{DS} = 0.75$ V (or for $V_{DS} = 1$ V at 5 mA).

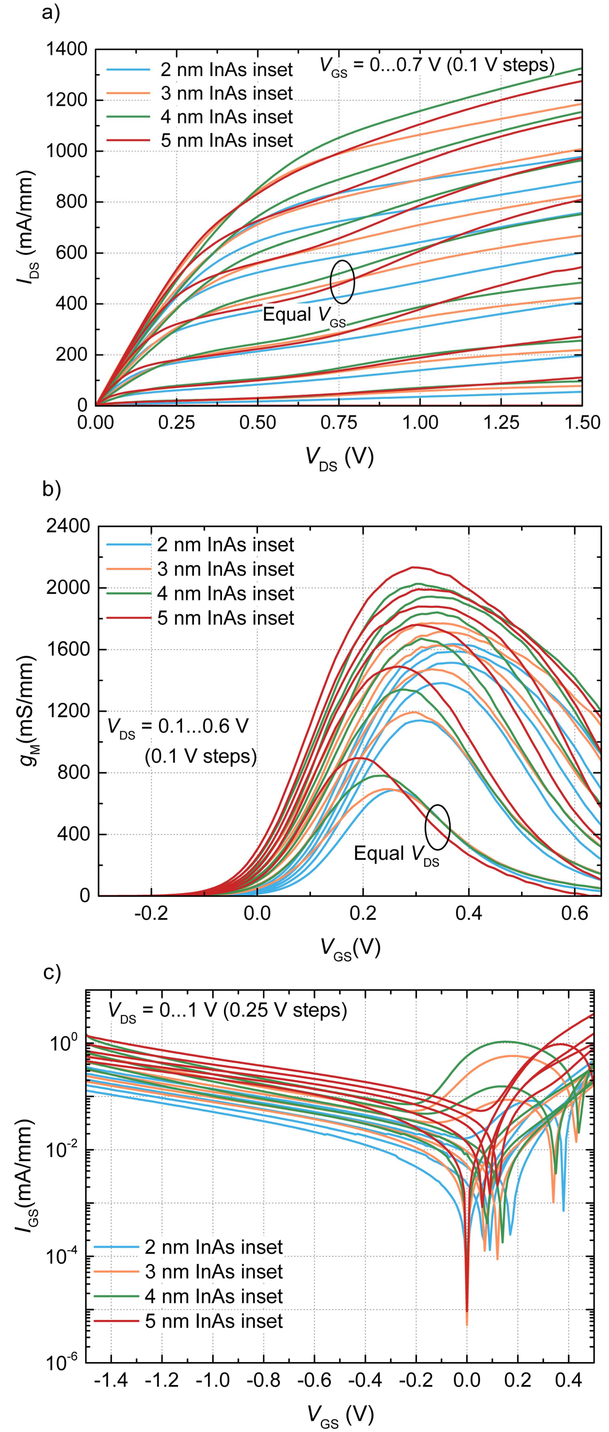


Fig. 6. (a) DC output, (b) transconductance, and (c) diode characteristics of the fabricated 50-nm gate (2 × 25) μm devices measured at 15 K.

Fig. 10 shows that impact ionization levels increase with $V_{DS}$ and InAs inset thickness.

Impact ionization induces channel noise because in carrier number and velocity fluctuations in the channel, we ascribe the high-frequency $NF_{MIN}$ degradation experienced with thicker InAs insets to their higher levels of impact ionization. The conclusion is supported by the Monte Carlo studies of Vasallo *et al.* [17] showing that impact ionization increases noise well into mm-wave frequencies.

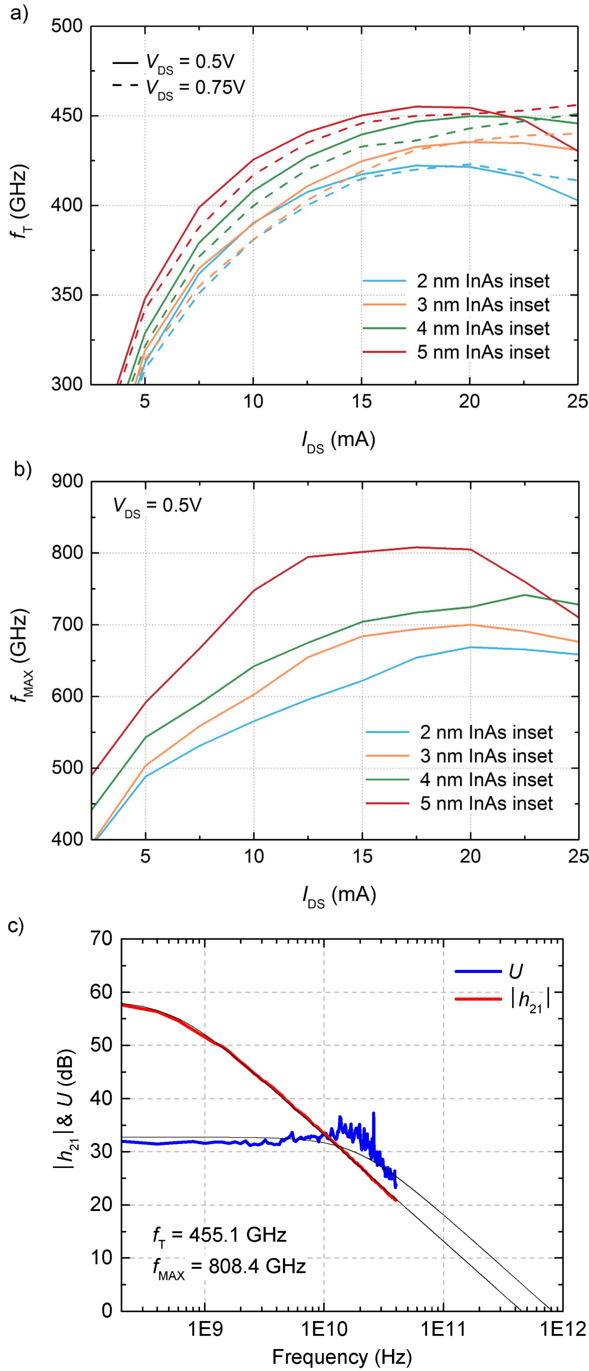


Fig. 7. (a) Short-circuit current gain cutoff frequency $f_T$ versus $I_{DS}$ at $V_{DS} = 0.5$ V for 50-nm gate (2 × 25) $\mu$m devices measured at 15 K. (b) Maximum oscillation frequency $f_{MAX}$ versus $I_{DS}$ at $V_{DS} = 0.5$ V for same devices. (c) Representative deembedded extrapolation of $|h_{21}|^2$ and Mason's maximum unilateral gain $U$ for a 5-nm InAs inset device with equal geometry biased at $V_{DS} = 0.5$ V and $I_{DS} = 17.5$ mA.

Fig. 11 compares $NF_{MIN}$ at $V_{DS} = 0.5$ and 1 V, and the same ordering in terms of InAs inset thickness is preserved, indicating that the inset properties carry on to higher voltages, albeit with notably increased noise levels. Higher $V_{DS}$ results in higher gate leakage current for the 2-nm inset $I_G = 13.7$ (0.5 V) and 61.8 $\mu$A (1 V), and for the 5-nm inset, $I_G = 167.8$ (0.5 V) and 237.1 $\mu$A (1 V), respectively. The implications are addressed in Section V.

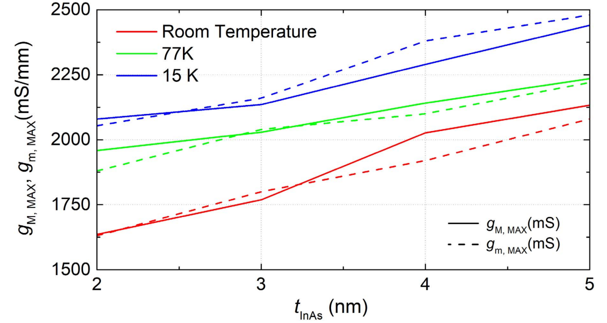


Fig. 8. Extracted intrinsic small-signal transconductance $g_m$ and maximum DC transconductance $g_M$ versus the InAs inset thickness at room temperature, 77 and 15 K.

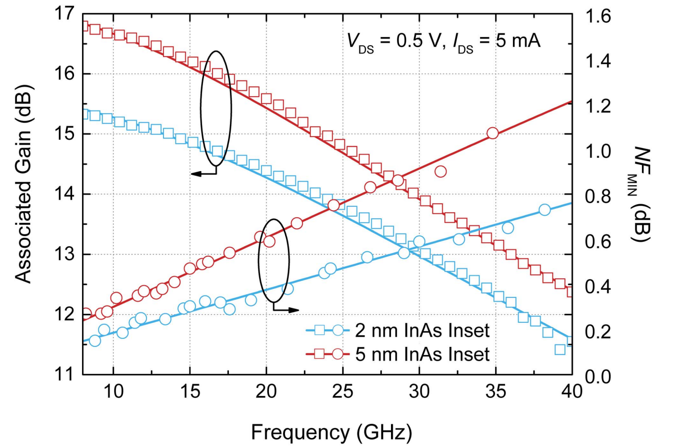


Fig. 9. Measured (symbols) and simulated minimum noise figure $NF_{MIN}$ and associated gain of 50 nm gate (2 × 25) $\mu$m HEMTs with 2 and 5-nm InAs insets biased at $V_{DS} = 0.5$ V and $I_{DS} = 5$ mA at 300 K. The 3- and 4-nm results lie between the 2 and 5-nm data (not shown for clarity). Effectively, thicker InAs insets increase the $NF_{MIN}$ slope factor $K_f$ from (2).

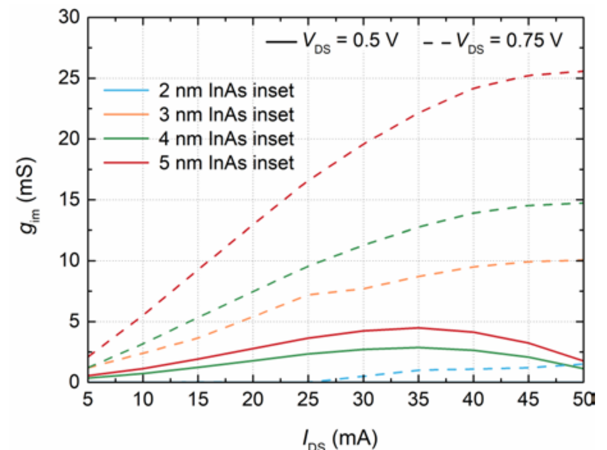


Fig. 10. Extracted impact ionization transconductance $g_{im}$ as per the model of Reuter *et al.* [15] for various InAs inset thicknesses. This parameter quantifies the drain current increase caused by impact ionization in the channel. Solid line: $V_{DS} = 0.5$ V. Dashed lines: $V_{DS} = 0.75$ V. The 2-nm inset channel is free of impact ionization at $V_{DS} = 0.5$ V.

## IV. Discussion

The increased gate diode leakage current with thicker InAs insets can partly be justified by examining carrier confinement

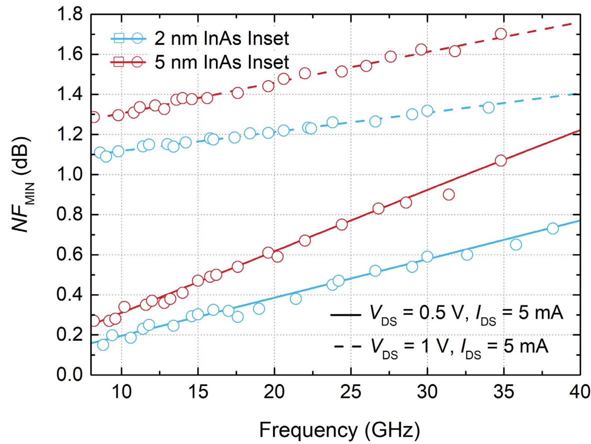


Fig. 11. Comparison of the minimum noise figure at $V_{DS} = 0.5$ and 1 V for a drain current $I_{DS} = 5$ mA. Symbols: measured data; lines: fit to the measured data. The $V_{DS} = 0.5$ V data is repeated from Fig. 9 for comparison. For the 2-nm inset: $I_G = 13.7$ (0.5 V) and 61.8 $\mu$A (1 V); and for the 5-nm inset: $I_G = 167.8$ (0.5 V) and 237.1 $\mu$A (1V), respectively. The 3 and 4-nm results lie between the 2- and 5-nm data (not shown for clarity).

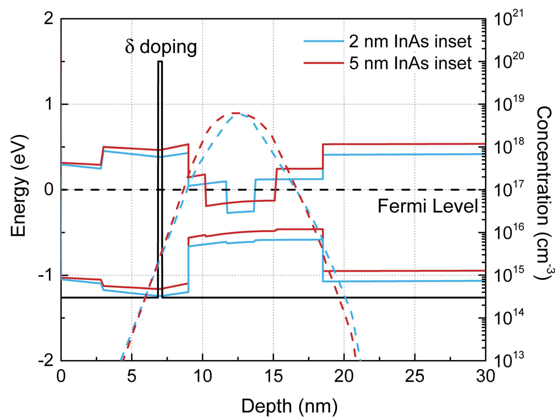


Fig. 12. Numerical simulations of the equilibrium band diagram and electron density in HEMT structure with 2- and 5-nm InAs insets in the GaInAs channel under the InP etch stop. Simulations performed in the Sentaurus TCAD environment.

in the channel. To illustrate this, Fig. 12 shows numerically simulated band diagrams of HEMTs structures with InAs inset thickness of 2 and 5 nm. The simulation shows a higher wave function amplitude in the top AlInAs barrier with a 5-nm InAs inset which likely accounts for a rise in the tunneling current between the gate and channel. Increased channel impact ionization at higher drain biases with thicker InAs insets also contributes additional gate current in transistor operation because the ionization-generated holes tend to flow to the negatively biased gate contact [15].

Apart from device operation-related mechanisms, such as tunneling and impact ionization, gate leakage may also increase in wider InAs insets because of epitaxial layer defects arising due to lattice-mismatched epitaxy. Such electronic defect states could offer leakage paths via intermediate states through the barrier material. Indirect evidence for such defects is visible by scanning electron microscopy (SEM) following device isolation by wet etching when pits were revealed on the etched mesa floor surface (Fig. 13). Such pits were observed on the mesa floor of all samples to various degrees.

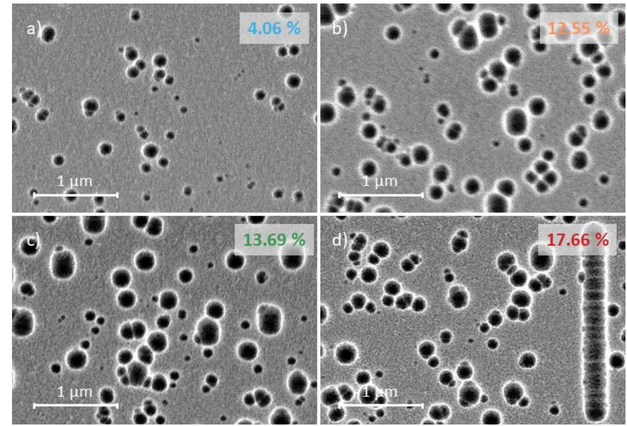


Fig. 13. SEM images of HEMT mesa floor surface with (a) 2 nm, (b) 3 nm, (c) 4 nm, and (d) 5 nm after device isolation with the calculated percentage of defects per unit area on the top right corner.

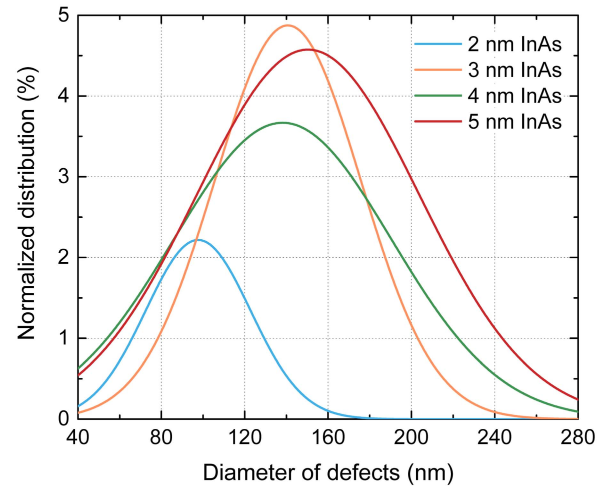


Fig. 14. Normalized distribution of mesa floor defects as a function of defect diameter for the four epitaxial layer structures considered in this article.

On the other hand, the gate recess InP etch stop surface remained pristine on all samples, indicating that the origin of the pits is not related to morphological growth defects propagating through the layers. As shown in Table I, thicker InAs insets consistently improve channel mobilities, but it appears they also lead to some enhanced localized etching patterns that transferred to the mesa floor surface during etching.

As Fig. 13 depicts, the diameter and surface areas occupied by the defects scale with the InAs inset thickness in the channel. The maximum diameter found for a defect with a 2-nm InAs inset substrate is 180 nm, whereas defects can reach a diameter of 330 nm with the 4 and 5-nm InAs insets. Likewise, the fractional area covered by defects from 4.1% for the 2-nm InAs inset to 17.8% for 5-nm InAs inset. Besides the rise in concentration and size, large defect clusters forming rod-shaped structures with lengths greater than 2 $\mu$m are also observed for the thickest InAs inset.

To correlate the defect density and extent with the InAs inset thickness, the number of defects was a fit to Gaussian distribution, as shown in Fig. 14. For the considered images,

the density of defects is increased for a thicker InAs inset, as well as raising the average diameter from 97 to 149 nm.

## V. Conclusion

We characterized the effects of different InAs inset thicknesses in GaInAs channel InP HEMTs with respect to DC, RF, and noise performances. Our work shows that increasing the InAs inset thickness is beneficial for DC and RF performances while it degrades the noise performance due to the combination of impact ionization and higher gate leakage current. An increase in the carrier density is experienced for thicker InAs insets, reaching remarkably high mobilities at both room and cryogenic temperatures as evidenced by Hall measurements. This leads to higher DC drain currents $I_{DS}$ and peak transconductances DC and RF transconductances $g_M$ and $g_m$, as well as improved cutoff frequencies $f_T$ and $f_{MAX}$.

The higher gate leakage currents with thicker InAs insets potentially arise from several mechanisms, including impact ionization in transistor operation, and wave function barrier penetration and even defects generated during the severely mismatched epitaxial growth of thicker InAs insets, which may affect gate diode leakage.

Because the noise performance of HEMTs is limited by gate leakage at low frequencies, and by channel noise at high frequencies [18], the impact ionization degrades the noise both at low and high frequencies; at low frequencies because of the increased gate leakage due to impact ionization generated holes [15], and at high frequencies because of the effect of number and velocity fluctuations on the spectral density of drain-current fluctuations calculated by Vasallo *et al.* [17].

In their analysis of the influence of gate leakage on the noise performance of HEMTs, Danneville *et al.* [19] showed that gate leakage increases $NF_{MIN}$ below a cutoff frequency $f_{sh}$ (which can be significant since proportional to both $f_T$ and increases with gate current as $I_G^{1/2}$—reaching $\sim 0.3 f_T$), thereby reducing the frequency dependence of $NF_{MIN}$ compared to a low gate leakage case [19]. Despite this, Fig. 11 clearly shows that at $V_{DS} = 0.5$ and 1 V, the higher leakage 5-nm InAs inset HEMT shows a stronger $NF_{MIN}$ frequency dependence than the lower leakage 2-nm inset HEMT, indicating stronger noise contributions at higher frequencies with the wider inset. We believe the present results provide the first experimental evidence of high-frequency impact ionization noise described by Vasallo *et al.* [17].

Although InAs channel insets effectively improve the channel mobility and high-frequency performance of InP pHEMTs, thicker InAs insets may not be suitable for low noise applications because they result in an increase in the $K_f$ slope factor in the Fukui equation (2). A key finding of this article is that InP pHEMT development has now reached a level of maturity beyond which increases in cutoff frequencies $f_T/f_{MAX}$ no longer guarantee improvements in noise performance. Achieving gain at higher frequencies in HEMTs requires shorter gate lengths, high mobility narrower gap channels, and thinner barriers—these factors contribute to higher impact ionization levels and gate leakage currents, thereby increasing $NF_{MIN}$ at both low and high frequencies.


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