Demonstration of UV-Induced Threshold Voltage Instabilities in Vertical GaN Nanowire Array-Based Transistors

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***Abstract*— This paper investigates the degradation of vertically aligned gallium nitride (GaN) nanowire (NW) arrays submitted to gate bias stress and UV light. Based on electrical tests and simulations, we demonstrate the existence of trapping processes that depend on the applied stress voltage $V_{Gstress}$ and on the applied light during stress (wavelength, λ). We demonstrate the following original results: 1) for positive and negative $V_{Gstress}$ conditions, no significant variation in dc characteristics is observed when the samples are stressed in dark and 2) when the devices are submitted to negative $V_{Gstress}$ and to UV light, a positive variation in threshold voltage (V_{th}) is observed. The positive V_{th} shift is ascribed to the transfer and trapping of electrons from the gate metal to the oxide, promoted by UV light. We also evaluated the temperature dependence of the threshold voltage shift under UV light. We demonstrated an increased trapping at higher temperatures, indicating a role of thermionic processes in electron trapping. On the other hand, detrapping from oxide states proceeds through defect-mediated conduction, i.e., is limited by the number of available states.**

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***Index Terms*— Gallium nitride (GaN), MOS, nanowire (NW) transistor, threshold voltage, UV illumination, vertical electronics.**

I. Introduction

THE wide bandgap and the high-electron mobility of gallium nitride (GaN) make this semiconductor very promising for high-voltage devices. The most widely used GaN transistor topology is the planar one that already demonstrated excellent performance for 650-V range applications. However, lateral transistors have limited current capability, and do not handle the high-power levels (<10 kW) and breakdown voltages (<1.2 kV) required for applications such as electric vehicles, photovoltaic inverters, and industrial motors [1].

In addition, the breakdown voltage of lateral devices scales with the gate–drain length (and device area/cost) and is limited by drain–substrate leakage. Finally, lateral high-electron mobility transistor (HEMT) may suffer from surface trapping effects [2]. In order to overcome these limitations, vertical GaN devices are currently investigated as the next generation of power devices.

Several vertical transistor structures have been proposed, including the current aperture vertical transistor (CAVET, [2]–[4]), in which the source region is separated from the drain region by an insulating layer with a narrow conducting aperture by using an Mg-ion-implanted GaN layer as a current blocking layer. Another interesting solution is the vertical GaN-based trench gate MOSFET, grown on a GaN substrate [5]. A blocking capability of 1.6 kV has been demonstrated based on this approach [6]. With the novel structure of multiple vertical GaN channel FETs operating in parallel, a current density of more than 4 kA/cm^2 with an ON-resistance of 0.84 m$\Omega\cdot$cm^2 has been demonstrated [7]. The stability of the threshold voltage under positive gate in GaN vertical transistors has been studied [8].

Among these approaches, vertically aligned GaN nanowires (NWs) have recently demonstrated to be a novel and promising approach to study for understanding the fundamental issues useful for applications in power electronics [9]–[12]. Similar devices have been also demonstrates by

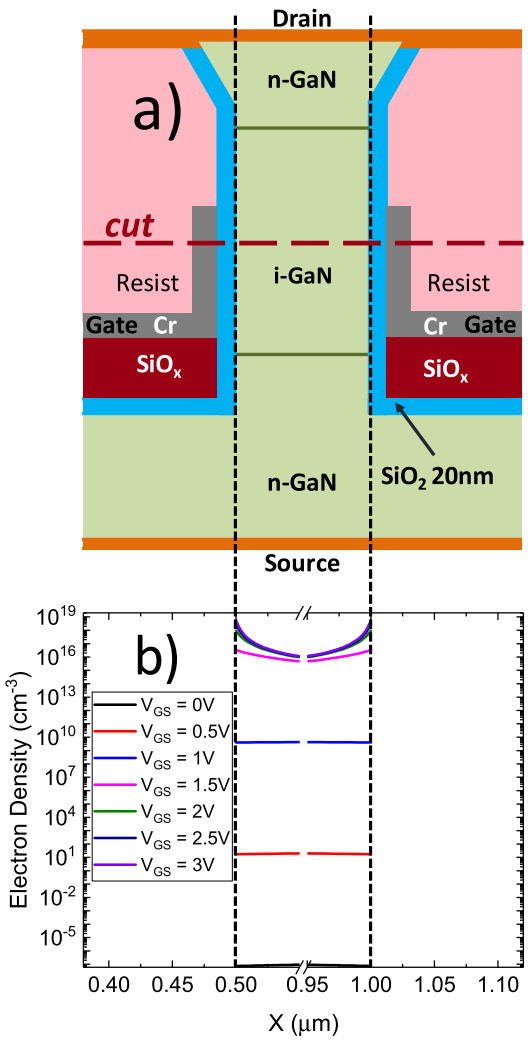

Fig. 1. (a) Pictorial view of the cross section of one GaN NW inside the transistor under test and (b) electron density simulation in the *i*-GaN channel (along the cut) under different gate biases: for $V_{GS} = 0$ V, the device is in OFF condition; hence, the electron density in the channel is very low (around 7×10^{-8} cm^{-3}), and the maximum is located in the center of the *i*-GaN region far from the interfaces. At low gate voltage ($V_{GS} = 1$ V), the e-density increases but it is still relatively low ($\leq 10^{10}$ cm^{-3}). At high gate voltages ($V_{GS} \geq 1.5$ V), the electron density shows a peak (5×10^{18} cm^{-3}) at the SiO_2/GaN interface.

other groups [13], [14]. They ensure E-mode operation and potentially scale down the device size compared to the lateral architecture. The 3-D approach can result in an effective use of device area and in a small vertical leakage. Moreover, the wrap-around gate can ensure a good electrostatic control of the channel.

The cross section of a single NW is reported in Fig. 1: for gate voltage higher than 1 V, current flows vertically through the low-doped n-GaN channel region, and it is collected at the drain contact. The Cr gate metallization is placed on a 20-nm SiO_2 layer, which is wrapped all around the NW.

Despite the potential of this new technology, very little is known about the dynamic performance and the stability of these devices. The aim of this paper is to present an extensive analysis of the stability of the threshold voltage of vertical NW FETs submitted to gate stress tests. This work also contributes to understand characteristics and problematics of vertical MOS structures, useful for implementing the novel approach for power applications. We demonstrate a trapping mechanism which is induced by the combined presence of gate voltage and UV light, and we propose a model to interpret the data. Specifically, when the device is submitted to a constant voltage bias (negative or positive) in dark conditions, no significant shift of the threshold voltage is observed. If we perform the same stress condition under UV light, we observe that a positive shift is induced for the negative gate bias. By investigating the impact of monochromatic light on gate leakage, we observe a significant increase of the current for $\lambda \leq 420$ nm, while longer wavelengths do not induce relevant effects. The combined effect of the negative $V_{Gstress}$ and the light exposure induces the transfer of electrons toward defects located in the gate dielectric; this causes a positive shift of the threshold voltage and the increase in the leakage current. The evaluation of the threshold voltage shift was performed at different temperatures by applying a gate voltage of 0 V and by exposing the device to UV light during stress. We observe that higher temperature can enhance the trapping of electrons in the insulator, due to a thermally assisted component. On the other hand, detrapping is not strongly thermally activated.

II. Device Description

The devices tested in this work are the enhancement mode GaN FETs composed of vertically aligned NWs with wrap-around gates. The GaN NWs have nonpolar *a*-plane sidewalls obtained by a top–down etching method. In Fig. 1(a), a cross-sectional schematic of one GaN NW is illustrated. The epitaxial layers were grown by metal–organic vapor phase epitaxy (MOVPE) on *c*-plane sapphire substrates. A 2.5-μ m-thick unintentionally doped GaN buffer layer was grown on the substrate; then, a 1-μm-thick Si-doped GaN with doping concentration of 10^{18} cm^{-3} was grown as a bottom source access layer. A 2-μm-thick unintentionally doped GaN was grown as the channel layer, and finally, a 0.5-μm-thick Si-doped GaN cap layer was grown for the top drain contact with a doping concentration of 10^{19} cm^{-3}. Vertically aligned NW arrays were fabricated in a top–down approach combining inductively coupled plasma reactive ion etching (ICP RIE) and KOH-based wet chemical etching. The sidewalls were conformally coated with 20-nm-thick SiO_2 as the dielectric layer by atomic layer deposition (ALD). A passivation layer (200-nm-thick SiO_x) was deposited between the n-GaN layer and the gate metal (200-nm-thick Cr). The NWs obtain a "mushroom" shape due to the anisotropic wet etching treatment [9]–[11] which prevents the accumulation of SiO_x on sidewalls during the deposition of the passivation layer.

The device is normally-OFF with a threshold voltage $\approx$1 V. For voltages below the threshold, the channel is depleted due to the work-function difference between the gate metal and GaN. At higher gate voltages, the drain current flows vertically from the drain to the source through the channel formed by the accumulation at the SiO_2/GaN interface. We use the Synopsys SDevice software to simulate numerically the electrical behavior of a single GaN NW device [15], represented by a 2-D cross section. Carrier transport is modeled

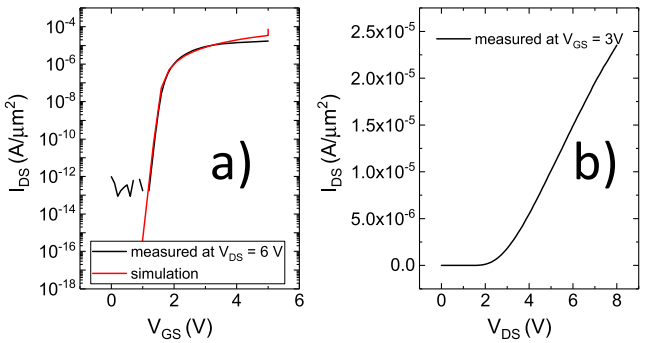

Fig. 2. (a) I_D–V_G plot of one measured device at $V_{DS} = 6$ V (black curve) compared with the simulated I_D–V_G (red curve). (b) I_D–V_D plot of one measured device. The number of NWs in the selected device is 289, and the total considered area is 56.644 μm^2.

with the standard drift–diffusion system. Shockley–Read–Hall (SRH) recombination adds recombination terms to the system. The carrier mobility is defined by a model, which takes into account the degradation due to impurity scattering and includes a material dependence. Drain and source contacts are ohmic, with a resistance of 0.001 Ω, gate contacts are Schottky with metal work function of 4.5 eV. In order to take into account the charge stored on traps in SiO_2, we inserted a fixed charge of -5×10^{17} uniformly distributed inside the oxide; simulation results were calibrated against experimental measurements. The simulation results in a self-consistent solution of Poisson equation, carrier continuity equation for electrons and holes. The simulation of the channel electron density in one NW for different gate voltages is reported in Fig. 1(b) [11]: below the threshold voltage ($V_{GS} = 0$ V), the electron density is negligible, the device is in the OFF-state and the channel is depleted. For low voltage ($V_{GS} = 1$ V), the electron density is still relatively low. For gate voltages higher than the threshold ($V_{GS} \geq 1.5$ V), the electron density peaks at the SiO_2/GaN interface (5.8×10^{18} cm^{-3}): the channel formed by accumulation is confined near the interface. The device tested in this study is composed of 289 NWs having a diameter (of the middle rod) of 500 nm. The total active area (56.644 μm^2) considered for the analysis is given by the sum of the areas of the active NWs. In Fig. 2(a), the plot of the measured drain current density versus gate voltage at $V_{DS} = 6$ V is reported (black curve), and in Fig. 2(b), the output characteristic is reported. The transfer curve is compared with the simulated I_D–V_G of one NW submitted to gate bias and with 6 V at the drain contact (red curve) [11]. The tested device shows a threshold voltage of 1.43 V. For the threshold voltage calculation, we extrapolate the value of the gate voltage at which the current reaches the value of at 10^{-9} A/μm^2 $= 10^{-1}$ A/cm^2.

III. Experimental Details

In Fig. 3, the schematic representation of the experimental setup is reported. The device under test is submitted for 100–1000 s to a constant gate voltage stress with the drain and the source terminal biased at 0 V under light or dark conditions. During the stress, fast I_D–V_G and I_D–V_D measurements are performed at defined steps in dark conditions. After the stress, a recovery phase in dark conditions is performed with gate–drain and source terminals at 0 V for 1000 s. Also, during the recovery, the changes in the dc characteristics are monitored by carrying out fast I_D–V_G and I_D–V_D measurements.

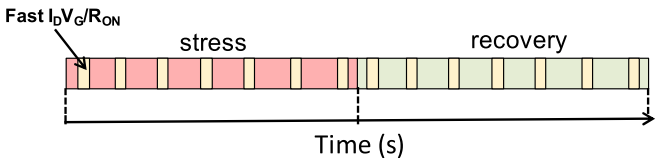

Fig. 3. Schematic representation of the procedure used for this analysis: the device was kept in constant voltage stress under positive or negative gate voltage of stress ($V_D = V_S = 0$ V) for 1000 or 100 s, and then a recovery phase was performed with all the terminals grounded. During the stress and recovery phases, fast I_D–V_G and I_D–V_D measurements were performed at defined steps. During the stress (not during the measurements), the device was kept in dark or lightened with 365-nm LED light.

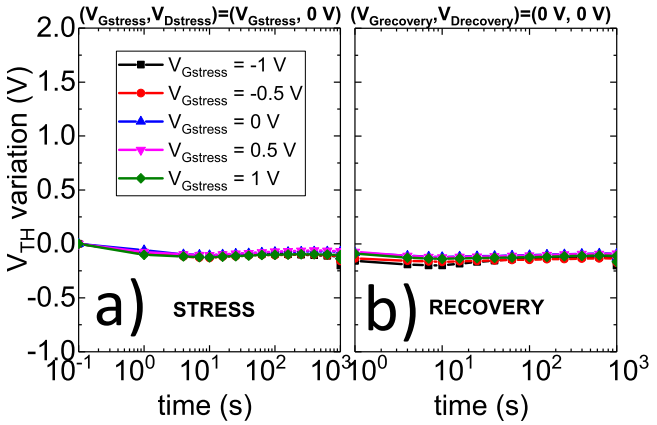

Fig. 4. Threshold voltage variation during (a) stress and (b) recovery phases. During the constant voltage stress test, the device was submitted to different gate voltages of stress ($V_D = V_S = 0$ V) for 1000 s in dark conditions; then, the recovery phase was performed with $V_G = V_D = V_S = 0$ V for 1000 s. No significant shift of the threshold voltage was observed.

IV. Results

A. Constant Voltage Stress and UV-Light Effect

In order to analyze the instabilities of the threshold voltage, we submitted the devices to a constant gate voltage in dark conditions for 1000 s at several voltages between −1 and 1 V. From the I_D–V_G measurements performed at defined steps during the stress, we obtained the threshold voltage variation during the stress and recovery phase. The applied positive and negative gate voltages induce negligible variation in the threshold voltage (Fig. 4); therefore, the devices are stable under dark conditions.

In order to further investigate the device performance, we tested the variation of the threshold voltage under light. During the 100-s constant voltage stress, the device was illuminated with a 365-nm LED source, the fast I_D–V_G/I_D–V_D was measured in dark conditions. The results of the stress test are shown in Fig. 5: exposure to light induces a positive shift of the threshold voltage for more negative gate voltages. Typically, a positive shift in the threshold voltage indicates trapping of electrons in the oxide. The fact that the V_{th} shift is observed only under light suggests the presence

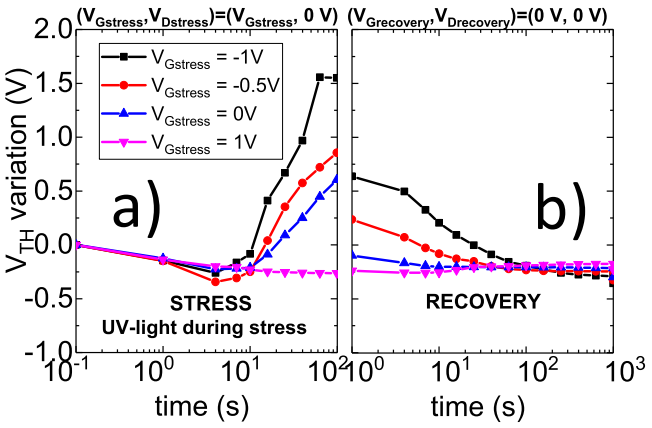

Fig. 5. Threshold voltage variation during (a) stress and (b) recovery phases. During the constant voltage stress test, the device was submitted to different gate voltages of stress ($V_D = V_S = 0$ V) for 100 s, and it was lightened with a UV-light LED (365-nm wavelength); then, the recovery phase was performed in dark with $V_G = V_D = V_S = 0$ V for 1000 s. The negative bias applied to the gate terminal, and the UV light induces a positive shift of the threshold voltage (fully recoverable).

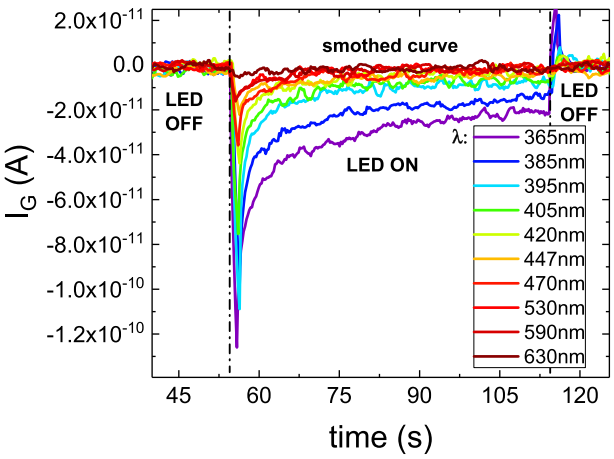

Fig. 6. Transient of the gate leakage current of the device under test when it was lightened with LED light at different wavelengths (λ) but the same intensity (W/cm^2). A significant increase in gate leakage (electrons injected toward insulator) was observed for $\lambda \leq 420$ nm.

of a barrier for electron injection/trapping. These aspects are discussed later in this paper. After the stress, also the recovery phase was characterized, with all terminals grounded and in dark conditions for 1000 s. The results (Fig. 5) indicate that the light-induced trapping process is fully recoverable. The UV-light exposure could lead to the creation of electron–hole pairs inside the GaN since the bandgap of GaN is equal to the UV-light energy. However, we can exclude the trapping of holes at the GaN/oxide interface and/or in the oxide, because in that case, we should see the effect in a negative shift of the threshold voltage [16]. The slight initial negative shift in the stress phase is possibly related to a photon-related detrapping process of negative charge in the oxide. We have discrepancies because between the stress and recovery phase few seconds pass without any bias applied due to limitations in the measurement system. We can conclude that during that period of time, the detrapping process already started and what we see at the beginning of the recovery phase is the threshold voltage of the device partially detrapped.

B. Wavelength Dependence

In order to analyze if the observed light-induced trapping process is wavelength-dependent, we evaluated the transients of the gate leakage current under monochromatic LED illumination. All LEDs were calibrated in order to generate the same light flux (mW/cm^2) for all wavelengths. A transient setup was developed and used for this aim. First, the devices are kept at 0 V with no applied light. Then, monochromatic light is shone on the samples for 60 s, and the gate leakage (at 0 V) is continuously monitored, to evaluate the light-induced current.

The plot of the gate current during time in the dark condition and under light is depicted in Fig. 6. First, we notice that even at 0 V, a significant current is measured when the light is shone on the sample. Such current is negative, i.e., entering the instrument. This is consistent with an electron current injected from the gate toward the oxide. From Fig. 6, we notice that the amount of increase induced by light changes with wavelength: a significant increase in gate leakage was observed for $\lambda \leq 420$ nm, while longer wavelengths did not induce a strong effect. Out of the tested values, UV light at 365 nm induces the maximum variation in the gate leakage current.

Our hypothesis is that the transients of the gate current are induced by the injection of electron toward the insulator: photons impinging on the metal/oxide interface can excite electrons on the Fermi level of the metal/oxide interface toward higher energy levels, either at the conduction band of the oxide or at shallow oxide traps. Then, electrons can proceed toward the GaN layer, thus being collected at the semiconductor side. This mechanism is enhanced by the light with wavelength below 420 nm, suggesting the existence of threshold energy equal to 2.95 eV. This threshold energy appears to be lower than the energy barrier from gate to the oxide: $q(\Phi_{Cr} - \chi_{SiO_2}) = 4.5 - 0.8$ eV $= 3.7$ eV, so that supposedly the energetic level of traps should be, at most, at 0.75 eV below the conduction band. Given the continuous increase in leakage with increasing photon energy, the conducting states are likely configured as a miniband of defects. A schematic representation of this process is shown in Fig. 7, indicating that light transfers energy to electrons at the metal/oxide interface; the combined effect of UV light and slight band bending can help electrons being injected to defect states in the dielectric layer. In the beginning, many trap states are available in the oxide and can be occupied quite quickly; this leads to a current spike, while with increasing time, the traps are filled more and more, leading to an exponentially decreasing current. When light is turned off, electrons remain temporarily trapped in the insulator. Fig. 6 shows that for a few seconds, a positive current is measured, suggesting that (at least a part of) the electrons in the insulator move back toward the gate metal (see below for a discussion on the recovery phase). The model shown in Fig. 7 is in good agreement with the results reported in Fig. 5(a): at more negative gate bias, the electric field in the oxide is higher, thus leading to an increase in the charge transfer rate.

C. Temperature Effect

In order to further analyze the mechanism, we tested the devices at different temperatures, by biasing the all

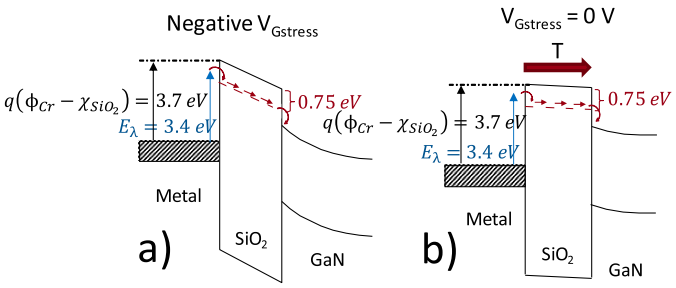

Fig. 7. (a) Schematic interpretation of the measurement results: the combined effect of the energy given from light related to the threshold wavelength of photocurrent measurements ($E_\lambda = 3.4$ eV) and the band bending (negative V_{Gstress}) helps electrons from gate metal to be trapped inside the oxide inducing the observed shift of the threshold voltage. (b) Pictorial view of the effect of the temperature in the trapping/detrapping mechanisms: 1) the temperature supports the trap-assisted tunneling, reducing the time of retention of electrons trapped in the insulator, and 2) detrapping from oxide states proceeds through defect-mediated conduction, i.e., is limited by the number of available states.

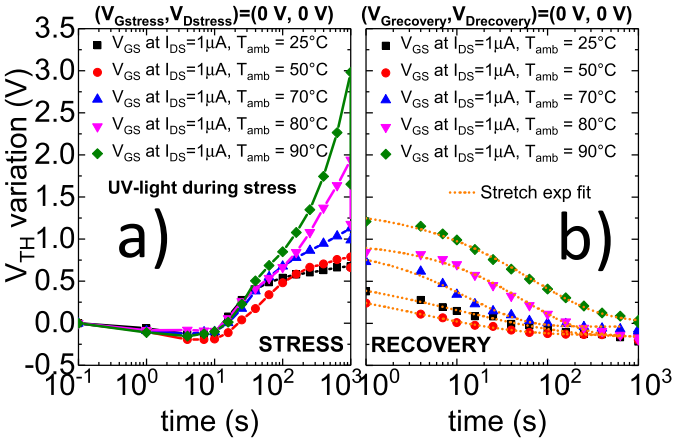

Fig. 8. Evaluation of the threshold voltage shift at different temperatures by applying a gate voltage of 0 V and by exposing the device to UV light during (a) stress and (b) recovery was performed in dark. The positive threshold voltage shift increases with the temperature. The recovery curves can be fit with stretched exponential fit demonstrating that the recovery is thermally activated.

the terminals at 0 V. The results are reported in Fig. 8: here, a sample was submitted to trapping and subsequent recovery under 0-V and 365-nm illumination. By increasing the temperature, an increased charge trapping was observed, as shown in Fig. 8(a). This can be explained by two concurring mechanisms: 1) by increasing the temperature, we increase the thermal energy of electrons injected toward the oxide, which can occupy states at higher energy levels and 2) temperature promotes conduction inside the oxide. This latter hypothesis is in good agreement with the trend of the threshold voltage variation during stress at different temperatures shown in Fig. 8(a). Up to 40 s, all the curves are overlapped: in this phase, the deep levels close to the metal are filled without significant temperature enhancement. At longer stress times, the additional states to be filled are far away from the interface; temperature promotes trap-assisted conduction (by a charge hopping or Poole–Frenkel mechanism), leading to an increased trapping rate for defects located deep in the oxide. Thus, if light excitation is the main origin of charge transfer to the insulator, the thermal effect may further enhance the process.

The results shown in Fig. 8(b) indicate that the V_{th} shift is fully recoverable, indicating a complete re-emission of the charge trapped in the insulator.

A reasonable possibility is that during the recovery phase, the trapped electrons move out of the oxide through hopping or Poole–Frenkel conduction. Under this assumption, electrons are transferred from one trap to another via a tunneling mechanism. Chiu *et al.* [17] reported that at low electric fields 0.6 MV/cm, the experimental J–E data match the simulated hopping conduction curves very well from 300 to 400 K, i.e., around room temperature. The hopping current can be derived by using the following equation:

$$J = qan\nu \exp\left(\frac{qaE}{kT} - \frac{E_a}{kT}\right) \tag{1}$$

where a is the mean hopping distance, n is the electron concentration in the conduction band of the dielectric, ν is the frequency of thermal vibration of electrons at trap sites, and E_a is the activation energy.

The instantaneous current is given by the derivative of the electric charge by time, i.e., by the variation of the electron concentration in the dielectric; with the constant electric field and temperature, we have

$$J(t) = \frac{dq(t)}{dt} = \frac{dn(t)}{dt} = qa\nu \exp\left(\frac{qaE}{kT} - \frac{E_a}{kT}\right) n(t). \tag{2}$$

The solutions of the differential equation (2) are

$$n(t) = c_1 e^{qa\nu \exp\left(\frac{qaE}{kT} - \frac{E_a}{kT}\right)t}. \tag{3}$$

This would imply that during the recovery phase, the variation of V_{th} would follow an exponential function; this is consistent with the fact that the recovery curves can be fit by a stretched exponential equation [see Fig. 8(b)], possibly due to a distribution of traps in the oxide [(1)].

In Fig. 7(b), a pictorial view of the mechanism activated during stress is reported: at 0 V, the bands of the structure are slightly bended ($V_{\text{Flatband}} \approx 1.22$ V), the electrons illuminated by the UV source can overcome the gate barrier and be injected from the metal layer toward trap states in the oxide. Here, they can be trapped in the oxide traps and slowly move to the semiconductor side. By increasing the temperature, a stronger injection may be possible, thanks to the higher electron energy [18]. The total effect, in these conditions, is an increase of the gate current for higher temperatures. The trap-to-trap conduction is supposed to be responsible also for the detrapping phase, whose kinetics can be fit by stretched exponential functions in agreement with (3).

V. Conclusion

In order to contribute to understand the vertical MOS structure required for the new generation of power devices, we carried out the first analysis of the stability of the threshold voltage in NW-vertical GaN FETs submitted to gate stress. We demonstrated the existence of a light-triggered trapping process, which favors the injection of electrons from the metal toward the oxide. Specifically, once the device has been submitted to a constant negative voltage stress combined with

UV light, the threshold voltage shifts toward more positive values due to the injection of electrons from the gate metal into the gate dielectric. The higher temperature supports the injection through the insulator even at null gate bias. At 0 V, the bands are slightly bended, and the electrons illuminated by the UV source can overcome the gate barrier and be injected in the oxide. Electrons can tunnel trap-to-trap inside the oxide; the detrapping (performed in dark condition) proceeds by defect-mediated conduction, whose kinetics are limited by the number of traps available.

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