Foreword
Special Issue on Compact Modeling for Circuit Design

THIS Special Issue is dedicated to recent research in the field of compact modeling for circuit design. The topics included all device structures, provided it was demonstrated that the presented compact modeling solutions were implementable in circuit design tools. The last Special Issue addressing compact modeling of all types of semiconductor devices was published in 2006. Since then, new device structures, and with different materials, have emerged, and significant and successful research in compact advance device modeling has been done, as well in the application of compact models to circuit design. Therefore, a new Special Issue was needed that could include high-quality papers in these topics.

A total of 60 regular papers were submitted to this Special Issue, of which 21 were accepted. Besides, the Special Issue includes four invited papers. All papers, including the invited ones, were subjected to thorough peer review. A high number of reviewers have participated in this process. This has resulted in a Special Issue containing very high-quality papers.

The published papers target compact modeling aspects for a wide number of devices: several MOSFET structures, tunnel FETs, HEMTs, nanowire FETs, TMD FETs, TFTs, OLEDs, solar cells, photodiodes, and so on.Besides, different operation regimes and analyses are addressed: dc, RF, HV, ballistic regime, variability, reliability, aging, and so on.

The four invited papers also target different topics. The paper by C. C. McAndrew is focused on the successes and challenges of MOS compact models. S. Dongaonkar *et al.* address the opportunities and challenges of circuit design methodologies ranging from process corners to statistical circuit design. P. Zampardi *et al.* discuss the industrial view of III–V device compact modeling for circuit design. Finally, Madec *et al.* target a quite different and challenging environment for the modeling of biosensors, biosystems, and lab-on-chips.

I would like to thank the work done by the rest of the Editors of this Special Issue and also by all the reviewers who participated in this process. And of course, I want to thank all the authors for their interest in submitting papers to this Special Issue. Thanks to authors, reviewers, and editors, this high-quality Special Issue has been possible.

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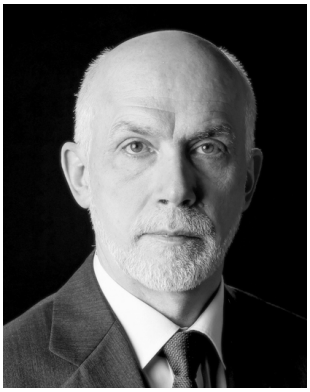
From 1997 to 1998, he was a Post-Doctoral Researcher with the Rensselaer Polytecnhnic Institute, Troy, NY, USA. From 1998 to 2001, he was a Post-Doctoral Scientist with the Université catholique de Louvain, Louvain-la-Neuve, Belgium. He has published over 150 research papers in international journals and over 140 papers in the proceedings of conferences. He has led one European Union funded project about compact modeling of nanoelectronic devices. He was supported by two Marie Curie Fellowships from the European Commission. He has participated as Team Leader with Universitat Rovira i Virgili (URV), Tarragona, Spain, in more than five European Union funded projects and in two research contracts with Silvaco., Inc. He is currently leading one project about compact modeling of thin-film transistors (TFTs). In 2001, he joined the Department of Electronic, Electrical and Automatic Control Engineering, URV, as a Titular Professor, where he became a Full Professor in 2010. His current research interests are compact modeling of advanced electron devices (in particular MOS structures, GaN HEMTs, and TFTs), parameter extraction techniques, and semiconductor device physics and electrical characterization.

Dr. Iñiguez was elected as an EDS BoG Member at-large in 2017. He has been a Distinguished Lecturer since 2004. He received the Distinction from the Generalitat for the Promotion in University Research in 2004 and the ICREA Academia Award from the ICREA Institute in Catalonia, Spain, in 2009 and 2014. He has been the Vice-Chair of EDS Region 8. Since 2017, he has been the Chair of the Compact Modeling Technical Committee of EDS. Since 2016, he has been an Associate Editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES.



Wladek Grabinski received the Ph.D. degree from the Institute of Electron Technology, Warsaw, Poland, in 1991.

From 1991 to 1998, he was a Research Assistant with the Integrated Systems Laboratory, ETH Zürich, Zürich, Switzerland, supporting the CMOS and BiCMOS technology developments by the electrical characterization of the processes and devices. From 1999 to 2000, he was with Electronics Laboratory, École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, where he was involved in compact MOSFET model developments supporting numerical device simulation and parameter extraction. Later, he was a Technical Staff Engineer at Motorola, Geneva, Switzerland, and subsequently at Freescale Semiconductor, Geneva Modeling Center, Geneva. He is currently a Consultant responsible for SPICE modeling, characterization, and parameter extraction of MOST devices for the analog/RF IC applications. He is also consulting on the development of next-generation compact models for the nanoscaled technology very large-scale integration circuit simulation. His current research interests include high-frequency characterization, compact modeling, and its Verilog-A standardization and device numerical simulations of MOSFETs for analog/RF low-power IC applications. He is an Editor of the reference modeling book *Transistor Level Modeling for Analog/RF IC Design* and also authored or co-authored more than 50 papers.

Dr. Wladek is a Member-At-Large of Swiss IEEE ExCom and also supports the EPFL IEEE Student Branch acting as its Interim Branch Mentor. He is involved in the activities of the MOS-AK Association and has been serving as a Coordinating Manager since 1999. He is the Chair of the ESSDERC Track4: Device and Circuit Compact Modeling and has served as a member of the Organization Committee of ESSDERC/ESSDERC and the Technical Programme Committee of Symposium on Microelectronics Technology and DEvices, Simulation of Semiconductor Processes and Devices, and Mixed Design of Integrated Circuits and Systems Conferences. He has served as a Reviewer of the IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS, *International Journal of Numerical Modeling*, *Microelectronic Engineering*, and *Microelectronics Journal*.

Slobodan Mijalković (SM'01) received the Engineering, Magister, and Ph.D. degrees from the Faculty of Electronics Engineering, University of Niš, Yugoslavia, Serbia, in 1982, 1989, and 1991, respectively. His Magister and Ph.D. research was focused on a development of efficient meshing and solver techniques for application in TCAD process simulation tools.

He was appointed as a Teaching Assistant at the Faculty of Electronics Engineering, University of Niš from 1983 to 1991. From 1991 to 1998, he was with the Department of Microelectronics, Faculty of Electronics Engineering, University of Niš, as an Assistant/Associate Professor of physical electronics. He also served as a Guest Researcher at the German National Center for Information Technology, Sankt Augustin, Germany, in 1995 and 1996, where he was involved in a research on coupled oxidation and diffusion process simulation. From 1998 to 2007, he was a Principal Researcher at the Delft University of Technology, Delft, The Netherlands, where he has led a team for standardization of the Mextram bipolar transistor model with compact model coalition. Since 2007, he has been a Senior R&D Engineer at Silvaco Inc., Santa Clara, CA, USA, and St. Ives, U.K., responsible for all aspects of compact model development and implementation in Silvaco EDA tools. He has authored about 50 cited publications and a monograph *Multigrid Methods for Process Simulation* in the Springer Computational Microelectronics series. His current research interests include compact/SPICE modeling for flexible electronics, thin-film transistors, and emerging electron devices.

Dr. Mijalković is a member of the IEEE EDS Compact Modeling Committee. He received an External European Research Program Grant from Digital Equipment Corporation in 1990 for his Magister and Ph.D. research. He has also founded and chaired the four editions of the Compact Modeling for RF Application Workshop associated with the IEEE Bipolar/BiCMOS Circuits and Technology Meetings.

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He joined Philips Research Laboratories, Eindhoven, The Netherlands, in 1996. In 2005, he was promoted to Senior Principal Scientist. In 2006, he joined NXP Semiconductors, Beijing, China, which was, at that time, spun off from Philips, where he has co-developed and industrialized the well-known compact models MOS Model 9, MOS Model 11, and PSP, the latter of which was elected as the CMC standard MOSFET model in 2005. He is the Principal Developer of JUNCAP2, a comprehensive model for MOSFET junctions. He is currently involved in the measurement, understanding, and modeling of the HBT safe operating area. He has published more than 100 journal papers, conference contributions, and book chapters.

Dr. Scholten served as the IEDM Committee Member twice from 2000 to 2001 and from 2013 to 2014. He has been an Editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES since 2015.

Yogesh Singh Chauhan (SM'12) is an Associate Professor at IIT Kanpur, Kanpur, India. He was with the Semiconductor Research and Development Center, IBM, Yorktown Heights, NY, USA, from 2007 to 2010, the Tokyo Institute of Technology in 2010, and the University of California at Berkeley, Berkeley, CA, USA, from 2010 to 2012. He is the Lead Developer of the industry standard BSIM-BULK (formerly BSIM6) model. He is also the co-developer of the ASM-HEMT model for GaN HEMTs, which is under industry standardization at the compact model coalition. His current research interests include characterization, modeling, and simulation of semiconductor devices.

Dr. Chauhan was a Technical Program Committee Member of the IEEE International Conference on Simulation of Semiconductor Processes and Devices 2013 and the IEEE European Solid-State Device Research Conference 2016/2017. He is a member of the IEEE-EDS Compact Modeling Committee. He received the Ramanujan Fellowship in 2012, the IBM Faculty Award in 2013, and the P. K. Kelkar Fellowship in 2015.

Ananda S. Roy received the B.E. degree in electronics and telecommunications engineering from Jadavpur University, Kolkata, India, in 2001, the M.Tech. degree in microelectronics from IIT Bombay, Mumbai, India, in 2003, and the Ph.D. degree in microelectronics and microsystems from the Swiss Federal Institute of Technology Lausanne, Lausanne, Switzerland, in 2007.

Since 2009, he has been with Intel Corporation, Hillsboro, OR, USA, where he has contributed to the development of Intel's internal MOSFET compact model. He has contributed to several publications in compact modeling area. His current research interests include device and variation modeling for digital, analog, and RF applications.

Dr. Roy is an Associate Editor of the *Journal of Computational Electronics*.

Sadayuki Yoshitomi (M'18) received the Ph.D. degree from Yokohama National University, Yokohama, Japan, in 1993.

In 1993, he joined the Research and Development Center, Toshiba Corporation, Kawasaki, Japan, where he was involved in the research and development of RF BiCMOS technologies. In 1998, he moved to the System-LSI Development Division, where he was involved in the developments of RF-CMOS process design kits from 130 to 40 nm. Since 2016, he has been with Toshiba Memory Corporation, Yokohama, Japan, where he was involved in the development of process design kits and compact models for 3-D NAND-Flash memory products.

Dr. Yoshitomi is currently a member of Technical Program Committee of the European Solid State Device Research Conference, the BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium, the Mixed Design of Integrated Circuits and Systems Conference, and the International Conference on Microwave & THz Technologies and Wireless Communications (IRPhE') and the Extended Compact Modeling Committee of MOS-AK.

Kaikai Xu received the Ph.D. degree from the University of California at Irvine, Irvine, CA, USA.

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Dr. Xu has been a member for the IEEE Electron Devices Society Optoelectronic Devices Committee since 2015, has been a member for the Administrative Committee of the IEEE Electron Device Society since 2015, was the Vice Co-Chair for the Optical Society of America Photonics and the Opto-Electronics Division, Laser Systems Technical Group from 2016 to 2017, has been a member of the Illuminating Engineering Society of the North America Light Sources Committee since 2016, and has been the Chair for the IEEE Nanotechnology Council Nano-Optics, Nano-Photonics, and Nano-Optoelectronics Technical Committee since 2016. He serves on the Technical Program Committee for numerous international conferences held by the IEEE, OSA, and SPIE.