Compact Modeling of Charge Transfer in Pinned Photodiodes for CMOS Image Sensors

Raffaele Capoccia, Assim Boukhayma, Farzan Jazaeri, and Christian Enz, *Student Member, IEEE*

***Abstract*— In this paper, we propose a physics-based compact model of the pinned photodiode (PPD) combined with the transfer gate. A set of analytical expressions is derived for the 2-D electrostatic profile, the PPD capacitance, and the charge transfer current. The proposed model relies on the thermionic emission current mechanism, the barrier modulation, and the full-depletion approximation to obtain the charge transfer current. The proposed physics-based model is fully validated with technology computer-aided design simulations, i.e., stationary and optoelectrical simulations. The development of such a compact model for PPD represents an essential step toward the design, simulation, and optimization of PPD-based pixels in CMOS image sensors.**

***Index Terms*— Charge transfer, CMOS image sensors (CISs), compact modeling, pinned photodiode (PPD).**

I. Introduction

PINNED photodiodes (PPDs) are key components in CMOS image sensors (CISs). They are mainly used into mass market applications, e.g., smartphones, tablets, and digital cameras, but also advanced high-end scientific and industrial applications. The PPD has been first introduced in charge-coupled devices [1]. Nowadays, PPDs are the photodetecting element in CIS, determining their performance in terms of sensitivity, image lag, dark current, and full-well capacity (FWC) [2]–[4]. The PPD is usually associated with a transfer gate (TG), which transfers the electrons accumulated during illumination within the photodiode to the sense node (SN), having lower capacitance and hence providing a readable voltage variation. The PPD/TG interface is becoming more critical for further improvements [5] in advanced applications, e.g., subelectron read noise levels [6], [7], high frame rates [8], [9], and time of flight (ToF) [10], [11]. Moreover, the nonideal effects due to the charge transfer mechanism from the PPD to the SN, which affects both the static and dynamic operations, has recently become a new research topic [12]–[14].

The compact modeling of PPD-based pixels is still at its early stage of development and to the best of our knowledge, no compact model has been developed so far. A charge transfer model based on thermionic emission theory has been recently developed in [12]. This model shows that the floating diffusion capacitance and the area of the photodiode also affect the charge transfer. However, this paper does not model the potential barrier, V_b, and does not give a closed form expression for the charge transfer current. Given the advantages of using explicit expressions for compact modeling purposes, we developed a physics-based model of the PPD together with the TG. A detailed electrostatic analysis of the PPD and TG is carried out, allowing to derive the electrical parameters. The potential barrier between the PPD and TG is analytically expressed as a function of the PPD and TG voltages and other physical parameters. This leads to a physics-based model of the charge transfer current of the photogenerated electrons from the PPD to the SN. The proposed model is verified and validated with Synopsys technology computer-aided design (TCAD) [15] simulation results.

This paper is organized as follows. In Section II, the operation principle of the PPD together with the TG is briefly explained. Section III addresses a detailed analysis of the static parameters, validated by TCAD simulations. Section IV is devoted to the influence of the potentials and physical parameters on the potential barrier, supported by transient simulations performed in TCAD. In Section V, adopting thermionic emission current mechanism approach, a physics-based model of the charge transfer current is developed and validated with TCAD simulation results. Finally, the conclusions are drawn in Section VI.

II. Principle of Operation and Device Structure

A PPD is a device made by a n-well buried in a p-substrate. On top of this well, a thin layer of highly p-doped semiconductor takes place. Even though the structure does not differ a lot from a standard p-n photodiode, the working principle of this device is quite different. A PPD operates as a unipolar charge accumulator, where the photogenerated electrons, N_e, can be stored. Lowering the energy barrier (below the energy at the PPD well), by imposing a positive voltage to the TG next to the PPD, allows the accumulated charge to move toward the SN. This node is initially set to a positive reset voltage, e.g., 2.5 V. It should be noted that the TG isolates the PPD and SN capacitances, leading to a lower capacitance at the SN. Due to the fact that the SN capacitance, C_{SN}, is lower than the PPD capacitance, C_{PPD}, the transferred electrons cause a

Manuscript received May 25, 2018; revised July 18, 2018, August 28, 2018, and October 2, 2018; accepted October 5, 2018. Date of publication October 30, 2018; date of current version December 24, 2018. The review of this paper was arranged by Editor A. S. Roy. *(Corresponding author: Raffaele Capoccia.)*

The authors are with the Integrated Circuits Laboratory, École Polytechnique Fédérale de Lausanne, 1015 Lausanne, Switzerland (e-mail: raffaele.capoccia@epfl.ch).

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Digital Object Identifier 10.1109/TED.2018.2875946

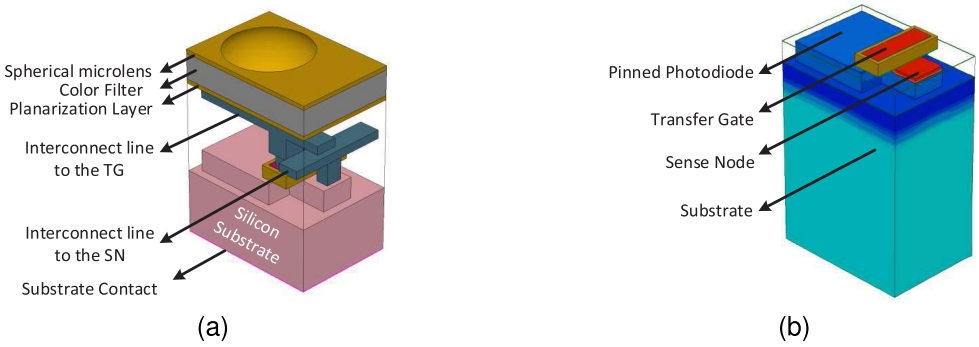

Fig. 1. (a) Back end—the microlens, the color filter, and the interconnections. (b) Front end—the PPD, the TG, and the SN.

higher voltage variation that can be processed by the readout circuitry [$\Delta V_{SN} = (qN_e)/C_{SN}$].

The 3-D geometry of the back end is depicted in Fig. 1(a), including the silicon at the bottom, the two metal interconnects, connected through a via to the TG and the SN contacts. As illustrated, a color filter is sandwiched between a layer of deposition on the bottom and a spherical microlens on the top. The color filter is indeed chosen accordingly to the wavelength used for the input light. In this paper, an ideal red color filter is used centered at a wavelength equal to 650 nm. Fig. 1(b) shows a 3-D view of the front end of the device, including the photodiode, the TG made in polysilicon and surrounded by an insulating material, and the SN diffusion. Blue, red, and light blue are corresponding to the p^+type, n^+ type regions, and p substrate, respectively.

III. PPD Device

A. Electrostatics in PPD Device

On top of Fig. 2, the simplified cross section of a PPD is shown, made by a p^+np structure. In this figure, the electrostatic potentials of the PPD are also shown under different conditions. Fig. 2(a) corresponds to the equilibrium condition, while the impact of charge transfer is sketched in Fig. 2(b) and the one of light in Fig. 2(c). At the equilibrium condition, the n-well region is partially neutral and the electrostatic potential remains almost constant. The two built-in potentials, V_{bi1} and V_{bi2}, are illustrated in Fig. 2(a). The doping concentration in the p^+ layer is typically higher than the one in the p-substrate. Hence, the built-in potential of the p-n junction, V_{bi2}, is lower than the one with the p^+ layer, V_{bi1}. After the free carriers are transferred from the PPD, the maximum value of the electrostatic potential increases, allowing to make the n-well fully depleted of the carriers. In Fig. 2(b), V_{pin} is retrieved as the maximum variation of the electrostatic potential, in consistency with the definition given in [16]. On the other hand, when the photodiode is exposed to the light, the entire electrostatic potential moves toward the flat-band condition as shown in Fig. 2(c).

In this paper, the electrostatic analysis of the PPD is performed for the structure depicted in Fig. 3(a). This structure is characterized by a fully depleted n-well. The full-depletion of the n-well can be achieved as soon as all the accumulated charges are transferred to the SN during the reading operation. Since a full-depletion approximation is assumed along the

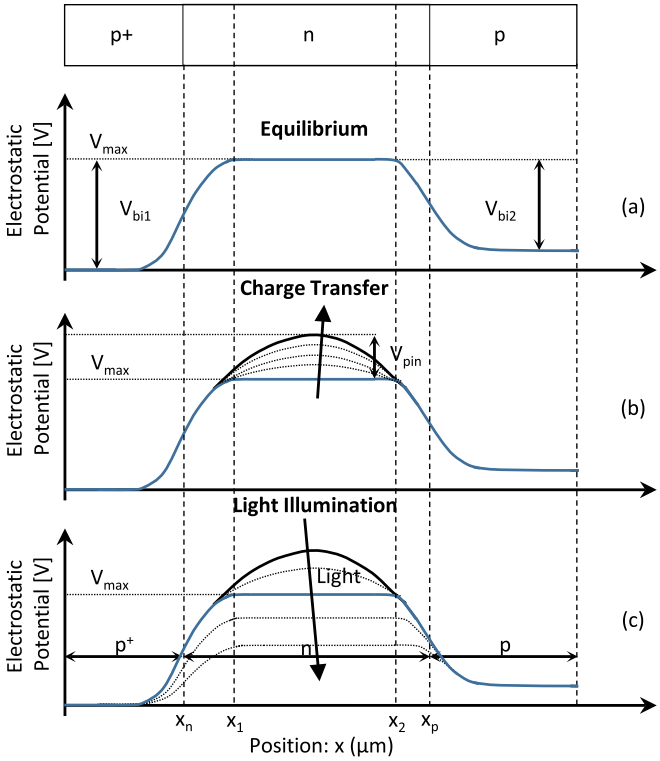

Fig. 2. Sketches of the electrostatic potential of the PPD at (a) equilibrium condition, two built-in potentials, V_{bi1} and V_{bi2}, and maximum potential, V_{max}, are shown. (b) Maximum value of the electrostatic potential increases until the empty condition is reached while transferring the charges from the PPD to the SN. The maximum variation of the electrostatic potential is the pinning voltage, V_{pin}, as defined in [16]. (c) Potential moves toward the flat-band condition due to the applied illumination.

device, the free carrier concentrations are negligible compared to the fixed charge density. In TCAD simulations, the full-depletion is reached by a proper choice of the physical parameters; hence, the two depleted regions intersect in one point. This is a particular case where the maximum of the electrostatic potential, V_{max}, is equal to the highest built-in potential, namely, the one of the p^+n junction, V_{bi1}. If the length of the n-well is further reduced, the structure is still pinned, but V_{max} is lower than V_{bi1}. In the simplified cross section of a PPD illustrated in Fig. 3(a), the left side corresponds to the top of the structure shown in Fig. 1(b). To simplify the analysis, the following assumptions are added: 1) an abrupt transition between the neutral and the depleted region is used

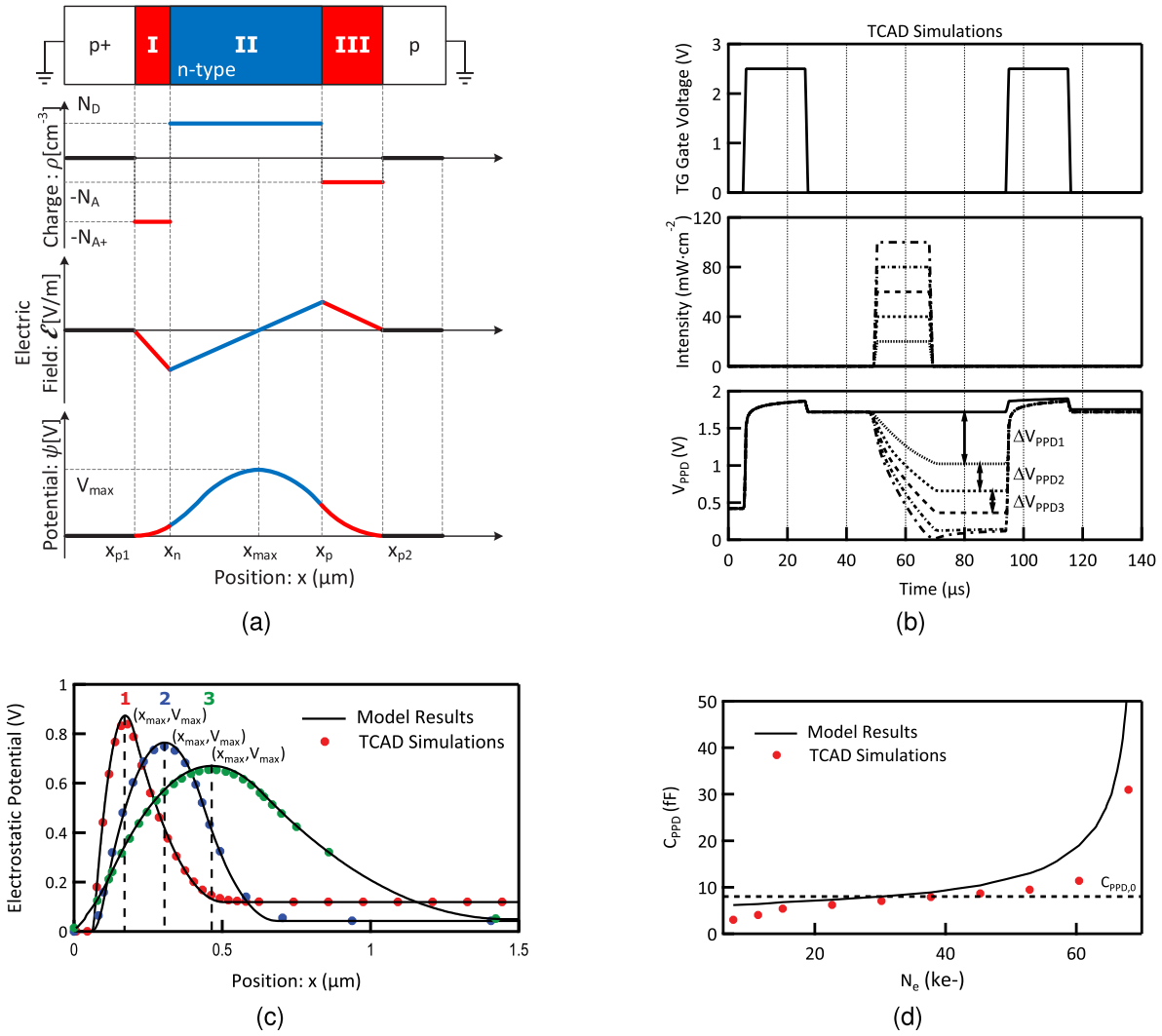

Fig. 3. (a) Simplified cross section of a PPD under the assumptions of full-depletion and abrupt transition. $\rho(x)$ is the charge distribution, $\mathcal{E}(x)$ is the electric field, and $\psi(x)$ is the electrostatic potential along the position x. x_n is the junction boundary between p^+ and n layers, x_p is the junction boundary between n and substrate, x_{p1} and x_{p2} are the limits of the depletion regions on the p^+ and p regions of the two junctions, respectively. Expressions for the electric field and the electrostatic potential are given in Appendix A. (b) Optoelectrical transient simulations—the gate voltage applied to the TG, the intensity of the incident wave and the electrostatic potential inside the PPD. The changes in the electrostatic potential are proportional to the incident light and can be used to derive the PPD capacitance. (c) Electrostatic potential inside the PPD structure for Case 1–3 reported in Table I. The profile simulated in TCAD is compared with the expression derived in the proposed model. x_{max} is at 170 nm and V_{max} is 0.84 V at 300 K in case I, 305 nm and 0.76 V in case II, and 460 nm and 0.67 V in case III. (d) PPD capacitance as function of the photogenerated electrons—TCAD simulations are compared with the proposed model.

for both junctions and 2) both the applied voltages in the substrate and at the pinned layer are set equal to zero. This condition is required to impose the boundary conditions. Under these assumptions, the total charge density $\rho(x)$ along the PPD is plotted in Fig. 3(a). Solving the Poisson equation $\nabla^2\psi(x) = -\rho(x)/\varepsilon_s$, analytical expressions of the electric field, $\mathcal{E}(x)$, and electrostatic potential, $\psi(x)$, are derived and reported in Appendix A. $\mathcal{E}(x)$ and $\psi(x)$ are depicted in Fig. 3(a). The maximum of the electrostatic potential, V_{max}, and its corresponding position, x_{max}, are obtained and given by the following expressions:

$$x_{max} = x_n + \frac{N_{A^+}}{N_D}(x_n - x_{p1}) = x_p - \frac{N_A}{N_D}(x_{p2} - x_p) \quad (1)$$

$$V_{max} = \frac{qN_{A^+}}{2\varepsilon_s} \cdot \frac{N_{A^+} + N_D}{N_D}(x_n - x_{p1})^2 \quad (2)$$

where N_{A^+} and N_D are the doping concentrations in the p^+ and the n-well regions, q is the electron charge, and ε_s is the absolute permittivity of silicon. The maximum of the potential occurs at x_{max}, corresponding to the point where the electric field is equal to zero. Hence, x_{max} is obtained by solving $\mathcal{E}(x) = 0$ in the depleted n region resulting in (2). Imposing the charge neutrality between the depleted p and n regions, given by

$$N_A x_{p2} - N_{A^+} x_{p1} = (N_A + N_D)x_p - (N_{A^+} + N_D)x_n \quad (3)$$

leads to the right-hand side of (2). The two derived expressions of (2) confirm that x_{max} is comprised between x_n and x_p.

TABLE I
MAIN PARAMETERS OF THREE CASES OF PPDS

	Case 1	Case 2	Case 3
$\mathbf{N}_{A+}$ (cm^{-3})	10^{18}	10^{17}	10^{16}
$\mathbf{N}_{D}$ (cm^{-3})	10^{17}	2×10^{16}	5×10^{15}
$\mathbf{N}_{A}$ (cm^{-3})	10^{16}	10^{15}	10^{15}
$\mathbf{x}_{n}$ (nm)	70	100	120
$\mathbf{x}_{p}$ (nm)	200	430	630
$\mathbf{x}_{max}$ (nm)	170	305	460
$\mathbf{V}_{max}$ (V)	0.84	0.76	0.67

Inserting x_{max}, obtained from (2), into (A.2) leads to the expression for the maximum of the electrostatic potential, V_{max}, given by (2).

Fig. 3(c) shows the TCAD simulation results for the electrostatic potential profile along the device, for different geometrical parameters, reported in Table I. The potential profile of this device obtained with TCAD simulations and the model is plotted. The agreement between the model and TCAD simulations is excellent. The equilibrium FWC (EFWC) is defined in [17] as the maximum photogenerated charges that can be accumulated in the PPD in dark conditions and neglecting the TG leakage current. Following this definition, the EFWC can be accurately estimated by the number of electrons stored in the PPD at equilibrium condition. The full well number of photogenerated electrons in the PPD volume between x_2 and x_1 (see Fig. 2) is given by $N_{e,EFWC} = A_{PPD}(x_2 - x_1)N_D$, where A_{PPD} is the area of the PPD.

B. PPD Capacitance

During illumination, the electrostatic potential inside the n-well decreases proportionally to the intensity of the light [18]. The ratio of the accumulated charges and the voltage variation corresponds to the capacitance $C_{PPD} = (q\,N_e)/\Delta V_{PPD}$. On the other hand, a detailed analytical model has been proposed in [19], the well-known expression of the junction capacitance [20] has been used in [2] and [21] to obtained an analytical expression of C_{PPD}. Therefore, C_{PPD} can be expressed as

$$\left(\frac{C_{PPD}}{A_{PPD}}\right)^2 = \frac{q\varepsilon_s}{2(V_{max} - \Delta V)} \frac{N_D \cdot N_{A+}}{N_D + N_{A+}} \tag{4}$$

where ΔV is the variation of the electrostatic potential due to photogeneration. Typically for PPDs, $N_{A+} \gg N_D$ while ΔV can be expressed as a function of N_e, equal to N_e/C_{PPD}. After some mathematical manipulations, the derived expression is

$$\left(\frac{C_{PPD}}{A_{PPD}}\right)^2 \approx \frac{q\varepsilon_s N_D}{2V_{max}\left(1 - \frac{N_e}{N_{e,0}}\right)} \tag{5}$$

where N_e and $N_{e,0}$ are, respectively, the number of photogenerated electrons and the amount of electrons in the n-well at the equilibrium, equal to $C_{PPD} \cdot V_{max}$. In order to validate the proposed formula of C_{PPD}, a TCAD transient simulation with different values of light intensity is carried out. The light is represented by a linearly polarized plane wave for which the intensity, the wavelength, and the angle of incidence can be properly set. In the performed TCAD simulations, the illumination is set to have a wavelength of 650 nm and a normal angle with respect to the surface of the device. The applied voltage to the TG, the pulses of light, and the PPD voltage with respect to time are depicted in Fig. 3(b). First, to deplete the PPD from the charges, a positive potential is applied to the gate. Then, the PPD is exposed to a pulse of light which generates an amount of photoelectrons. Increasing the light intensity leads to an increase of the PPD voltage variation. To evaluate the $C_{PPD} = N_e/\Delta V_{PPD}$, N_e and the maximum voltage variation, ΔV_{PPD}, are required to be extracted properly using TCAD simulations. ΔV_{PPD} can be readily determined from Fig. 3(b) for each value of the light intensity. In addition, N_e is estimated in TCAD simulations using the optical generation parameter, providing informations of the semiconductor charge density. This parameter is integrated over the active volume and then multiplied by the integration time. To validate the proposed model, the equivalent capacitance of the PPD is obtained through (5) and compared to TCAD simulations in Fig. 3(d). The agreement between the numerical calculation and the model is reasonable.

IV. POTENTIAL BARRIER MODELING

In this section, a physics-based model for the charge transfer from the PPD to the SN is derived. This approach relies on the transfer mechanism limited by the interface properties between the PPD and TG. This assumption is verified for relatively short devices that are not limited by internal diffusion mechanism [22]. The n-p junction between the PPD n-well and the TG results in a potential barrier between the charge accumulation region and the semiconductor beneath the gate, as shown in Fig. 4(a). This barrier has been already reported in [12] and measurements are performed in [23]. A model of this potential barrier is proposed here, predicting its behavior with respect to the applied voltage to the TG and PPD voltage. For this purpose, an equivalent 2-D structure of all the regions crossed by path A is shown in Fig. 5(a). The proposed structure is a stretched version of the effective charge transfer path from the PPD to the SN and contains the MOS part, the p^+ layer, the n-well, and the p substrate. Path A is used to perform an electrostatic analysis deriving the potential barrier from Fig. 5(b) and illustrating the impact of the TG voltage. On the other hand, Path B corresponds to the current path and it is introduced to derive the proposed model of the transferred charges, validated by TCAD simulation results. As shown in Fig. 4(b), the region beneath the TG is depleted of electrons along the effective charge transfer path. The SN is biased to the value of 2.5 V, leading to the fully depleted region of the carriers around this node due to the high shift in the quasi-Fermi potential. In such configuration, with a positive voltage applied to TG, there is no inversion layer under the gate. The presence of mobile charges under the TG can impact the barrier height. However, in this particular case, where the SN is kept to a high voltage value and the substrate to ground, any mobile charge under the TG will move toward the corresponding contact. Moreover, it is assumed that the SN voltage

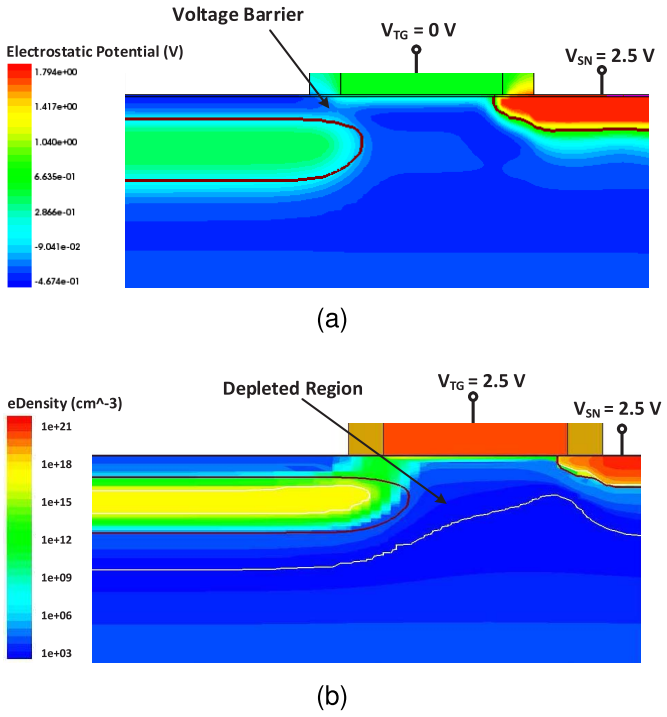

Fig. 4. (a) Electrostatic potential of the interface between the PPD and the TG when $V_{TG} = 0$ V. Evidence of a potential barrier between the n-well and the semiconductor beneath the TG. (b) Interface region is fully depleted along the effective charge transfer path, for a $V_{TG} = 2.5$ V and $V_{SN} = 2.5$ V.

is constant, allowing to neglect the impact of its variation on the charge transfer [12]. The workfunction difference between the metal and the semiconductor together with the voltage applied to TG determine the surface potential, ψ_s. During the rising edge of V_{TG}, all the electrostatic potentials of the MOS structure are shifting up, as illustrated in Fig. 5(a). On the other hand, we define the potential barrier V_b as the voltage difference between the voltage inside the n-well, V_{PPD}, and the minimum voltage in the p-doped semiconductor beneath TG, V_{min}. This allows to predict the behavior of the barrier during all the transfer time and leads to

$$V_b(t) = V_{PPD}(t) - V_{min}(t). \tag{6}$$

The term $V_{PPD}(t)$ can be derived by the following expression:

$$V_{PPD}(t + \Delta t) = V_{PPD}(t) + \frac{i(t)\Delta t}{C_{PPD}} \tag{7}$$

where $i(t)$ is the charge transfer current and Δt is the time interval between two consecutive instances along the discretized time axis. Starting from the initial value, $V_{PPD,0}$, the values of $V_{PPD}(t)$ are calculated at each iteration by the potential variation due to the amount of transferred charges, $i(t)\Delta t$.

On the other hand, Fig. 5(a) depicts the potential along path A at different instants during the rise of V_{TG}. It clearly shows that the the potential barrier V_b is reduced due to the increase of the TG gate voltage, which enables the transfer of the charges to the SN. Using again the full-depletion approximation, the charge distribution, and electric field and electrostatic potential along the proposed path are derived and plotted in Fig. 5(b). The expressions for the electric field and electrostatic potential are presented in Appendix B. Starting from a_2, the solution of the Poisson equation is equal to

$$\psi(a) = \psi_s - E_s(a - a_2) + \frac{qN_{A^+}}{2\varepsilon_s}(a - a_2)^2. \tag{8}$$

The increase in the gate voltage will increase the depletion region beneath the gate, until merging with the depleted region around the n-well. Under this assumption, $\rho(a)$ can be considered to be equal to $-qN_{A^+}$ for $a_2 \le a \le a_5$. $V_{min}(t)$ is the minimum value of the electrostatic potential in the region between the PPD and the semiconductor beneath the TG, while a_{min} is the position of V_{min} ($V_{min} = \psi(a_{min})$). Since, in this point, the value of the electric field must be zero, a_{min} is equal to $a_2 + t_{p^+} - d_{p1}$, where t_{p^+} is the thickness of the p^+ layer and d_{p1} is the width of the depletion region of the p^+n junction in the p^+ region [see Fig. 5(b)]. The solution of the Poisson equation allows to obtain an analytical expression of the barrier, which includes the effect of V_{TG}.

By using the expression of the depletion region in a metal–oxide–semiconductor as a function of the applied gate voltage (reported in Appendix B) and after some mathematical manipulations, V_{min} results in

$$\begin{aligned} V_{min}(t) = {} & \frac{qN_{A^+}}{2\varepsilon_s}(t_{p^+} - d_{p1})^2 + \\ & - (t_{p^+} - d_{p1})\frac{qN_{A^+}}{C_{ox}}\left[1 - \sqrt{1 + \frac{C_{ox}^2}{2q\varepsilon_s N_{A^+}}V_{TG}(t)}\right] \\ & + \frac{q\varepsilon_s N_{A^+}}{2\,C_{ox}^2}\left[1 - \sqrt{1 + \frac{C_{ox}^2}{2q\varepsilon_s N_{A^+}}V_{TG}(t)}\right]^2. \end{aligned} \tag{9}$$

From the proposed formula, it can be seen that the height of the potential barrier is a function of V_{TG}, the doping concentration in the semiconductor and the thickness of the p^+ layer t_{p^+}, which defines the position of the n-well. To verify the validity of the proposed analytical expression of the potential barrier and its variation over time, a transient simulation in TCAD is performed. This simulation decouples the illumination from the charge transfer, by having first a pulse of light and then a pulse of voltage applied to the TG. Thus, the light does not affect the potential barrier during the transfer and its impact is not taken into account in the proposed model of V_b. To guarantee a full charge transfer, the width of the TG pulse is set to be longer than needed. Moreover, in the specific case in which the transfer time is set to be shorter, i.e., high-speed applications such as ToF, the dynamic effects of the charge transfer, which are not considered in this derivation, have to be included. During this simulation, the SN is kept at the constant voltage of 2.5 V and a constant value equal to 7 fF has been used as a good approximation of C_{PPD} within the range of interest. The potential profile along the path B [Fig. 5(a)] is plotted during different instants of time in Fig. 5(c). The simulation results show that this potential barrier is modulated by the gate voltage, as predicted by (6). All different values of V_b are calculated from each potential profile and plotted as a function of the simulation time in Fig. 5(d). Initially, the barrier decreases following the linear

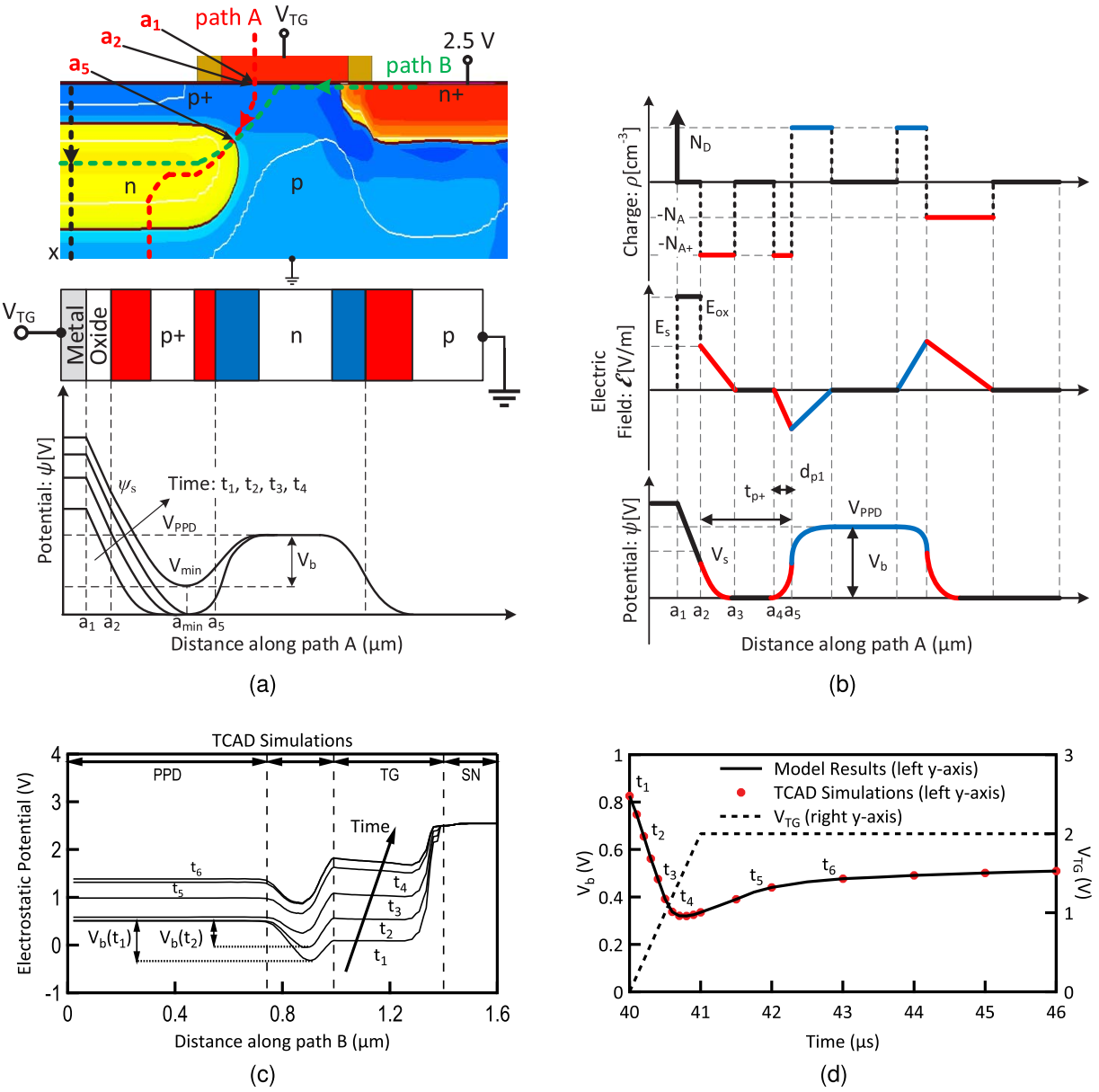

Fig. 5. (a) Section of the interface between the TG and PPD with the 2-D equivalent stretched version. Electrostatic potential at the interface between the PPD and the TG during the sweep of the gate voltage. The barrier voltage is changed by the TG and PPD voltage values. (b) Charge distribution, electric field, and electrostatic potential under the assumptions of fully depletion and abrupt transitions. (c) Electrostatic potential along the path B crossing the PPD well, the interface, the area beneath the TG and the SN, for different time instants. $t_1 - t_4$ corresponds to the rising edge of V_{TG}, while $t_5 - t_6$ refer to V_{TG} constant. (d) Value of the potential barrier during time along the charge transfer period. The behavior of the barrier is well predicted by the proposed model.

slope of the V_{TG} rising edge. Once the gate voltage reaches the maximum value and remains constant, the potential barrier also starts to saturate and is slowly changing due only to the charge transfer. As shown in Fig. 5(d), the simple model given by (6) is in excellent agreement with the TCAD simulation results. Increasing V_{TG} lowers V_b until V_{TG} reaches the threshold voltage of the MOS structure, above which the surface potential, ψ_s, only increases logarithmically with V_{TG} and most of the voltage drop occurs across the oxide [24]. This means that the above-mentioned threshold, the surface potential will almost not be influenced by V_{TG} and no additional potential barrier reduction is achieved. On the other hand, a higher voltage will force the surface p^+ layer to be further depleted. Once this layer is fully depleted, the pinned structure is no longer present and the potential inside the n-well is then determined by the V_{TG} voltage.

V. Charge Transfer Modeling in PPD

A. Charge Transfer Across a Potential Barrier

Once the analytical expression of the potential barrier is developed and validated with TCAD simulations, it can be used to derive an expression of the charge transfer current. Relying on the thermionic emission mechanism, the transfer current crossing a potential barrier is obtained. The thermionic emission theory states that the electrons which have enough

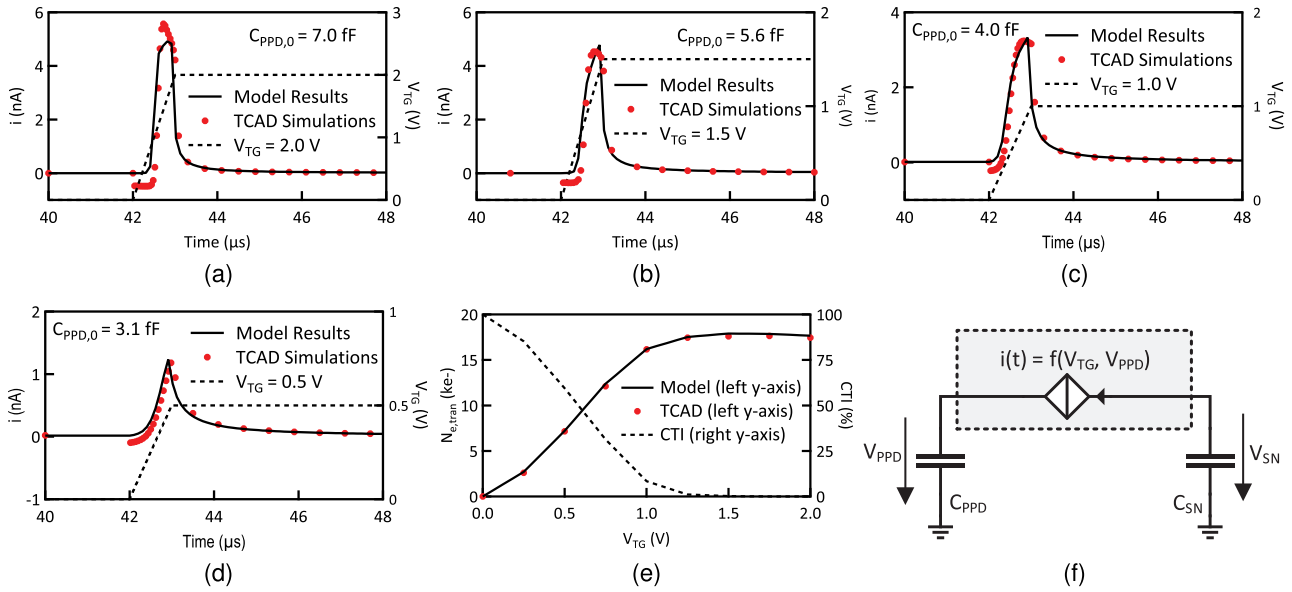

Fig. 6. (a)–(d) Current pulses representing the charge transfer from PPD to SN for four different V_{TG} values. TCAD simulations are compared with the proposed model. (e) Total number of transferred electrons from PPD to SN and CTI as a function of V_{TG}, derived when integrating the current over the time. (f) Proposed equivalent circuit for the PPD, TG, and SN, where the function f is given in (10).

thermal velocity in the transfer direction will cross the barrier on the charge transfer path [20] and it has been used to model the charge transfer between the PPD and the SN [12], [25]. In TCAD simulations, path A is chosen as the path with the minimum barrier, and therefore the highest current density. In the model, the assumption is that all the current is flowing along the minimum barrier path, path A. Based on this transportation mechanism, the expression of the charge transfer current that embeds the effects of both the PPD and TG voltages and the other physical parameters on V_b is derived. The charge transfer current is given by

$$i(t) = I_0 \cdot \exp\left[-\frac{V_b(t)}{U_T}\right] \tag{10}$$

where V_b is given by (6) and (9) and I_0 is equal to AS_AT^2, with A equal to the Richardson constant [20], and S_A is the area of the cross section on the charge transfer path at the barrier position. To validate this expression, the total current that flows through the SN can be extracted from the transient TCAD simulation results. The latter is shown in Fig. 6(a)–(d) for different values of V_{TG}: 2.0, 1.5, 1.0, and 0.5 V. The simulation results obtained during the charge transfer can be compared with (10). The agreement between TCAD simulation results and the proposed model is good and confirms that the derived expression predicts the characteristic of the charge transfer from the PPD to the SN. The exact values of the cross section S_A have to be extracted from TCAD by looking at the current density distribution during the charge transfer. Based on the analysis of C_{PPD} shown in Section III-B, we initially considered C_{PPD} as a constant parameter of the model, named $C_{PPD,0}$, for the specific value of light used during simulation. The value of $C_{PPD,0}$ is equal to 7 fF and is shown in Fig. 3(d). However, to obtain such an agreement between TCAD simulations and the proposed model, the constant value $C_{PPD,0}$ has been used as a fitting parameter. Thus, the value of $C_{PPD,0}$ has been reported for each simulated case in Fig. 6(a)–(d). This variation is reasonably predicted in Fig. 3(d), where the value of C_{PPD} is not independent of the number of electrons stored in the photodiode. Although the dynamic modeling of C_{PPD} will need a further investigation, its use as a fitting parameter allows to verify the proposed expression for the charge transfer current. All the current pulses in Fig. 6(a)–(d) exhibit almost zero transferred charges untill the TG voltage reaches a precise value. The voltage beneath the gate has to be higher than the PPD voltage in order to allow an efficient transfer of the integrated charge. The delayed charge transfer with respect to the TG voltage is consistent with [26]. When the final value of V_{TG} is below V_{PPD}, it results in an incomplete charge transfer. The latter is shown in the last two cases in Fig. 6(c) and (d), where the pulse of current is considerably smaller than Fig. 6(a) and (b). On the other hand, initially, the current exhibits negative values in transient simulations. This negative current can be explained as a capacitive coupling (overlap) between the TG and the SN. The calculated current through the proposed model does not include this phenomena, and hence, the two curves substantially differ in this interval of time. The data of Fig. 6(a)–(d) can be used to evaluate the charge transfer inefficiency (CTI) for a total integrated charge of 18.000 e^- in the PPD as a function of V_{TG}, over a transfer time of 10 μs. Once integrating the current over the time, the total transferred charge is obtained and plotted in Fig. 6(e), which is in excellent agreement with results of TCAD simulation. The CTI is plotted together with the amount of transferred electrons, $N_{e,tran}$, in Fig. 6(e).

B. Model Implementation and Equivalent Circuit of PPD

In order to simulate the transient behavior with the proposed model, a quasi-static assumption together with (5), (6), and (10) is used. An equivalent circuit for the charge transfer from the PPD to the SN is given in Fig. 6(f). The PPD and the SN are replaced by two equivalent linear and

time-invariant capacitors, C_{PPD} and C_{SN}. The TG is replaced by a voltage-controlled-current-source (VCCS). Since in a p^+np PPD, the electrons are transferred to the SN, the VCCS indicates a current flowing from the SN to the PPD. Relying on the proposed model, the transfer current is expressed as a function of V_{TG} and V_{PPD} according to (10). This equivalent circuit, together with the proposed expressions, represents an essential step toward the circuit-level design of PPD-based pixels in CISs. This model covers the case where the charge transfer is limited by the potential barrier between the PPD and the TG, with the SN voltage remaining at a constant voltage and always higher than the PPD maximum voltage and the TG channel voltage.

VI. Conclusion

In this paper, a physics-based compact model for the PPD with the TG is developed and fully validated with TCAD optoelectrical simulations. This model is able to predict the electrical behavior of the charge transfer from the PPD to the SN for different values of the physical parameters, when the transfer is only limited by the potential barrier between the PPD and TG. The proposed model relies on the thermionic emission current mechanism, full-depletion approximation, and barrier modulation due to V_{TG} and V_{PPD} to express the charge transfer current with respect to the physical parameters. The presented physics-based model provides the core of a more complete future PPD compact model, enabling the design and circuit-level simulations of a PPD-based pixel in CISs.

Appendix

A. Electrostatics in PPD device

Solving Poisson equation, the electric field and the potential profiles in the PPD device are, respectively, given by

$$\begin{aligned}\mathcal{E}(x) &= -\frac{qN_{A^+}}{\varepsilon_s}(x-x_{p1})\left[u(x-x_{p1})-u(x-x_n)\right] \\ &+\left[\frac{qN_D}{\varepsilon_s}(x-x_n)+\mathcal{E}(x_n)\right]\left[u(x-x_n)-u(x-x_p)\right] \\ &+\left[-\frac{qN_A}{\varepsilon_s}(x-x_{p2})+\mathcal{E}(x_p)\right]\left[u(x-x_p)-u(x-x_{p2})\right]\end{aligned} \tag{A.1}$$

$$\begin{aligned}\psi(x) &= +\frac{qN_{A^+}}{2\varepsilon_s}(x-x_{p1})^2\left[u(x-x_{p1})-u(x-x_n)\right] \\ &+\left[-\frac{qN_D}{2\varepsilon_s}(x-x_n)^2+\frac{qN_{A^+}}{\varepsilon_s}(x_n-x_{p1})\,x+\psi(x_n)\right] \\ &\times\left[u(x-x_n)-u(x-x_p)\right] \\ &+\left[\frac{qN_A}{2\varepsilon_s}(x-x_{p2})^2+\psi(x_p)\right]\left[u(x-x_p)-u(x-x_{p2})\right]\end{aligned} \tag{A.2}$$

where $u(x-x_0)$ is the step function and is equal to unity when $x > x_0$ and zero elsewhere.

B. Electrostatics Along Path A

Solving Poisson equation under full-depletion approximation leads to the electric field $\mathcal{E}(a)$ and electrostatic potential $\psi(a)$ along the path A between a_2 and a_5, given by the following expressions:

$$\begin{aligned}\mathcal{E}(a) &= \left[E_s-\frac{qN_{A^+}}{\varepsilon_s}(a-a_2)\right]\left[u(a-a_2)-u(a-a_5)\right] \\ \psi(a) &= \left[\psi_s-E_s(a-a_2)+\frac{qN_{A^+}}{2\varepsilon_s}(a-a_2)^2\right] \\ &\times\left[u(a-a_2)-u(a-a_5)\right]\end{aligned} \tag{B.1}$$

where ψ_s is the surface electrostatic potential and E_s is the electric field at the surface, obtained by $\psi_s = x_d^2 qN_{A^+}/2\varepsilon_s$ and $E_s = -x_d q\,N_{A^+}/\varepsilon_s$. Moreover, to obtain (9), the following expression for the depletion region, x_d, in a metal-oxide-semiconductor is used:

$$x_d = -\frac{\varepsilon_s}{C_{ox}}+\sqrt{\left(\frac{\varepsilon_s}{C_{ox}}\right)^2+\frac{\varepsilon_s}{2qN_{A^+}}V_{TG}}. \tag{B.2}$$

This has been derived by solving Poisson equation of the TG MOS structure [27].

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Raffaele Capoccia received the B.Sc. and M.Sc. degrees in electrical engineering from the Polytechnic University of Turin, Turin, Italy, in 2012 and 2014, respectively.

He is currently a Doctoral Assistant with the Integrated Circuits Laboratory, École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, where he is involved in the research on CMOS image sensors (CISs). His current research interests include design of low-noise readout circuits and device modeling for CISs.

Assim Boukhaym received the Ph.D. degree from the Ecole Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland, and Commissariat a l'Energie Atomique (CEA-LETI), Grenoble, France, under Prof. C. Enz, with a focus on the CMOS image sensors.

He is currently a Researcher Leader with the Integrated Circuits Laboratory, EPFL.

Farzan Jazaeri received the Ph.D. degree in microelectronics from the Ecole Polytechnique Fédérale Lausanne (EPFL), Lausanne, Switzerland, in 2015.

He is currently a Research Scientist and a Project Leader with the Integrated Circuits Laboratory, EPFL. His current research interests include solid state physics and advanced semiconductor devices for operation within extreme harsh environments, i.e., high-energy particle background and cryogenic temperatures for space applications and quantum computations.

Christian Enz (M'84–S'12) received the M.S. and Ph.D. degrees in electrical engineering from the Ecole Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland, in 1984 and 1989, respectively.

In 2013, he joined EPFL as a Full Professor, where he is currently the Director of the Institute of Microengineering, Neuchâtel, Switzerland, and also the Head of the Integrated Circuits Laboratory, Neuchâtel. His current research interests include the very low-power analog and RC IC design and semiconductor device modeling.