Evaluation of Pulsed *I–V* Analysis as Validation Tool of Nonlinear RF Models of GaN-Based HFETs

Hassan Hirshy, *Member, IEEE*, Manikant Singh, *Member, IEEE*, Michael A. Casbon, *Member, IEEE*, Richard M. Perks, Michael J. Uren, *Member, IEEE*, Trevor Martin, Martin Kuball, *Senior Member, IEEE*, and Paul J. Tasker, *Fellow, IEEE*

***Abstract*— This paper evaluates the applicability of pulsed *I–V* measurements as a tool for accurately extracting nonlinear gallium nitride (GaN)-based heterojunction field-effect transistor (HFET) models. Two wafers with the identical layer structure but different growth conditions have been investigated. A series of *I–V* measurements was performed under dc and pulsed conditions demonstrating a dramatic difference in the kink effect and current collapse (knee walkout) suggesting different trapping behaviors. However, when radio frequency (RF) *I–V* waveform measurements, utilizing active harmonic load–pull, were used to study the impact of these traps on the RF performance, both wafers gave good overall RF performance with no significant difference observed. This absence of correlation between pulsed *I–V* measurement results and RF performance raises a question about the applicability of pulsed *I–V* measurements alone as a tool for extracting nonlinear device models in the case of GaN HFETs.**

***Index Terms*— Active harmonic load–pull, current collapse, gallium nitride (GaN), heterojunction field-effect transistor (HFET), high-electron mobility transistor, kink effect, knee walkout, pulsed *I–V*, trapping effect.**

I. Introduction

DUE to the unique material properties of gallium nitride (GaN), particularly high-electron mobility, high breakdown field strength, and high thermal conductivity, GaN-based transistors have found increasing market penetration in the field of radio frequency (RF) systems and now power electronics applications. However, despite recent improvements in the growth and fabrication process for the successful realization of high-performance devices, the lack of a complete understanding of the measured shortfall in the performance of GaN-based heterojunction field-effect transistors (HFETs) still stands as an obstacle to full utilization of these devices in commercial applications. One of the main issues affecting the reliability and dynamic performance is the presence and impact of charge trapping [1]. A full understanding of many trapping phenomena and their effect on the electrical performance of GaN devices remains a major challenge. It has been observed that the trapping processes can induce the so-called "current collapse," a recoverable decrease in the drain current when operated with large gate–drain voltage swings [2]. Binari *et al.* [3] suggested that the compromised microwave power performance and the current collapse of the dc device characteristics are related to the presence of traps in the surface and in the GaN buffer layer. Several established models [4], [5] have been used to describe the nonlinear behavior of HFETs and MESFET devices. However, these models generally do not consider the trapping effect on the RF performance. For the experimental investigations of the traps [6]–[11], the pulsed I–V measurement method (P-I–V) [11] is widely utilized and is often used to extract the modified device models that aim to take into consideration the charge trapping effects when predicting the transistor's RF behavior. Initially applied to GaAs-based devices, the application of these modeling concepts has now become a major focus in the development of nonlinear large-signal RF GaN HFET models. In recent years, many empirical and compact physical models have been reported, aimed at predicting the performance of the GaN HFET devices [12]–[21]. Most of these models again rely on P-I–V measurements as a model extraction and validation tool when including the trapping effects. For instance, Tarazi *et al.* [20], [21] suggested that a trap model is crucial to fit dc-I–V characteristics and accurately predict the

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H. Hirshy, M. A. Casbon, R. M. Perks, and P. J. Tasker are with the Centre for High Frequency Engineering, School of Engineering, Cardiff University, Cardiff CF24 3QR, U.K. (e-mail: hirshyh@cardiff.ac.uk; casbonma@cardiff.ac.uk; perksrm@cardiff.ac.uk; tasker@cardiff.ac.uk).

M. Singh, M. J. Uren, and M. Kuball are with the Centre for Device Thermography and Reliability, H. H. Wills Physics Laboratory, University of Bristol, Bristol BS8 1TL, U.K. (e-mail: manikant.manikant@bristol.com; michael.uren@bristol.ac.uk; martin.kuball@bristol.ac.uk).

T. Martin is with IQE, Cardiff CF3 0LW, U.K. (e-mail: tmartin@iqep.com).

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large-signal performance of GaN HFET devices. They used P-I–V measurements to acquire the fitting parameters of the trap controlling voltage in the modified nonlinear device model. Huang *et al.* [19] proposed a new 13-element drain current source model validated by measured P-I–V data with various quiescent biases and power dissipation.

In this paper, we investigate the impact of traps in AlGaN/GaN HFETs with and without the "kink effect" [22]–[23] and having differing "knee walkout" in P-I–V measurements. ("Kink effect" is a hysteresis very commonly observed in the knee region, but which is normally assumed to have no impact on the RF performance). An RF-I–V waveform measurement system utilizing active harmonic load–pull is also used to investigate the impact of these traps under RF conditions (RF-I–V). A comparative analysis of the behavior and impact of the traps under pulsed I–V and RF is reported. It is found that the measured "kink effect" in dc-I–V, and "knee walkout" in P-I–V, does not necessarily provide a valid prediction of the "knee walkout" observed under RF excitation.

II. Experimental Details

The AlGaN/GaN epi-layers were grown by metal–organic chemical vapor deposition on 4-in silicon carbide wafers. Two wafers were grown with identical layer structures of the AlGaN barrier, GaN buffer, and AlGaN nucleation layer. Both wafers incorporated a conventional Fe doping profile in the GaN bulk to suppress short-channel effects, having a peak density of 3×10^{18} cm^{-3} which decreased exponentially toward the surface. Both wafers had a 0.2-μm GaN channel region with unintentionally incorporated carbon density of 5×10^{16} cm^{-3}, but different growth conditions in the lower part of the GaN layer resulted in different carbon profiles. Wafer A had $3 \pm 1 \times 10^{17}$ cm^{-3} carbon, and wafer B had 2×10^{16} cm^{-3} carbon. Oxygen and silicon were below the secondary ion mass spectroscopy background of 5×10^{15} cm^{-3}. Wafer A exhibited significant "kink" in the knee region while wafer B showed almost no kink under dc conditions, as shown in Fig. 1. The 2 μm $\times$ 125 μm device fabrication on both wafers was identical with a source–drain spacing of 4 μm and a gate length of 0.25 μm. The entire experiment was repeated using a second pair of wafers with the same epitaxy and fabrication process resulting in the same measurement results reported here. More details on the epitaxy, drain current transient measurements, and on the kink effect mechanism are given in [24]. The higher background carbon profile of wafer A results in it having a floating p-type buffer leading to the kink and long-time constant recovery while wafer B has a n-type buffer which shows recovery in a few milliseconds.

A series of I–V measurements was performed under dc and pulsed conditions to study the carrier trapping and their effect on current collapse (knee walkout) and the kink effect. A Keithley source measurement system was used for dc measurements and current transients while a dynamic pulsed current–voltage analysis system (AU4850) was used for pulse measurements. The dc-I–V measurements were carried out for $V_{GS} = -3$–0 or $+1$ V (0.5-V step) and $V_{DS} = 0$–$+40$ V

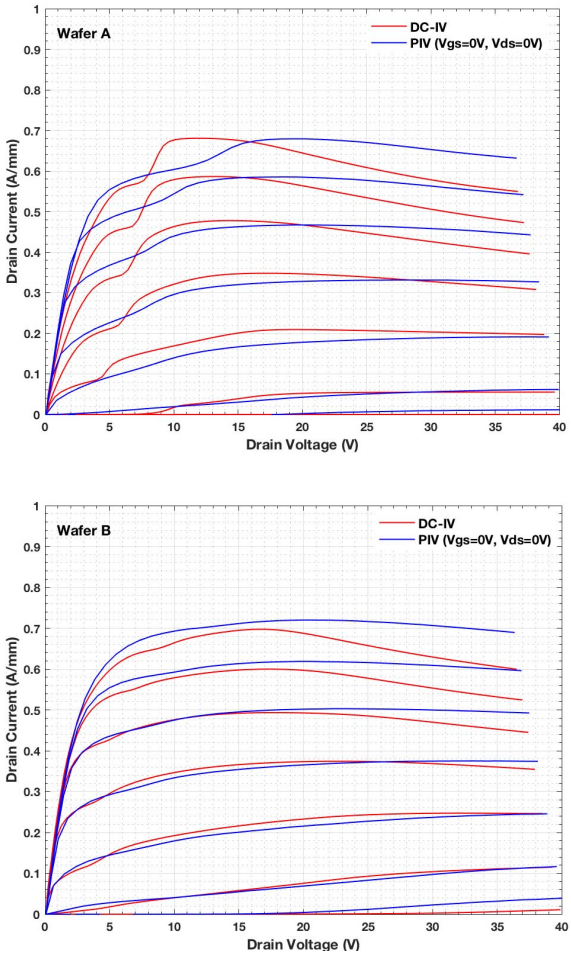

Fig. 1. Output characteristics of 2 μm $\times$ 125 μm device during dc sweep (red) and P-I–V ($V_{GSQ} = 0$ V and $V_{DSQ} = 0$ V) (blue), 1-μs pulse and 1-ms quiescent. $V_{GS} = -3$–0 V in 0.5-V steps.

(1-V step). In the case of the P-I–V measurement, a conventional simultaneous pulse (gate and drain lag) setup was adopted with soft switching. The device was held at a quiescent bias point, and the drain current versus the drain voltage curves were measured with short pulses (1 μs) and 1-ms quiescent bias. No significant difference was observed between 200-ns and 1-μs pulse lengths. The same V_{GS} sweep direction for all our dc and P-I–V measurements has been maintained. Advanced double-pulse approaches to measure the impact of trapping [25] could have been used but would only have accentuated the differences observed between the wafers.

Four quiescent bias points were used for this investigation as follows.

1) $V_{GSQ} = 0$ V and $V_{DSQ} = 0$ V designed to minimize trapping.
2) $V_{GSQ} = -6$ V and $V_{DSQ} = 0$ V designed to highlight trapping under the gate region (gate-lag effect).
3) $V_{GSQ} = -6$ V and $V_{DSQ} = 40$ V designed to highlight trapping under the gate–drain region (drain-lag effect), with no self-heating.
4) $V_{GSQ} = -1.7$ V and $V_{DSQ} = 10$–28 V designed to highlight trapping under class-B operation (emulation of saturated RF performance).

A large-signal RF-I–V waveform engineering system architecture based on a VTD SWAP-X402 receiver that was developed at Cardiff University [26], [27] has been used for the RF analysis in this paper. An integrated external modulator with high-speed RF switches (1 GHz) has been used to provide the RF pulsing unit, and a high-side FET switch is used to modulate the drain under dc when needed. The ability to independently switch the RF and dc drain bias between pulse and continuous wave without making any changes to the sampling regime delivers comparability between different measurement conditions; therefore, any measured changes can safely be ascribed to the device under test. A full range of common classes, such as A, B, AB, F, J, and continuous F, can be explored. In this paper, the devices are analyzed under class-B operational mode that delivers high power added efficiency (PAE). A resistive load is applied at the fundamental frequency with a short circuit at higher harmonics. The quiescent bias current is initially set to a low level, which rises as the RF drive is increased. The result is a nominally sinusoidal RF drain voltage, $v_{\mathrm{ds}}(t)$, waveform and a half-wave rectified RF drain current, $i_d(t)$, waveform that flows primarily when the voltage is at a minimum resulting in improved efficiency. These RF-I–V waveforms were measured over a range of fundamental load impedances and at five different dc drain bias points (10, 15, 20, 25, and 28 V) for five different devices on each wafer.

It is important to note that no irreversible degradation was observed in any of the measurements or as a result of bias conditions applied during the experiments. Hence, the differences in buffer doping did not lead to the degradation as has been observed previously [28].

III. Results and Discussion

A. Pulsed I–V

The presence of trapping can be identified from the analysis of the dc and pulsed I–V characteristics, starting from several quiescent bias points. Fig. 1 shows the output characteristics of both wafers under dc and pulsed measurements ($V_{\mathrm{GSQ}} = 0$ V and $V_{\mathrm{DSQ}} = 0$ V). It can be noticed that there was a fall in the dc-I–V curves at high I_D and V_{DS} for both wafers. This drop in the drain current is not trap related but can be associated with thermal effects. As already noted, wafer A showed significant kink, especially during the dc sweep with wafer B showing only a small kink. The kink behavior was strongest during slow dc sweeps (0.1 V/s) at drain voltages less than 10 V. On the other hand, when $V_{\mathrm{DS}} > 10$ V, the dc sweep both up and down showed the identical results, demonstrating that trapping/detrapping is strongly driven by the field. Gate leakage for both wafers was insignificant and $\sim$4 μA/mm at $V_{\mathrm{GS}} = -6$ V.

For wafer A, the P-I–V measurements (Fig. 2) showed an increase in ON-resistance from 4 to 6.25 Ω·mm when pulsed from ($V_{\mathrm{GSQ}} = 0$ V and $V_{\mathrm{DSQ}} = 0$ V) up to $V_{\mathrm{DS}} = 40$ V compared to pulsing only up to $V_{\mathrm{DS}} = 10$ V. This demonstrates that rapid trapping in acceptor traps was occurring on a timescale less than the 1-μs pulselength at the highest drain voltage. In contrast, wafer B showed no change in the current with respect

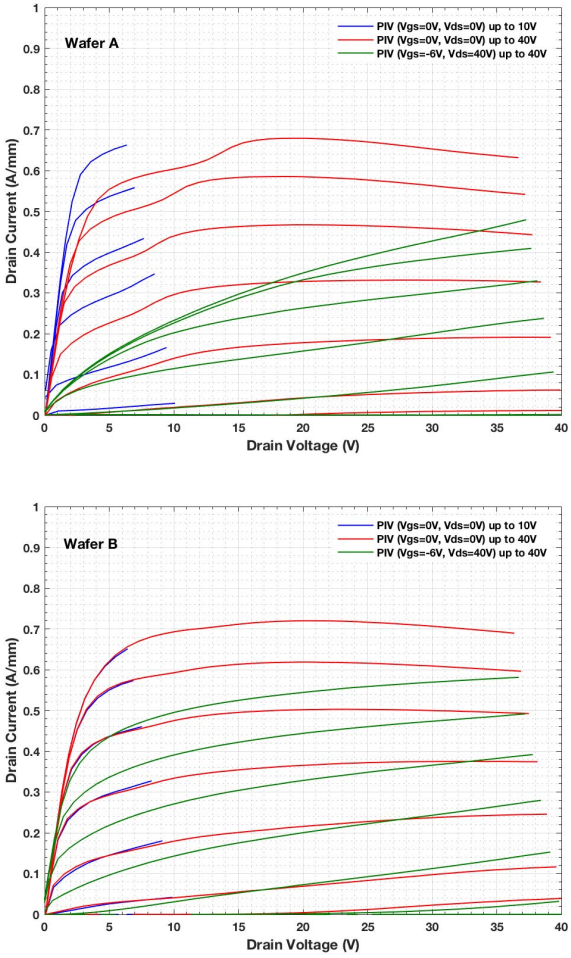

Fig. 2. Output characteristics of 2 μm $\times$ 125 μm device during P-I–V sweep ($V_{\mathrm{GSQ}} = 0$ V and $V_{\mathrm{DSQ}} = 0$ V) up to 10 V (blue), up to 40 V (red), and ($V_{\mathrm{GSQ}} = -6$ V and $V_{\mathrm{DSQ}} = 40$ V) up to 40 V (green) for both wafers. $V_{\mathrm{GS}} = -3$–0 V in 0.5-V steps.

to the drain stress during P-I–V sweep when the maximum pulse voltage changed between 10 and 40 V. This implies that for this wafer, trapping occurred on a timescale longer than 1 μs at 40 V. When comparing the devices pulsed to 40 V from ($V_{\mathrm{GSQ}} = 0$ V and $V_{\mathrm{DSQ}} = 0$ V) and ($V_{\mathrm{GSQ}} = -6$ V and $V_{\mathrm{DSQ}} = 0$ V) (gate lag), very little difference has been noticed with overlaid output curves for both wafers suggesting that the drain bias has the most prominent effect on the traps (not shown). In Fig. 2, the presence of knee walkout and current collapse under drain stress conditions in both wafers is clearly seen when biased at ($V_{\mathrm{GSQ}} = -6$ V and $V_{\mathrm{DSQ}} = 40$ V). However, the severity of this knee walkout and current collapse is much larger in wafer A than that observed for wafer B. Fig. 3 further confirms these observations when both wafers were biased under ($V_{\mathrm{GSQ}} = -1.7$ V and $V_{\mathrm{DSQ}} = 28$ V) in the emulation of the self-biased class-B operating point in saturation under RF. Wafer A again shows much stronger current collapse.

If the P-I–V data of Fig. 3 were used to extract the model coefficients for use in a nonlinear model modified to account for trapping [12]–[21], two different models would be generated, and the predicted RF performance of the wafers

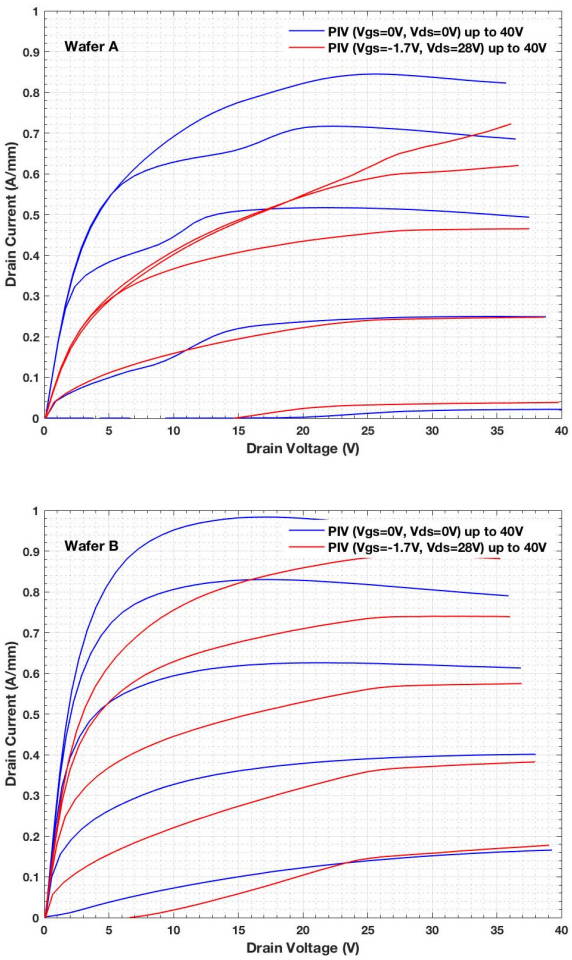

Fig. 3. Output characteristics of 2 μm $\times$ 125 μm device during P-I–V sweep ($V_{GSQ} = 0$ V and $V_{DSQ} = 0$ V) up to 40 V (blue) and ($V_{GSQ} = -1.7$ V and $V_{DSQ} = 28$ V) up to 40 V (red) for both wafers. $V_{GS} = -3$–$+1$ V in 1-V steps.

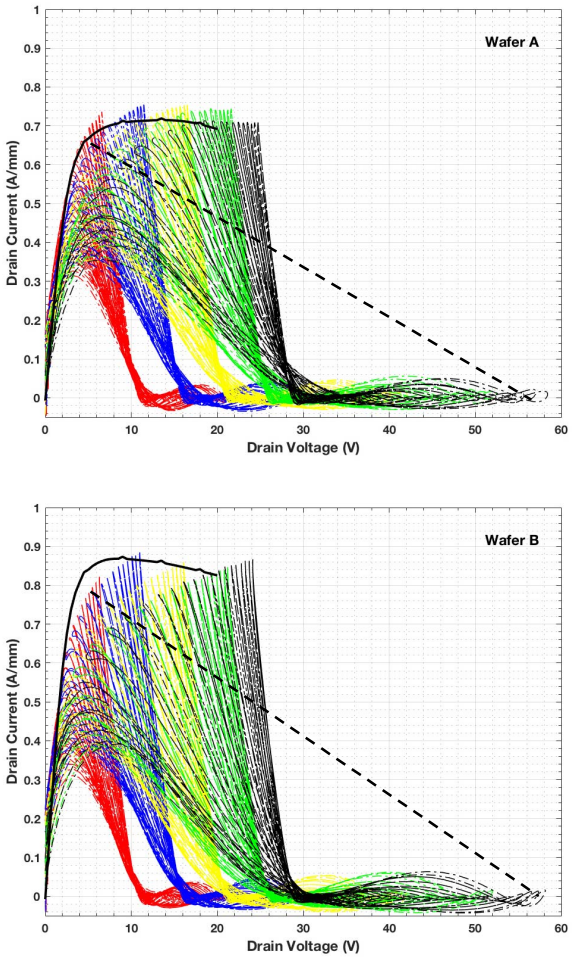

Fig. 4. RF-I–V fan diagrams of 2 μm $\times$ 125 μm at $V_{DS} = 10$ V (red), $V_{DS} = 15$ V (blue), $V_{DS} = 20$ V (yellow), $V_{DS} = 25$ V (green), and $V_{DS} = 28$ V (black), device identifying the RF knee walkout with increasing drain bias. Reference dc-I–V at $V_{GS} = +1$ V (black solid line).

would be very different. However, it will now be shown that the measured RF performance of these wafers is very similar and contradicts this expectation.

B. Large-Signal RF

To investigate the severity of the knee walkout and current collapse under RF conditions, the measured RF-I–V waveforms are transformed into RF dynamic load line plots, $i_d(t)$ plotted versus $v_{ds}(t)$. Here, the input gate voltage swings between $+1$ and -6 V corresponding to full saturation. These RF-I–V waveform measurements were performed at five different dc drain biases over a range of fundamental load impedances for the devices on both wafers, producing the results shown in Fig. 4 referred to as an "RF-I–V fan diagram" [29], [30]. The "RF-I–V fan diagrams" highlight that there is no dramatic difference between the two wafers in contrast to what was seen for P-I–V in Fig. 3. There is also no pinchoff or buffer leakage issue observable at high drain bias with either of the wafers. In Fig. 4, it can be noticed that the "knee" of the RF curves, high-current/low-voltage boundary observed in $i_d(t)$ versus $v_{ds}(t)$ plots, of each load impedance sweep softens and moves to the right with increasing dc drain bias voltage indicating that there is still a V_{DS} bias-dependent knee walkout. Table I summarizes the maximum output power and maximum PAE measured for both wafers for the same P_{IN} in saturation. The wafers show very comparable behavior, with the higher power shown by wafer B entirely explained by the higher maximum drain current measured under dc and is not attributable to any difference in trapping.

TABLE I
SUMMARY OF MEASURED P_max AND PAE_max. Δ_P AND δ_PAE ARE THE VARIATION RANGES BETWEEN THE MEASURED DEVICES

	P_max (dBm)	Δ_P (dBm)	PAE_max (%)	Δ_PAE (%)
Wafer (A)	35.56	0.43	68.5	2.28
Wafer (B)	36.23	0.89	75.25	3.78

To emulate the trapping state attained during the RF class-B operation but using a P-I–V measurement, the devices were

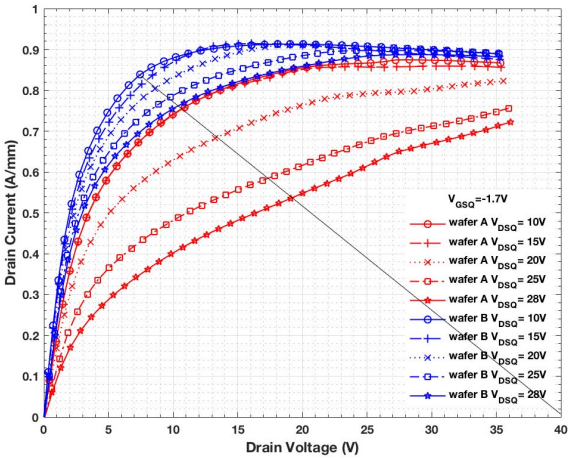

Fig. 5. Output characteristics of 2 μm $\times$ 125 μm device during P-*I–V* sweep at $V_{GS} = +1$ V ($V_{GSQ} = -1.7$ V and $V_{DSQ} = 10$, 15, 20, 25, and 28 V).

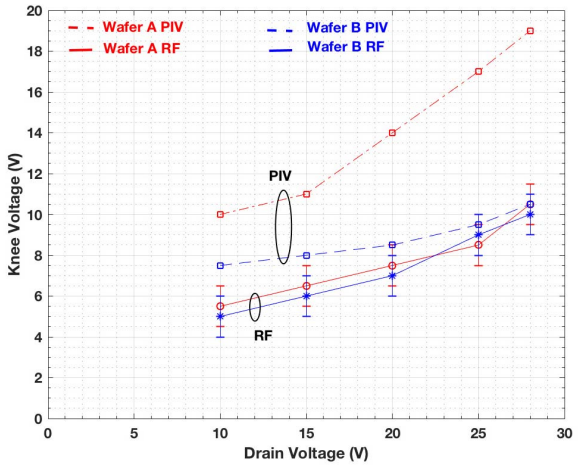

Fig. 6. Knee voltage as a function of drain bias point measured from dynamic RF load line measurements and P-*I–V* measurements ($V_{GSQ} = -1.7$ V and $V_{DSQ} = 10$, 15, 20, 25, and 28 V). Knee voltage is extracted using the load line shown in Figs. 4 and 5.

biased with $V_{GSQ} = -1.7$ V and $V_{DSQ} = 10$, 15, 20, 25, and 28 V. These quiescent points corresponded to the dc bias current (I_{DSQ}) that produced maximum output power in the RF measurement. Fig. 5 shows the $V_{GS} = +1$ V characteristics corresponding to the highest RF input voltage in Fig. 4. In Fig. 5, it is clearly evident that wafer A exhibits much larger knee walkout and current collapse than does wafer B with increasing drain bias, extending the observation shown in Fig. 3 to a wider range of operating conditions.

Fig. 6 shows the plot of the knee voltage against the drain bias voltage. There is no agreed definition of knee voltage, so here the knee voltage for the P-*I–V* data is extracted along the load line presented in Fig. 5, while the knee voltage for the RF-*I–V* data is extracted along the same load line as presented in Fig. 4. It is observed that both wafers (under RF conditions) show very similar knee walkout effect with increasing dc drain bias voltage in clear contradiction to the observations made under P-*I–V* where wafer A showed much more severe knee walkout than did wafer B.

The key difference between these wafers may perhaps best be identified in Fig. 2. Wafer A showed rapid trapping on a timescale shorter than the typically used from 100-ns to 1-μs pulselength and that led to a strongly distorted P-*I–V* characteristic. This was then unrepresentative of the 1-GHz RF-*I–V* waveform which presumably had a characteristic timescale much shorter than the trapping time although this has not been confirmed experimentally. By contrast P-*I–V* measurements on wafer B accurately represented the RF-*I–V* waveforms because both measurements involved dynamic changes that are faster than the trapping time.

IV. Conclusion

Two HFET wafers with different growth characteristics resulted in quite distinct dc and pulsed *I–V* behavior. Only one showed a kink effect and also showed much stronger knee walkout in pulsed *I–V*. The conventional interpretation of this behavior would suggest a dramatic difference in the RF performance. However, large-signal RF measurements showed no significant difference in output power or efficiency between the wafers. Hence, while pulsed *I–V* measurements can be a very useful tool for identifying charge trapping, it can fall short in predicting the impact of traps under RF conditions.

The great caution must be taken when utilizing pulsed *I–V* measurements to extract the RF device model coefficients aimed at including trapping effects in GaN-based HFETs. While it may well be possible to formulate a pulsed *I–V* measurement regime which correctly predicts the RF performance, this is likely to vary with process changes. Thus, appropriate large-signal RF-*I–V* waveform measurements are an essential additional requirement, if one is to develop robust nonlinear RF device models that include traps.

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Hassan Hirshy (M'15) received the Ph.D. degree from Cardiff University, Cardiff, U.K.

He was a Research Associate and the Project Manager with the Manufacturing Engineering Centre, Cardiff University, where he was involved in micro- and nanofabrication. He is currently a Research Fellow with the Centre for High Frequency Engineering. He is involved in device technology development and circuit design of III–V radio frequency devices.

Manikant Singh (M'18) is currently pursuing the Ph.D. degree in physics with the Centre for Device Thermography and Reliability, University of Bristol, Bristol, U.K.

His current research interests include the characterization and reliability of gallium nitride devices.

Michael A. Casbon (M'13) was a Waveguide Engineer in Cambridge, U.K., initially designing TV broadcast channel diplexers and vision/sound combiners, and subsequently designed the first 1-KW band 4/5 broadband module for what became the Harris–Sceptre solid-state TV transmitter range. He became the Chief Engineer with Wessex Electronics, Bristol, U.K. He is currently a Researcher with Cardiff University, Cardiff, U.K., where he is involved in active harmonic load–pull techniques to characterize the semiconductor devices.

Richard M. Perks received the B.Sc. and Ph.D. degrees from Swansea University, Swansea, U.K., in 1993 and 1997, respectively.

He was a Senior Scientist with BAE Systems till 1999 when he moved to Cardiff University. He is currently a Senior Lecturer with the School of Engineering, Cardiff University, Cardiff, U.K. He has published research in diverse fields ranging from oncology-to-semiconductor growth.

Michael J. Uren (M'06) received the M.A. and Ph.D. degrees in physics from the University of Cambridge, Cambridge, U.K. He was with RSRE, DERA, and QinetiQ, where he was involved in Si, SiC, and gallium nitride devices. He is currently a Research Professor with the University of Bristol, Bristol, U.K. He is also a fellow of the Institute of Physics.

Trevor Martin received the Ph.D. degree from the University of Glasgow, Glasgow, U.K., with a focus on molecular beam epitaxy growth on InP.

He was with QinetiQ and its predecessor RSRE, where he was responsible for the compound semiconductor epitaxy activities including the development of gallium nitride (GaN). He is currently the Director of global GaN strategy with IQE, Cardiff, U.K.

Martin Kuball (SM'09) received the Ph.D. degree from the Max Planck Institute for Solid State Research, Stuttgart, Germany.

He was the Feodor-Lynen Post-Doctoral Fellow with Brown University, Providence, RI, USA. He is currently a Professor of physics and the Director of the Center for Device Thermography and Reliability, University of Bristol, Bristol, U.K. He is also a fellow of IoP.

Dr. Kuball is a fellow of the IET, and SPIE.

Paul J. Tasker (F'15) received the B.Sc. and Ph.D. degrees from Leeds University, Leeds, U.K., in 1979 and 1983, respectively.

From 1984 to 1990, he was a Research Associate with L. Eastman at Cornell University, Ithaca, NY, USA. From 1990 to 1995, he was a Senior Manager with the Fraunhofer Institute for Applied Solid State Physics, Freiburg im Breisgau, Germany. In 1995, he joined Cardiff University, Cardiff, U.K., as a Professor.