All CVD Boron Nitride Encapsulated Graphene FETs With CMOS Compatible Metal Edge Contacts

Himadri Pandey, *Member, IEEE*, Mehrdad Shaygan, Simon Sawallich, Satender Kataria, Zhenxing Wang, Achim Noculak, Martin Otto, Michael Nagel, Renato Negra, Daniel Neumaier, and Max C. Lemme, *Senior Member, IEEE*

(Invited Paper)

***Abstract*— We report on the fabrication and characterization of field-effect transistors (FETs) based on chemical vapor deposited (CVD) graphene encapsulated between few layer CVD boron nitride (BN) sheets with complementary metal–oxide–semiconductor (CMOS) compatible nickel edge contacts. Noncontact terahertz time-domain spectroscopy (THz-TDS) of large-area BN/graphene/BN (BN/G/BN) stacks reveals average sheet conductivity >1 mS/sq. and average mobility of 2500 $cm^2/V \cdot s$. Improved output conductance is observed in dc measurements under ambient conditions, indicating the potential for radio frequency (RF) applications. Moreover, we report a maximum voltage gain of 6 dB from a low-frequency signal amplifier circuit. RF characterization of the GFETs yields an $f_T \times L_g$ product of 2.64 GHz $\cdot \mu$m and an $f_{Max} \times L_g$ product of 5.88 GHz $\cdot \mu$m. This paper presents for the first time THz-TDS usage in combination with other characterization methods for device performance assessment on BN/G/BN stacks. The results serve as a step toward scalable, all CVD 2-D material-based FETs for CMOS compatible future nanoelectronic circuit architectures.**

***Index Terms*— Boron nitride (BN), chemical vapor deposition (CVD), edge contacts, graphene, intrinsic voltage gain, mobility, radio frequency (RF), terahertz (THz), voltage amplifier.**

I. Introduction

SINGLE layer graphene, first reported experimentally more than a decade ago [1], [2], has been a fast emerging electronic material with large room temperature low-field carrier mobility [3]. Chemical vapor deposited (CVD) graphene is large area variant of this material, which has been shown to be useful for highly scalable devices [4]–[6]. Several applications have been suggested, demonstrated, and reported in the literature based on exfoliated, CVD as well as epitaxial graphene layers on various substrates in recent years. These include field-effect transistors (FETs) [7]–[9], inverters [10]–[14], microwave/radio frequency (RF) transistors [7], [15]–[19], various circuit applications [15], [20], [21] pressure sensors [22], [23], gas sensors [24], [25], and many more. The importance of the substrate for graphene mobility and—as a consequence—for graphene transistor performance has been outlined both through theoretical [26] as well as experimental studies [27]–[30]. Hexagonal boron nitride (hBN) has been identified by various authors as an ideal substrate for preserving nearly intrinsic, high mobility values in graphene. This has been attributed to the atomically flat surface of hBN, as well as minimal lattice mismatch with graphene [8], [28], [31]–[34]. In addition, poor current saturation in the output characteristics (source–drain current I_{DS} versus source–drain voltage V_{DS}) of single layer GFETs is a well-known bottleneck that results in poor voltage gain and limits f_{Max} performance [35]. Good current saturation, i.e., lower g_{ds}, improves this situation, and is thus the desired quantity [36], [37]. For this, exfoliated hBN encapsulated monolayer graphene devices with strongly quasi-saturating output characteristics have been suggested in [8]. However, most of these studies have utilized mechanically exfoliated hBN crystals for device fabrication, which limits its applicability as a scalable technology. Nonetheless, there have also been some attempts to grow large area hBN sheets using CVD techniques [38]. However, to the best of our knowledge, there have been no reports of CVD BN encapsulated CVD graphene (BN/G/BN) RF FETs in the literature till date. In this paper, we report on the fabrication of such devices with complementary metal–oxide–semiconductor (CMOS) compatible metal edge contacts to the graphene channel, and present comprehensive characterization data of the all CVD BN/G/BN FETs including dc, RF as well as terahertz time-domain spectroscopy (THz-TDS) methods. This paper is also the first one to our knowledge where THz-TDS mapping has been

Manuscript received April 26, 2018; revised July 19, 2018; accepted August 5, 2018. Date of publication September 5, 2018; date of current version September 20, 2018. This work was supported in part by the German Research Foundation under Grant DFG LE 2440/2-1 and Grant LE 2440/3-1 and in part by the EU Graphene Flagship under Grant 785219. The review of this paper was arranged by Editor F. Schwierz. *(Corresponding author: Max C. Lemme.)*

H. Pandey and S. Kataria are with the Chair of Electronic Devices, RWTH Aachen University, 52074 Aachen, Germany.

M. Shaygan, Z. Wang, M. Otto, and D. Neumaier are with the Advanced Microelectronic Center Aachen, AMO GmbH, 52074 Aachen, Germany.

S. Sawallich and M. Nagel are with Protemics GmbH, 52074 Aachen, Germany.

A. Noculak and R. Negra are with the Chair of High Frequency Electronics, RWTH Aachen University, 52074 Aachen, Germany.

M. C. Lemme is with the Chair of Electronic Devices, RWTH Aachen University, 52074 Aachen, Germany, and also with the Advanced Microelectronic Center Aachen, AMO GmbH, 52074 Aachen, Germany (e-mail: lemme@amo.de).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2018.2865382

directly used for assessing mobility in such all CVD BN/G/BN stacks. The transistors show an I_{ON}/I_{OFF} current ratio of ~6, mobility values ranging from 1000 to 5000 $cm^2/V \cdot s$, extracted contact and sheet resistance values of ~2 $k\Omega \cdot \mu m$ and ~750 Ω/sq., respectively, and quasi-saturating output characteristics. The low dc output conductance values observed in these devices are found to be lower than the conventional monolayer graphene on SiO_2 FETs, and are comparable to artificially stacked bilayer graphene (ASBLG) FETs, which have been recently proposed as an improvement over monolayer GFETs for obtaining enhanced intrinsic voltage gain performance [36]. These aspects are cumulatively exploited in demonstrating a voltage amplifier circuit application based on these GFETs which yield a voltage gain of up to ~6 dB in a resistive load scheme. RF characterization of the devices yields decent values of 2.64 GHz $\cdot \mu$m for $f_T \times L_g$ product and of 5.88 GHz $\cdot \mu$m for $f_{Max} \times L_g$ product. The highest intrinsic voltage gain of an individual transistor was measured to be 7.76.

II. Experiment

CVD graphene monolayer (grown on Cu) was obtained from Graphenea and large area CVD grown BN was obtained from Graphene Supermarket. The materials were removed from copper using a wet etch-based transfer technique and a BN/G/BN stack was fabricated by transfer onto a 1 μm thick thermally grown SiO_2 on p-doped Si substrate (Si resistivity ~1–5 $\Omega \cdot$ cm). Optical lithography was used to pattern device channels from this material stack, using ($CHF_3 + O_2$) plasma-based reactive-ion etching. This presented us with the possibility of forming edge contacts to the encapsulated graphene sheet from the sides, as the graphene is covered under the BN sheet from the top and the bottom. Source–drain contacts were then defined using optical lithography and formed using the CMOS compatible metal nickel (Ni) deposited through sputtering, followed by a liftoff process. Sputtering was preferred over evaporation because it provides isotropic metal coverage, thus facilitating the formation of edge contacts to the encapsulated graphene sheet. Ni has been demonstrated experimentally to have the largest work function difference to graphene, resulting in lower graphene–metal contact resistivity [39]. Therefore, Ni was chosen for forming edge contacts to graphene in these devices. More detailed discussions on these edge contacts have been reported elsewhere [40]. The advantage of using such edge-contacted graphene over regularly reported area-contacted graphene is that the former shows improved contact resistivity, thus leading to improved device performance in transistor configuration [40], [41]. On the top of the BN, a second top-gate dielectric of 20 nm of Al_2O_3 was deposited using atomic layer deposition (ALD) in an Oxford ALD reactor using a water vapor-based cyclic process. Trimethylaluminum was used as precursor. Nucleation was facilitated through a 2-nm-thick oxidized aluminum (Al) seed layer. Finally, top-gate fingers were fabricated using optical lithography, e-beam evaporation of 100-nm-thick Al and a liftoff process in acetone. Fig. 1(a) shows a simple schematic of such an all-CVD BN encapsulated GFET device. A color-enhanced scanning electron micrograph (SEM) of a typical finished device in RF compatible coplanar waveguide (CPW) layout with ground–signal–ground (GSG) pads is shown in Fig. 1(b). An atomic force micrograph (AFM) shows a stack thickness of approximately 16 nm [Fig. 2(a)]. This allows estimating the CVD BN thickness to be ~7–8 nm on each side of the monolayer graphene (~0.35 nm thick). A roughness map of the stack shows that the root-mean-square surface roughness was 3.1 nm [Fig. 2(b)]. On device Raman spectroscopy was used to characterize the quality of the stack to make sure that no damage occurred to the encapsulated graphene during the processing. Fig. 2(c) shows a single Raman spectrum acquired in the channel region with clear and sharp G and 2-D peaks. The monolayer nature of graphene is confirmed by a 2-D/G intensity ratio >1 [6], [42]. No significant D peak, related to the presence of defects in graphene [43], was observed indicating low damage to graphene from transfer and encapsulation during the stack fabrication process. No typical hBN peak at ~1370 cm^{-1} [44] could be observed in these spectra, suggesting an amorphous nature of the CVD grown BN. The uniformity of the channel regions was further confirmed by

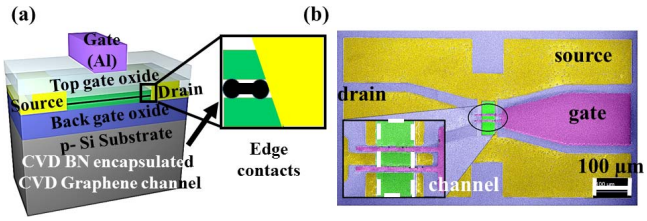

Fig. 1. (a) Device schematic of the all-CVD BN encapsulated GFET with CMOS compatible metal edge contacts. The contact metal is sputtered nickel while the top-gate metal is evaporated aluminum. (b) SEM (color enhanced) of a device in CPW layout, where the gate, source and drain terminals are highlighted. Inset: zoomed-in view of the channel region (BN/G/BN stack). Everything except the top-gate fingers is embedded under the top-gate dielectric film.

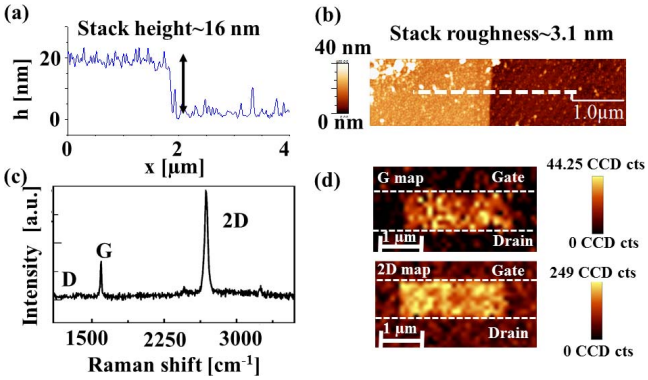

Fig. 2. (a) AFM scan of the CVD BN/G/BN stack showing a stack height of approximately ~16 nm. This indicates the presence of 7–8-nm-thick BN on both sides of the monolayer graphene (thickness ~0.35 nm). (b) Roughness map of the stack revealed a root-mean-square roughness value of 3.1 nm, measured along the white dotted line. (c) Typical Raman spectra (laser wavelength ~532 nm) of the stack. Characteristic G and 2-D peaks of the encapsulated graphene monolayer are clearly seen while the D peak, which denotes defects, was found to be negligibly small. (d) Uniform G and 2-D maps obtained on the sample are also shown. Both these observations suggest no damage to the graphene sheet during encapsulation between the CVD BN layers. No typical hBN peak around ~1370 cm^{-1} was observed in the Raman spectra, indicating a rather amorphous film.

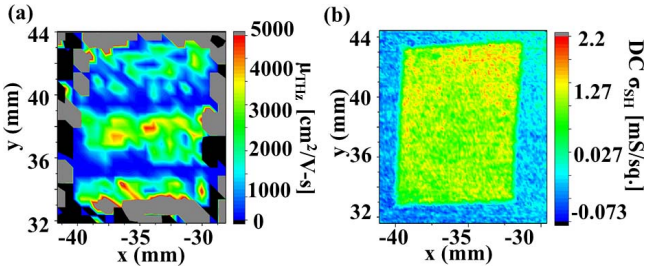

Fig. 3. (a) Spatially resolved mobility map of the all CVD BN/G/BN stack obtained from noncontact THz near-field spectroscopy indicating 1000 $cm^2/V \cdot s \leq \mu_{THz} \leq 5000\ cm^2/V \cdot s$. A median value of $\mu_{THz} \sim 1500\ cm^2/V \cdot s$ and an average of $\mu_{THz} \sim 2500\ cm^2/V \cdot s$ was observed over the whole stack. (b) Sheet conductivity map of the stack shows the average $\sigma_{SH} \geq 1$ mS/sq. for the encapsulated graphene sheet.

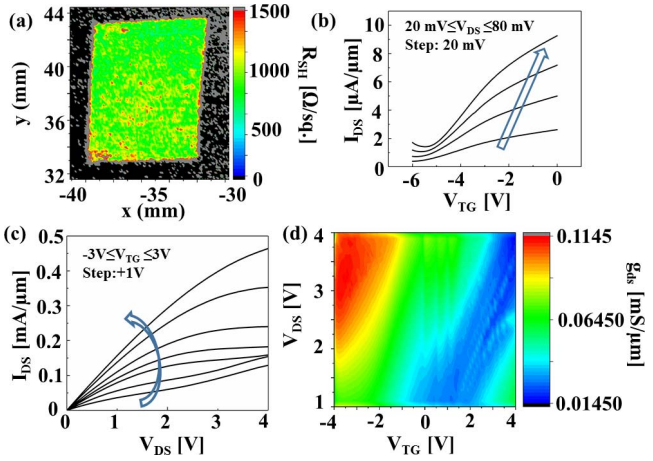

Fig. 4. (a) Extracted sheet resistance (R_{SH}) map of the CVD BN/G/BN stack. Average R_{SH} values of $\sim$750 Ω/sq. were observed in the sample. (b) Transfer characteristics of a BN/G/BN FET with a gate length of $L_G = 10\ \mu$m and a channel width of $W = 30\ \mu$m. The devices in general were observed to be n-doped. The arrow provides a guide to the eye in the direction of successively increasing V_{DS} values. (c) Output characteristics with clear saturation of the device shown in (b). The direction of successively increasing applied V_{TG} from -3 to $+3$ V in a step of $+1$ V is indicated by the arrow. (d) Output conductance (g_{ds}) map of the same device reveals improved minimum $g_{ds} \sim 0.01450$ mS/μm, which is lower compared to non-BN encapsulated monolayer GFETs. We note that this value is comparable to minimum g_{ds} values observed in ASBLG FETs [36].

Raman area scans which yielded uniform G and 2-D peak intensities over the entire channel, as shown in Fig. 2(d).

III. Results and Discussion

Prior to device fabrication, the whole CVD BN/G/BN stack was characterized using a THz-TDS setup equipped with microprobe detectors for high-resolution THz near-field imaging [45]. A THz plane wave is generated below the sample, transmitted through it and detected by a near-field detector that can be scanned at a small distance above the sample surface. Fig. 3(a) shows the THz mobility (μ_{THz}) map of the stack, with values ranging from 1000 to 5000 $cm^2/V \cdot s$. It should be noted that μ_{THz} describes the electron mobility values assessed using THz-TDS. A variation in THz (electron) mobility values between 1000 and 5000 $cm^2/V \cdot s$ suggested that device variability may be significant. The median of the μ_{THz} values was $\sim$1500 $cm^2/V \cdot s$, while the average μ_{THz} was $\sim$2500 $cm^2/V \cdot s$. The THz mobility map has a lateral scanning step size of 500 μm. At each pixel, we recorded a full THz transient and obtained the spectrally resolved THz transmission amplitude of the BN/G/BN stack via fast Fourier transformation. From this data, the frequency-dependent graphene conductivity has been calculated, and the mobility has been extracted by a Drude model fit to the real part of the conductivity [46]. The details of THz-TDS-based mobility extraction method for various environments have been already reported extensively in [46]–[48]. The large variation in μ_{THz} observed here may be attributed to variations in the fit of the measured (real) conductivity data with the Drude model. Fig. 3(b) shows the (quasi-dc) sheet conductivity (σ_{SH}) map of the BN/G/BN stack extracted from a measurement of the THz transmission amplitude with a spatial resolution of 100 μm. The sheet conductivity and the sheet resistance ($R_{SH} = 1/\sigma_{SH}$) of the material are calculated from the ratio of the THz amplitude transmitted through the sample stack area to the substrate-only transmission amplitude using Tinkham's formula [49]. We measured quite high average values of $\sigma_{SH} \geq 1$ mS/sq. for the BN/G/BN stack. A corresponding R_{SH} value of $\sim$750 Ω/sq. was extracted over the scan area of the sample, as shown in Fig. 4(a). In contrast to the mobility extraction, which requires full THz spectra, the sheet resistance/conductivity calculation requires only the THz amplitude. Therefore, the latter can be acquired significantly faster (or with a higher resolution in a fraction of the measurement time).

All reported dc characterization was carried out under ambient conditions in a Cascade Summit 12 000 probe station connected to an HP 4155B semiconductor parameter analyzer. As shown in Fig. 4(b), transfer characteristics (source–drain current, I_{DS} versus top-gate voltage V_{TG}) as a function of successively increasing source–drain bias (V_{DS}) measured on a GFET revealed a rather highly n-doped device: the Dirac point was observed to be located at around $V_{TG} = -5$ V. The device gate length and channel width were $L_G = 10\ \mu$m and $W = 30\ \mu$m, respectively. Such n-type doping was observed for all devices. Strongly saturating output characteristics (I_{DS} versus V_{DS}) as a function of successively increasing applied V_{TG} of the same device are shown in Fig. 4(c). Again, similar behavior was obtained for several devices, suggesting good gate control over the channel. It should be noted that the back gate voltage was $V_{BG} = 0$ V in all these data. This has been deliberately chosen to assess the RF performance potential of these devices, as will be discussed in the later part of this section. Low-field carrier mobility values were extracted from transfer characteristics measured on several devices by fitting to a variable resistor GFET model reported in [50]. The best fit to the transfer curve data obtained for a device with ($L_G = 10\ \mu$m and $W = 20\ \mu$m) at $V_{DS} = 10$ mV and $V_{BG} = 0$ V resulted in maximum electron mobility of $\mu_e \sim 3500\ cm^2/V \cdot s$, maximum hole mobility $\mu_h \sim 2500\ cm^2/V \cdot s$ and contact resistance values of $\sim 2\ k\Omega \cdot \mu m$, respectively. The mobility values are in line with the μ_{THz} values derived from the BN/G/BN stack prior to device fabrication. The slightly lower values obtained from contact mode (field effect) mobility compared to noncontact mode mobility (μ_{THz}) can

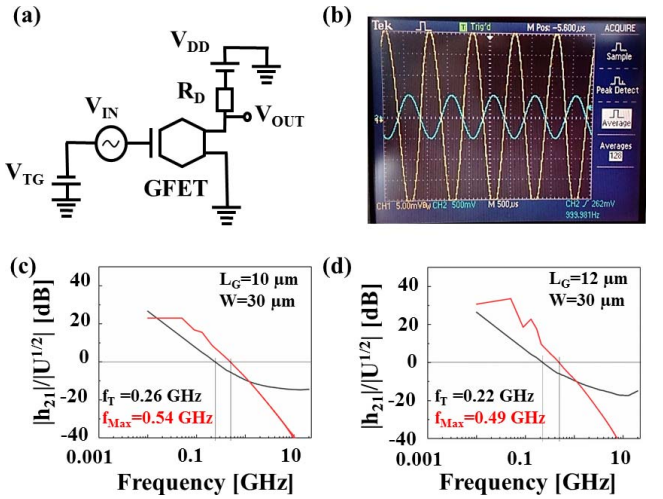

Fig. 5. (a) Schematic of a low frequency voltage signal amplifier circuit with resistive load scheme used to assess the voltage gain performance of the GFETs. A load resistance (R_D) of 10 kΩ was mounted on the drain end. (b) Screenshot of oscilloscope showing the highest measured voltage gain of ~6 dB at 1 kHz for a device with L_G = 10 μm and W = 10 μm. The applied signal is shown in blue while the amplified output signal is shown in yellow on the screen. The ac input voltage was 20 mV_{PP}, and the measured output voltage was 40 mV_{PP}. (c) Highest f_T ~ 0.26 GHz and f_{Max} ~ 0.54 GHz values measured for the device shown in Fig. 4 with L_G = 10 μm and W = 30 μm. (d) Highest f_{Max}/f_T ratio of ~2.21 measured on another device with L_G = 12 μm and W = 30 μm indicating the effect of lower minimum output conductance values on RF device performance in these devices.

be explained by considering the effects of finite contact resistance and additional fabrication process steps carried out after the THz measurements. This possibility of device variability pointed out during THz-TDS also reflected in fabricated devices, where extracted (low field, electron) mobility values were observed to vary between ~600 and 2500 cm^2/V · s. Fig. 4(d) shows a detailed dc data map (g_{ds} versus V_{DS} and V_{TG}) of a GFET with L_G = 10 μm and W = 30 μm, which allows choosing an optimized operating point for RF measurements. The minimum output conductance (g_{ds}) is ~0.01450 mS/μm. We note that this is an improvement over the minimum g_{ds} values reported for monolayer GFETs fabricated on conventional SiO_2/Si substrates in [37], where 0.02 mS/μm $\leq$ g_{ds} $\leq$ 0.05 mS/μm. The study in [37] was carried out using exfoliated monolayer graphene, which is monocrystalline, unlike CVD graphene used in this paper. We also note that this value is comparable to the minimum g_{ds} values observed in ASBLG FETs, which have been recently proposed as an improvement over the conventional monolayer GFET for obtaining enhanced intrinsic voltage gain [36]. The highest dc transconductance measured in BN/G/BN devices was 538 μS/μm. The highest measured intrinsic voltage gain ($g_{m,max}/g_{d,min}$) in these devices was 7.76. It is important to note that the improved current saturation tendency and good voltage gain performance in all CVD GFETs is observed despite of the presence of a large series resistance due to 3 μm access regions on both sides of the gate.

Furthermore, the BN/G/BN FETs were also tested for low-frequency amplifier circuit applications. Fig. 5(a) shows a simple schematic of a low-frequency amplifier circuit in resistive load scheme, which was used to assess the extrinsic voltage gain performance of these devices. Several devices were measured with 1-kHz input frequency signal applied to the gate with a resistive load of 10-kΩ mounted at the drain end. Fig. 5(b) shows a photograph of the high impedance oscilloscope used to monitor the output voltage. The highest measured voltage gain of ~6 dB was observed for a device with L_G = 10 μm and W = 10 μm, when the applied ac input voltage was 20 mV_{PP} while the measured output voltage was 40 mV_{PP}. This result demonstrates the potential capability of these all-CVD BN/G/BN FETs to be employed in circuit applications.

These devices were further tested for RF performance potential. Devices were characterized in a bandwidth of 10 MHz–25 GHz using calibrated Rhode & Schwarz ZVA 50 Vector Network Analyzer connected to a compatible probe station. Calibration was performed using a standard substrate provided by the manufacturer using the short–open–load–through method and two-port S-parameter measurements were performed using on-wafer GSG probes. The highest (extrinsic) maximum oscillation frequency f_{Max} of ~0.54 GHz and the highest (extrinsic) cutoff frequency f_T of ~0.26 GHz for a device with L_G = 10 μm and W = 30 μm was observed at V_{TG} = 1 V and V_{DS} = 4 V [Fig. 5(c)]. The highest f_{Max}/f_T ratio was ~2.21 for a device with L_G = 12 μm and W = 30 μm at V_{TG} = 0 V and V_{DS} = 4 V [Fig. 5(d)]. The average value of f_{Max}/f_T ratio in these devices was approximately 2. The state-of-the-art f_{Max}/f_T ratio of 3.2 has been demonstrated for similar micrometer-sized devices with access region length of ~100 nm [51], thus minimizing the effect of parasitic access resistance. We have compared our edge-contacted RF GFET devices with top-contacted RF GFET devices reported in the literature for benchmarking, as it was the only available data for devices having comparable device dimensions. Nonetheless, the improved f_{Max}/f_T ratio reflected in the high-frequency behavior and good low-frequency amplifier gain of these all CVD BN/G/BN devices are attributed to the low dc output conductance values observed in these devices [Fig. 4(d)]. The highest $f_T \times L_G$ product, which reflects the speed of the GFET, was 2.64 GHz · μm. The highest $f_{Max} \times L_g$ product observed in these devices was 5.88 GHz · μm. The RF figures of merit of these proof of concept, all CVD BN/G/BN FETs are promising given that the long transistor channel lengths are used. Therefore, these devices offer good scope for the future research. We also note that although the devices shown here are equipped with CMOS compatible metal (Ni) edge contacts to graphene, nevertheless, all the device fabrication steps needed for GFETs may or may not always be completely CMOS compatible. Some process steps used here such as CVD qualify for back-end-of-line CMOS processes.

IV. Conclusion

In this paper, we report large area all CVD BN/G/BN FETs with CMOS compatible metal (Ni) edge contacts. Devices have been characterized in ambient at room temperature. The device potential of such encapsulated graphene sheets has been assessed by contact (dc, RF, and low-frequency circuit) as well as noncontact (THz spectroscopy) methodologies. THz-TDS mapping has been used for the first time on an all CVD BN/G/BN stack. Both methodologies suggest mobility values

between 1000 and 5000 $cm^2/V \cdot s$ in the BN encapsulated graphene. Good contact and sheet resistance values of around 2 $k\Omega \cdot \mu m$ and ~750 Ω/sq. have been extracted from these measurements. The all CVD BN/G/BN FETs yield good intrinsic voltage gain, good low-frequency amplifier voltage gain as well as decent RF performance figures of merit. The complete set of dc, low-frequency circuit performance as well as RF data in these devices is quite promising for future optimization. The devices demonstrate the potential for scalable, CMOS compatible all CVD BN/G/BN FETs for future device and circuit applications.

REFERENCES

[1] K. S. Novoselov *et al.*, "Electric field effect in atomically thin carbon films," *Science*, vol. 306, no. 5696, pp. 666–669, 2004.

[2] M. C. Lemme, T. J. Echtermeyer, M. Baus, and H. Kurz, "A graphene field-effect device," *IEEE Electron Device Lett.*, vol. 28, no. 4, pp. 282–284, Apr. 2007.

[3] K. I. Bolotin *et al.*, "Ultrahigh electron mobility in suspended graphene," *Solid State Commun.*, vol. 146, pp. 351–355, Jun. 2008.

[4] K. S. Kim *et al.*, "Large-scale pattern growth of graphene films for stretchable transparent electrodes," *Nature*, vol. 457, no. 7230, pp. 706–710, Feb. 2009.

[5] A. Reina *et al.*, "Growth of large-area single- and Bi-layer graphene by controlled carbon precipitation on polycrystalline Ni surfaces," *Nano Res.*, vol. 2, no. 6, pp. 509–516, Jun. 2009.

[6] S. Kataria *et al.*, "Chemical vapor deposited graphene: From synthesis to applications," *Phys. Status Solidi A*, vol. 211, no. 11, pp. 2439–2449, Nov. 2014.

[7] I. Meric, N. Baklitskaya, P. Kim, and K. L. Shepard, "RF performance of top-gated, zero-bandgap graphene field-effect transistors," in *IEDM Tech. Dig.*, Dec. 2008, pp. 1–4.

[8] I. Meric, C. Dean, A. Young, J. Hone, P. Kim, and K. L. Shepard, "Graphene field-effect transistors based on boron nitride gate dielectrics," in *IEDM Tech. Dig.*, Dec. 2010, pp. 23.2.1–23.2.4.

[9] I. Meric *et al.*, "Channel length scaling in graphene field-effect transistors studied with pulsed current-voltage measurements," *Nano Lett.*, vol. 11, no. 3, pp. 1093–1097, Jan. 2011.

[10] S.-L. Li, H. Miyazaki, A. Kumatani, A. Kanda, and K. Tsukagoshi, "Low operating bias and matched input-output characteristics in graphene logic inverters," *Nano Lett.*, vol. 10, no. 7, pp. 2357–2362, Jun. 2010.

[11] H.-Y. Chen and J. Appenzeller, "Complementary-type graphene inverters operating at room-temperature," in *Proc. 69th Device Res. Conf.*, Jun. 2011, pp. 33–34.

[12] L. G. Rizzi *et al.*, "Cascading wafer-scale integrated graphene complementary inverters under ambient conditions," *Nano Lett.*, vol. 12, no. 8, pp. 3948–3953, Jul. 2012.

[13] D. Schall, M. Otto, D. Neumaier, and H. Kurz, "Integrated ring oscillators based on high-performance graphene inverters," *Sci. Rep.*, vol. 3, Sep. 2013, Art. no. 2592.

[14] H. Pandey, S. Kataria, A. Gahoi, and M. C. Lemme, "High voltage gain inverters from artificially stacked bilayer CVD graphene FETs," *IEEE Electron Device Lett.*, vol. 38, no. 12, pp. 1747–1750, Dec. 2017.

[15] H. Wang, A. Hsu, J. Wu, J. Kong, and T. Palacios, "Graphene-based ambipolar RF mixers," *IEEE Electron Device Lett.*, vol. 31, no. 9, pp. 906–908, Jul. 2010.

[16] A. Hsu, H. Wang, K. K. Kim, J. Kong, and T. Palacios, "High frequency performance of graphene transistors grown by chemical vapor deposition for mixed signal applications," *Jpn. J. Appl. Phys.*, vol. 50, no. 7R, p. 070114, Jul. 2011.

[17] S.-J. Han, A. V. Garcia, S. Oida, K. A. Jenkins, and W. Haensch, "High-performance multi-stage graphene RF receiver integrated circuit," Presented at the IEDM Tech. Dig., Dec. 2013, pp. 19.9.1–19.9.3.

[18] S. Rahimi *et al.*, "Toward 300 mm wafer-scalable high-performance polycrystalline chemical vapor deposited graphene transistors," *ACS Nano*, vol. 8, no. 10, pp. 10471–10479, Oct. 2014.

[19] S.-J. Han, A. V. Garcia, S. Oida, K. A. Jenkins, and W. Haensch, "Graphene radio frequency receiver integrated circuit," *Nature Commun.*, vol. 5, Jan. 2014, Art. no. 3086.

[20] H. Wang, D. Nezich, J. Kong, and T. Palacios, "Graphene frequency multipliers," *IEEE Electron Device Lett.*, vol. 30, no. 5, pp. 547–549, May 2009.

[21] E. Guerriero, L. Polloni, L. G. Rizzi, M. Bianchi, G. Mondello, and R. Sordan, "Graphene audio voltage amplifier," *Small*, vol. 8, no. 3, pp. 357–361, Feb. 2012.

[22] A. D. Smith *et al.*, "Electromechanical piezoresistive sensing in suspended graphene membranes," *Nano Lett.*, vol. 13, no. 7, pp. 3237–3242, Jun. 2013.

[23] A. D. Smith *et al.*, "Pressure sensors based on suspended graphene membranes," *Solid-State Electron.*, vol. 88, pp. 89–94, Oct. 2013.

[24] F. Schedin *et al.*, "Detection of individual gas molecules adsorbed on graphene," *Nature Mater.*, vol. 6, pp. 652–655, Jul. 2007.

[25] A. D. Smith *et al.*, "Resistive graphene humidity sensors with rapid and direct electrical readout," *Nanoscale*, vol. 7, pp. 19099–19109, Oct. 2015.

[26] A. Y. Serov, Z.-Y. Ong, M. V. Fischetti, and E. Pop, "Theoretical analysis of high-field transport in graphene on a substrate," *J. Appl. Phys.*, vol. 116, no. 3, p. 034507, Jun. 2014.

[27] M. Lafkioti *et al.*, "Graphene on a hydrophobic substrate: Doping reduction and hysteresis suppression under ambient conditions," *Nano Lett.*, vol. 10, no. 4, pp. 1149–1153, 2010.

[28] C. R. Dean *et al.*, "Boron nitride substrates for high-quality graphene electronics," *Nature Nanotechnol.*, vol. 5, no. 10, pp. 722–726, 2010.

[29] C. Hwang *et al.*, "Fermi velocity engineering in graphene by substrate modification," *Sci. Rep.*, vol. 2, Aug. 2012, Art. no. 590.

[30] J. Mohrmann, K. Watanabe, T. Taniguchi, and R. Danneau, "Persistent hysteresis in graphene-mica van der Waals heterostructures," *Nanotechnology*, vol. 26, no. 1, p. 015202, 2014.

[31] J. Xue *et al.*, "Scanning tunnelling microscopy and spectroscopy of ultra-flat graphene on hexagonal boron nitride," *Nature Mater.*, vol. 10, pp. 282–285, Feb. 2011.

[32] H. Wang *et al.*, "BN/graphene/BN transistors for RF applications," *IEEE Electron Device Lett.*, vol. 32, no. 9, pp. 1209–1211, Sep. 2011.

[33] M. Yankowitz, J. Xue, and B. J. LeRoy, "Graphene on hexagonal boron nitride," *J. Phys., Condens. Matter*, vol. 26, no. 30, p. 303201, Jul. 2014.

[34] N. Petrone, T. Chari, I. Meric, L. Wang, K. L. Shepard, and J. Hone, "Flexible graphene field-effect transistors encapsulated in hexagonal boron nitride," *ACS Nano*, vol. 9, no. 9, pp. 8953–8959, Aug. 2015.

[35] F. Schwierz, "Graphene transistors: Status, prospects, and problems," *Proc. IEEE*, vol. 101, no. 7, pp. 1567–1584, Jul. 2013.

[36] H. Pandey *et al.*, "Enhanced intrinsic voltage gain in artificially stacked bilayer CVD graphene field effect transistors," *Annalen der Physik*, vol. 529, no. 11, p. 1700106, Nov. 2017.

[37] B. N. Szafranek, G. Fiori, D. Schall, D. Neumaier, and H. Kurz, "Current saturation and voltage gain in bilayer graphene field effect transistors," *Nano Lett.*, vol. 12, no. 3, pp. 1324–1328, 2012.

[38] S. M. Kim *et al.*, "Synthesis of large-area multilayer hexagonal boron nitride for high material performance," *Nature Commun.*, vol. 6, Oct. 2015, Art. no. 8662.

[39] K. Nagashio, T. Nishimura, K. Kita, and A. Toriumi, "Contact resistivity and current flow path at metal/graphene contact," *Appl. Phys. Lett.*, vol. 97, no. 14, p. 143514, 2010.

[40] M. Shaygan *et al.*, "Low resistive edge contacts to CVD-grown graphene using a CMOS compatible metal," *Annalen der Physik*, vol. 529, no. 11, p. 1600410, Nov. 2017.

[41] L. Wang *et al.*, "One-dimensional electrical contact to a two-dimensional material," *Science*, vol. 342, no. 6158, pp. 614–617, 2013.

[42] A. Das, B. Chakraborty, and A. K. Sood, "Raman spectroscopy of graphene on different substrates and influence of defects," *Bull. Mater. Sci.*, vol. 31, no. 3, pp. 579–584, Jun. 2008.

[43] A. C. Ferrari *et al.*, "Raman spectrum of graphene and graphene layers," *Phys. Rev. Lett.*, vol. 97, no. 18, p. 187401, 2006.

[44] R. V. Gorbachev *et al.*, "Hunting for monolayer boron nitride: Optical and Raman signatures," *Small*, vol. 7, no. 4, pp. 465–468, Feb. 2011.

[45] M. Nagel, C. Matheisen, S. Sawallich, and H. Kurz, "Photoconductive microprobe enabled on-chip and wafer-scale terahertz sensing applications," in *Proc. Adv. Photon. OSA Tech. Dig.*, Jun./Jul. 2015, Paper SeM2D.5.

[46] J. D. Buron *et al.*, "Terahertz wafer-scale mobility mapping of graphene on insulating substrates without a gate," *Opt. Express*, vol. 23, no. 24, pp. 30721–30729, 2015.

[47] N. Vukmirović, C. S. Ponseca, Jr., H. Němec, A. Yartsev, and V. Sundström, "Insights into the charge carrier terahertz mobility in polyfluorenes from large-scale atomistic simulations and time-resolved terahertz spectroscopy," *J. Phys. Chem. C*, vol. 116, no. 37, pp. 19665–19672, Aug. 2012.

[48] J. Lauth *et al.*, "Photogeneration and mobility of charge carriers in atomically thin colloidal InSe nanosheets probed by ultrafast terahertz spectroscopy," *J. Phys. Chem. Lett.*, vol. 7, no. 20, pp. 4191–4196, Oct. 2016.

[49] M. Tinkham, "Energy gap interpretation of experiments on infrared transmission through superconducting films," *Phys. Rev. J. Arch.*, vol. 104, no. 3, pp. 845–846, Nov. 1956.
[50] S. Kim *et al.*, "Realization of a high mobility dual-gated graphene field-effect transistor with Al_2O_3 dielectric," *Appl. Phys. Lett.*, vol. 94, no. 6, p. 062107, 2009.
[51] E. Guerriero *et al.*, "High-gain graphene transistors with a thin AlO_x top-gate oxide," *Sci. Rep.*, vol. 7, Dec. 2017, Art. no. 2419.

Himadri Pandey (M'12) received the B.Tech. degree in mechanical engineering from the Motilal Nehru National Institute of Technology, Allahabad, India, in 2008, and the M.Sc. degree in nanotechnology from the KTH Royal Institute of Technology, Stockholm, Sweden, in 2013. He is currently pursuing the Ph.D. degree in high frequency applications of graphene under Prof. Dr.-Ing. Max C. Lemme with RWTH Aachen University, Aachen, Germany.

Mehrdad Shaygan received the Ph.D. degree in nanotechnology/nanoelectronics from the Pohang University of Science and Technology, Pohang, South Korea, in 2014.

He was involved in different types of nanomaterials and their potential application in nanoelectronics, including field-effect transistors and optoelectronic devices. He is currently a Research Associate with AMO GmbH, Aachen, Germany, where he is involved in graphene-based electronic devices.

Simon Sawallich received the Diploma degree in solid-state physics from RWTH Aachen University, Aachen, Germany, in 2012.

From 2012 to 2014, he was a Research Assistant for THz research and development at AMO GmbH, Aachen, before co-founding Protemics GmbH, Aachen, in 2014. Since then, he is the Chief Research Officer at Protemics GmbH and in charge of research activities and analytic services.

Satender Kataria received the Ph.D. degree in physics from Madras University, Chennai, India, in 2010.

In 2011, he joined the National Aerospace Laboratories, Bengaluru, India, as a Scientist Fellow. In 2012, he joined National Taiwan University, Taipei, Taiwan, as a Post-Doctoral Researcher. He is currently a Post-Doctoral Researcher with the RWTH Aachen University, Aachen, Germany. His current research interests include large-area synthesis and characterization of 2-D materials and their heterostructures.

Zhenxing Wang received the Ph.D. degree in nanoelectronics from the Department of Electrical Engineering, Peking University, Beijing, China, in 2012.

From 2012 to 2014, he was a Post-Doctoral Researcher with the University of Erlangen-Nuremberg, Erlangen, Germany. He is currently with AMO GmbH, Aachen, Germany, where he is focusing on graphene-based electronic devices and circuits.

Achim Noculak received the Dipl.-Ing. degree from Fachhochschule Aachen, Aachen, Germany, in 1996.

He is currently with the Chair of High Frequency Electronics, RWTH Aachen University, Aachen, where he is an in-charge of the High Frequency Measurement Laboratory.

Martin Otto received the Dipl.-Ing. degree in electrical engineering from RWTH Aachen University, Aachen, Germany, in 1999.

He is currently a Researcher with AMO GmbH, Aachen. His current research interests include graphene synthesis and transfer.

Michael Nagel was born in Viersen, Germany, in 1970. He received the Diploma degree in electrical engineering from RWTH Aachen University, Aachen, Germany, in 1996, and the Ph.D. degree from the Faculty of Electrical Engineering, RWTH Aachen University, in 2003.

From 2011 to 2014, he led the THz R&D Department, AMO GmbH, Aachen. Since 2014, he has been the CEO and the Co-Founder of Protemics GmbH, Aachen.

Renato Negra received the M.Sc. degree in telematics from the Graz University of Technology, Graz, Austria, and the Ph.D. degree in electrical engineering from ETH Zurich, Zürich, Switzerland.

From 1998 to 2000, he was with NorSpace AS, Horten, Norway, where he was involved in the design and characterization of space-qualified RF equipment. He currently holds the Chair of High Frequency Electronics at RWTH Aachen University, Aachen, Germany.

Daniel Neumaier received the Ph.D. degree in physics from the University of Regensburg, Regensburg, Germany, in 2009.

From 2006 to 2009, he was with the Group of Dieter Weiss, University of Regensburg, where he was involved in the field of GaAs-based spintronics. He has been the Head of the Graphene Group, AMO GmbH, Aachen, Germany, since 2009. In the Flagship-Project Graphene, he is the Leader of the work-package electronics devices and is the Head of Division 3.

Max C. Lemme (M'00–SM'06) received the Dipl.-Ing. and Dr.-Ing. degrees in electrical engineering from RWTH Aachen University, Aachen, Germany.

He currently holds the Chair of Electronic Devices at RWTH Aachen University and is the Director of AMO GmbH, Aachen. His current research interests include electronic, optoelectronic and nanoelectromechanical devices made from silicon, graphene, and 2-D materials and questions of process integration.