Failure of Switching Operation of SiC-MOSFETs and Effects of Stacking Faults on Safe Operation Area

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***Abstract*— When developing silicon carbide (SiC) devices, the reliability of the internal body diode is an important issue. Stacking faults (SFs) are expanded from basal plane defects by using a body diode. Although it is well known that on-voltage degradation occurs due to SFs, their effects on dynamic reliability have not been studied well. Furthermore, including the effects of SFs, there are not many reports about the dynamic reliability of SiC-MOSFETs. In this paper, a double-pulse switching test using 3.3-kV SiC-MOSFETs was carried out to clarify the failure mechanism of the switching operation of SiC-MOSFETs and effects of SFs on the safe operation area (SOA). Before the switching test, current stress was applied to the body diode of the devices under test (DUTs) to expand the SFs. The circuit configuration was half-bridge type, and a double-pulse gate signal was applied to the lower arm DUT. The switching voltage was 1.8 kV, and the switching current increased at about 8-A steps to failure. As a result, reverse recovery SOA (RRSOA) reliability decreased depending on the amount of SFs in the SiC-MOSFET. Because RRSOA failure was caused by avalanche due to the hole concentration during reverse recovery and the SFs raised local current density, reverse bias SOA (RBSOA) hardly decreased even if SFs containing SiC-MOSFETs were used. This is because RBSOA failure was caused by degradation of the gate isolation layer due to overheating and the temperature coefficient of the SFs electric resistance indicated negative.**

***Index Terms*— Body diode, safe operation area (SOA), SiC-MOSFET, stacking fault (SF).**

I. Introduction

SILICON carbide (SiC) is an advanced material for power electronics applications [1]–[3]. In particular, SiC-MOSFETs are being developed actively. Power modules are required to be smaller, which can be achieved by using SiC-MOSFETs with an internal body diode [4]–[6]. However, the reliability of the body diode is an important issue in SiC-MOSFETs. It is well known that ON-voltage degradation occurs due to the expansion of stacking faults (SFs) from basal plane dislocations (BPDs) [7]–[10]. Although MOSFETs are unipolar devices, if a body diode is used and BPDs exist, SF expansion occurs. Since electrons are trapped in SFs that exist epitaxial layer, not only the forward voltage of body diodes but also the ON-voltage of MOSFETs degrade. On the other hand, the effects of SFs on dynamic reliability, such as a safe operation area (SOA), have not been studied well. SOA is an important characteristic of power module operation [11]–[15]. Power modules must be used in the range of voltage and current defined by the SOA, but there are not many reports about the SOA of SiC-MOSFETs including the effects of SFs. In this paper, a double-pulse switching test using SiC-MOSFETs was carried out to measure reverse bias SOA (RBSOA) and reverse recovery SOA (RRSOA) to clarify the failure mechanism and effects of SFs.

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II. Experimental Procedure

A. Samples for Switching Test

In this paper, the SiC-MOSFETs for the switching test were double-implanted MOSFETs fabricated on a Si-faced, 4° off-axis toward the <11–20> direction, and n-type 4H-SiC substrate. The nominal voltage was 3.3 kV, and the epitaxial layer was 30 μm thick with an n-type doping concentration of 3×10^{15} cm^{-3}. To expand the SFs before the switching test, we applied 55 A/cm^2, 175 °C current stress to the body diode until degradation was saturated. The MOSFET ON-voltage was measured before and after the current stress was applied, and the degradation level was calculated using (1). If degradation did not occur, the degradation level was 1.0. The range of the degradation level of the devices under test (DUTs) was 1.0 through 8.0

$$\text{Degradation level} = \frac{V_{\text{on_after}}}{V_{\text{on_before}}}. \quad (1)$$

B. Switching Test Conditions

Fig. 1 shows the circuit configuration of the switching test, and Table I shows the circuit parameters. The circuit configuration was half-bridge, and the switching voltage was 1.8 kV. The Si-IGBT module was to protect the circuit from high current. It was turned OFF when the SiC-MOSFET failed to minimize influence of the failure and analyze the failure point. The gate and source terminals of the upper arm DUT

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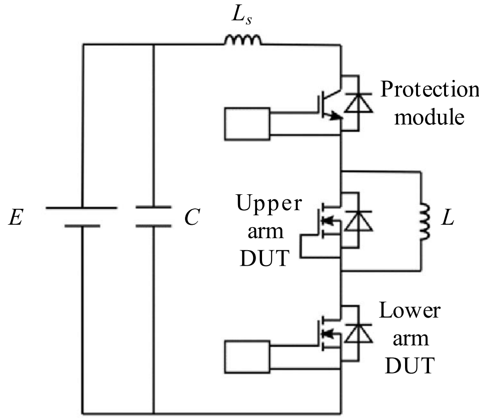


Fig. 1. Circuit configuration of the switching test.

TABLE I
CIRCUIT PARAMETERS

Name	Symbol	Value
Input voltage	E	1.8 kV
Input capacitance	C	470 µF
Stray inductance	L_s	4 µH
Load inductance	L	1 mH
Gate resistance	$R_{g(on/off)}$	130/160 Ω
Gate-drive voltage	$V_{g(on/off)}$	+15/-8 V

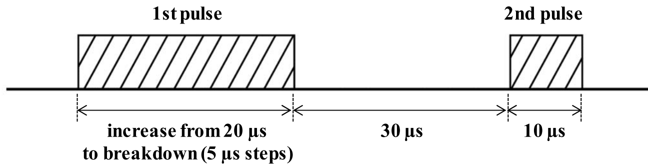


Fig. 2. Gate signal of the lower arm DUT.

were short connected to be used as a free-wheeling diode to analyze RRSOA. A double-pulse gate signal was applied to the lower arm DUT to analyze RBSOA. Fig. 2 shows the gate signal of the lower arm DUT. The width of the first pulse increased from 20 μs to failure in 5-μs steps, and the switching current ($I_{\rm sw}$) at failure was recorded. The failure of the upper arm DUT means that $I_{\rm sw}$ is beyond the limit of the RRSOA, and the failure of the lower arm DUT means that $I_{\rm sw}$ is beyond the limit of the RBSOA.

C. Current Flow Path Simulation

To estimate the carrier's route in SiC-MOSFETs containing SFs, current flow path simulation was carried out. The simulation software was ANSYS Q3D. Fig. 3 and Table II show the simulation conditions. The shape of the bulk was rectangular cuboid. Since the bulk material for the simulation has to be a conductor, copper was used. Pale gray area had 10× larger resistivity compared to that of yellow bulk and was put in the bulk in a 4° tilted state assuming SFs. Deep gray area had 1000× larger resistivity, assuming that there was a termination area. The current direction was from bottom to top, and the current density in the bulk was calculated.

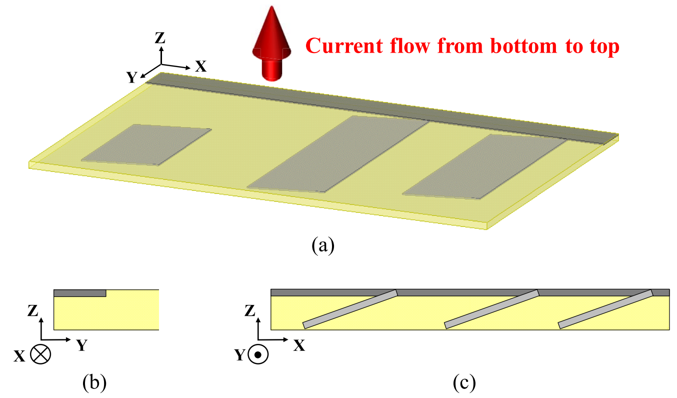


Fig. 3. Simulation diagram. (a) 3-D view. (b) *yz* plane. (c) *xz* plane.

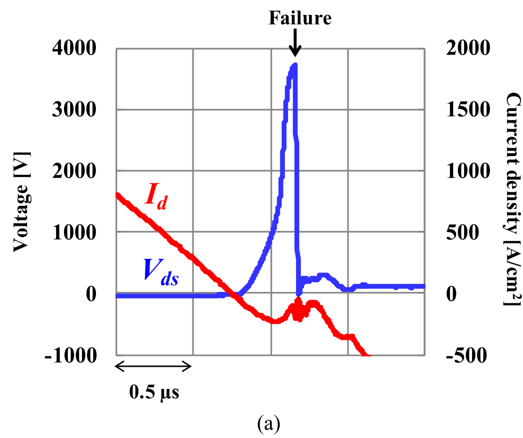
TABLE II
SIMULATION CONDITIONS

Color	Resistivity [Ω·m]	Width [µm]	Depth [µm]	Thickness [µm]
Yellow	1.68×10^{-8}	2000	1500	30
Pale gray	1.68×10^{-7}	340	Respective	5
Deep gray	1.68×10^{-5}	2000	170	5

III. RESULTS AND DISCUSSION

A. RRSOA and RBSOA Failure Model of SiC-MOSFET

Fig. 4 shows the RRSOA failure waveforms at degradation level 1.0. $I_{\rm sw}$ was about 1500 A/cm^2. The drain-to-source voltage ($V_{\rm ds}$) rose to 3.7 kV after the free-wheeling period, so it is inferred that the failure was caused by avalanche. Since $V_{\rm ds}$ at the previous step was barely lower than at failure, the failure occurred due to exceeding the limit of $V_{\rm ds}$. The failure occurred during the reverse recovery period. Then, the holes left in the n− epitaxial layer and n+ substrate went back to the source electrode, so the avalanche breakdown occurs at the point where more holes are concentrated. Fig. 5 shows a photoluminescence (PL) image of RRSOA failed DUT. The PL image was obtained at 420 nm using a long pass filter. Although the degradation level was 1.0, one SF existed. But the failure occurred near the termination area apart from the SF, so the holes were most concentrated and the local current density must be the highest at the failure point. Also, during Si bipolar device switching, there are reports that the current concentration and failure occur near the termination area [16], [17]. Fig. 6 shows a diagram of the hole concentration in a SiC-MOSFET. During reverse recovery, a high voltage is applied to the drain electrode, and holes left in the epitaxial layer and substrate are drawn to the source electrode, which is connected to the negative side of the power source. However, holes cannot pass through the termination area and concentrate near the MOSFET cell, which is located at the edge of the active area. Therefore, the avalanche breakdown occurs more easily at the edge of the active area. Fig. 7 shows the results of the current flow path simulation. The surface of the gray area was a high-resistance area assuming that there was a termination area. The current density was high at the edge of the high-resistance area.



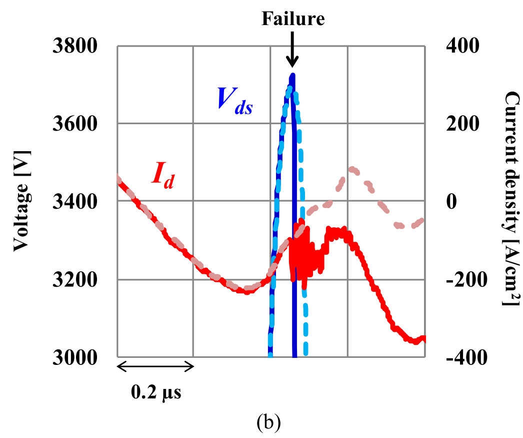


Fig. 4. RRSOA failure waveforms (degradation level 1.0). (a) Enlarged view of the failure point. (b) Dotted lines: previous step of failure.

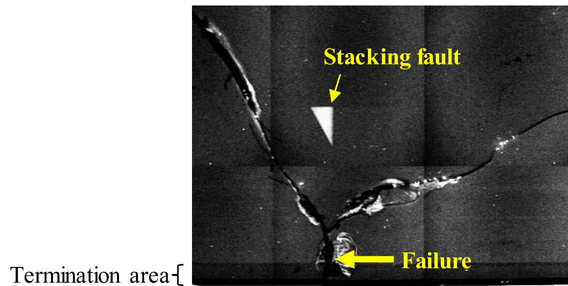


Fig. 5. PL image of RRSOA failed DUT (degradation level 1.0).

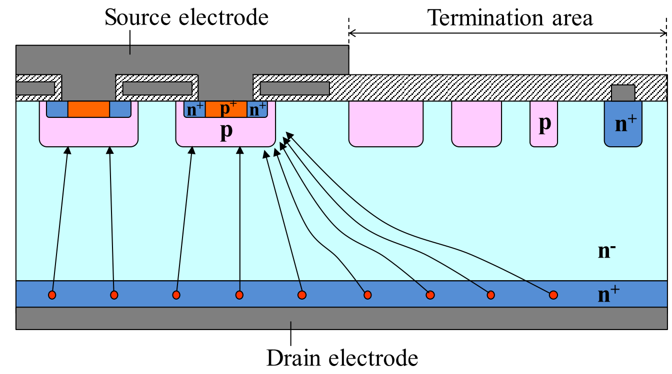


Fig. 6. Diagram of holes concentration.

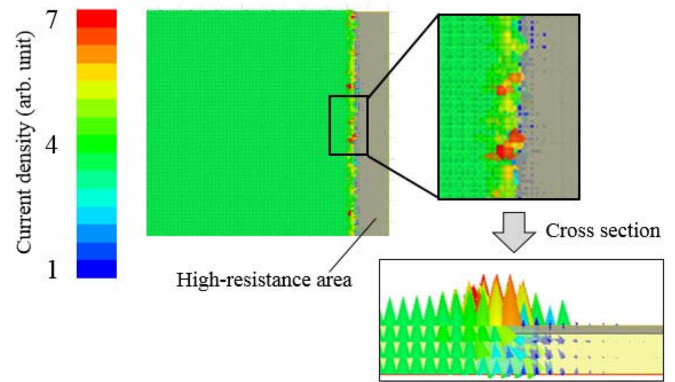


Fig. 7. Result of current flow path simulation (without SFs).

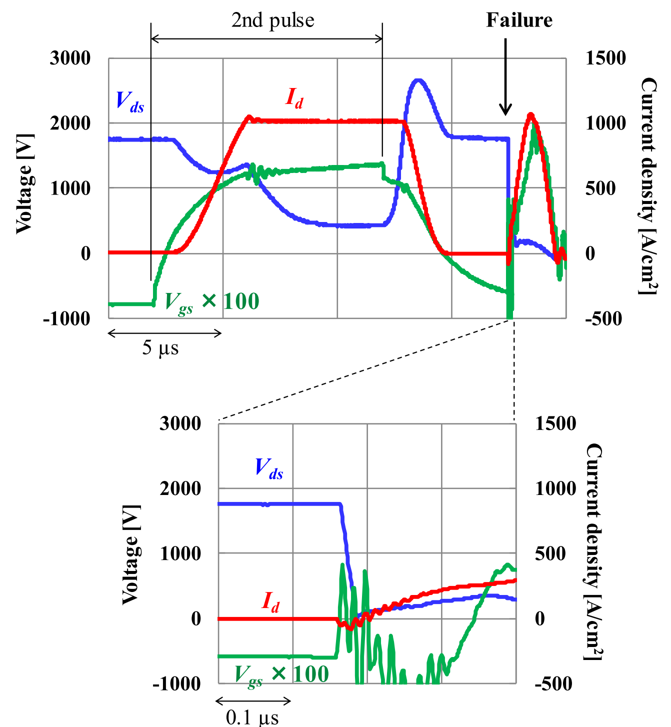


Fig. 8. RBSOA failure waveforms (degradation level 1.0).

This result indicates that the current avoids the high-resistance area and is concentrated at the edge of this area. Also, in actual SiC-MOSFETs, it is inferred that holes avoid the termination area and concentrate at the edge. When the current density is beyond the limit, avalanche breakdown occurs.

Fig. 8 shows the RBSOA failure waveforms at degradation level 1.0. I_{sw} was about 1000 A/cm^2. At the second pulse, the ON-voltage was close to 500 V because of the high I_{sw}, so self-heating should have been very high, and the temperature of the DUT should have risen. Then, the failure occurred after turn-OFF. Therefore, it is inferred that the gate isolation layer was broken by applying a high voltage and by the rising temperature because the gate isolation layer generally degrades under high temperature [18], [19]. Fig. 9 shows the temperature dependence of the gate leakage current. The gate leakage current increased depending on the temperature. The gate

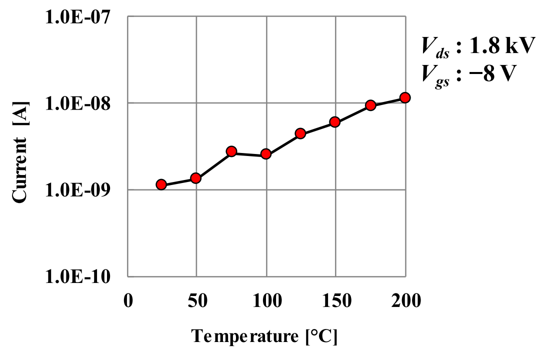


Fig. 9. Temperature dependence of gate leakage current.

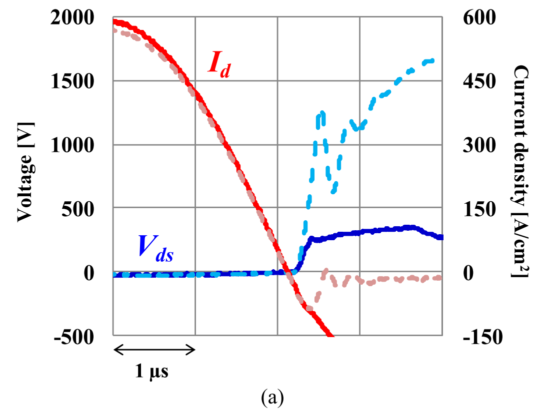
Fig. 10. Appearance image of RBSOA failed DUT (degradation level 1.0). Material of source electrode is aluminum.

leakage current was 10× larger at 200 °C compared to that at 25 °C. Therefore, the gate isolation layer steadily degraded as the temperature rose, and the failure occurred when it could not stand at the electric field that was applied to the drain electrode by high voltage. Also, in a Si-IGBT, failure mode where failure occurred some microseconds after turn-OFFhas been reported [20], [21]. These reports show failure mode occurring in a short-circuit test due to overheating. Fig. 10 shows the appearance image of RBSOA failed DUT. The aluminum electrode was severely damaged, so the DUT had a very high temperature, which was equal to or higher than the melting point of aluminum. The failure occurred near the bonding wire, and this is appropriate because the current heads toward the bonding wire, and the temperature rises more easily there.

These failure mechanisms shown in this section have no relation of SFs and can occur in any SiC-MOSFET.

B. Effects of Stacking Faults to SOA

Fig. 11 shows the RRSOA failure waveforms at degradation level 4.1 and 8.0. Fig. 11(a) shows the waveforms of degradation level 4.1. $I_{\rm sw}$ was about 600 A/cm^2 and was less than half of the result of degradation level 1.0. Fig. 11(b) shows the waveforms of degradation level 8.0. $I_{\rm sw}$ was about 270 A/cm^2 and was less than a quarter of the result of degradation level 1.0. These results indicate that the RRSOA reliability decreased dependently on the degradation level. The increasing of local current density due to SFs is considered to be the factor that leads to the results because the failure is caused by avalanche due to the hole concentration. Since SFs electrically act as resistance, if expansion of SFs occurs, the effective active area decreases, and the local current density in the nonaffected areas increases. Therefore, the failure occurred at lower $I_{\rm sw}$ at large degradation level DUTs. Fig. 12 shows the results of the current flow path simulation assuming DUTs containing SFs. The pale gray areas have 10× larger the resistivity and 1/6 the thickness compared to the yellow area assuming SFs. Fig. 12(a) and (b) contains three SFs and eight SFs, respectively. In Fig. 12(b), the current density is higher than in Fig. 12(a) wholly and near the dark gray area in which surface lets no current flow through. Also, in actual SiC-MOSFETs, it is inferred that



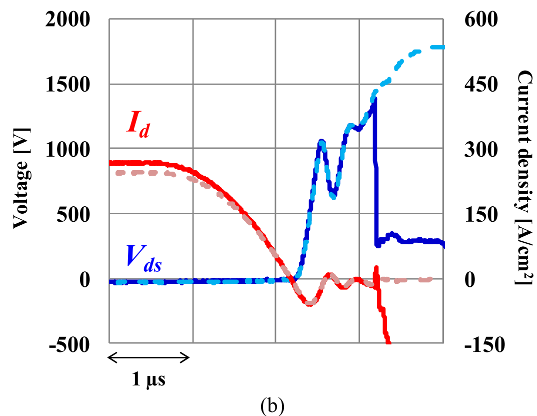


Fig. 11. RRSOA failure waveforms of (a) degradation level 4.1 and (b) degradation level 8.0. Dotted lines: previous step of failure.

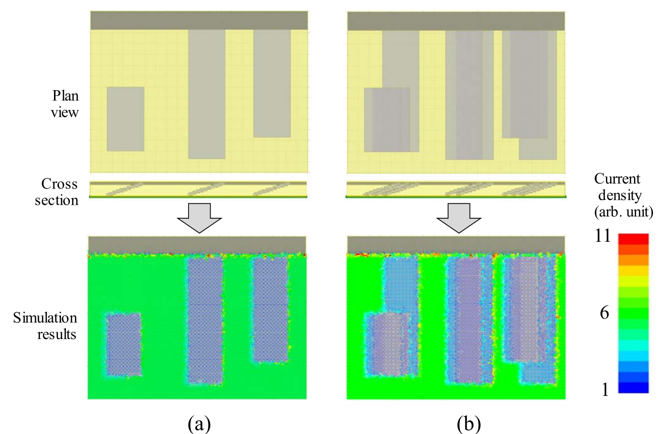


Fig. 12. Results of current flow path simulation with (a) three SFs and (b) eight SFs.

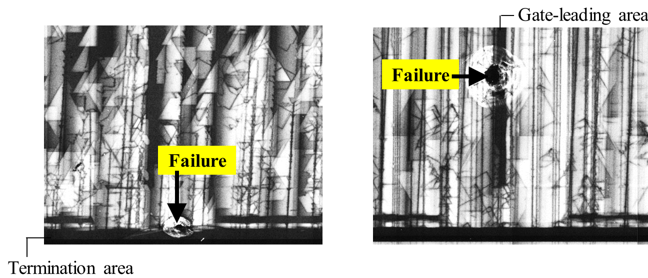


Fig. 13. PL image of RRSOA failure DUTs of (a) degradation level 4.1 and (b) degradation level 8.0.

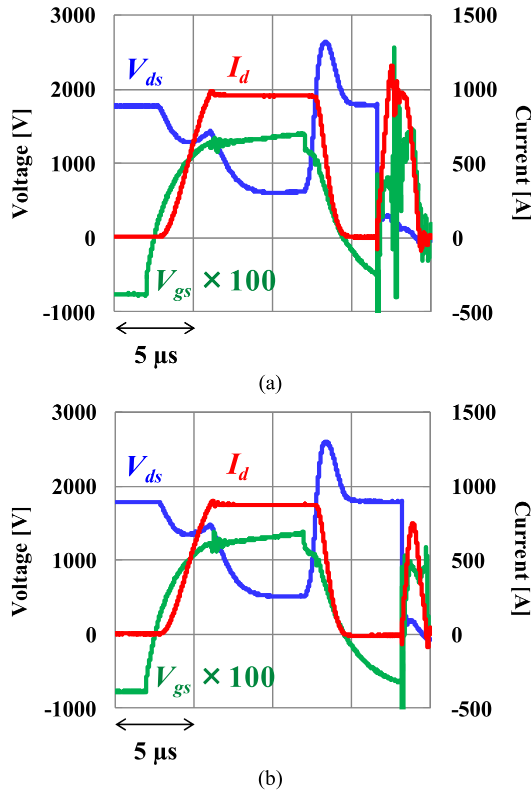


Fig. 14. RBSOA failure waveforms of (a) degradation level 4.1 and (b) degradation level 8.0.

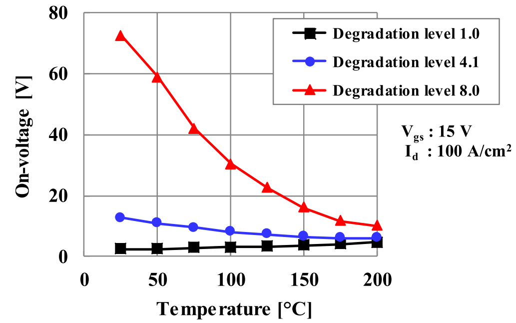


Fig. 15. Temperature dependence of the on-voltage.

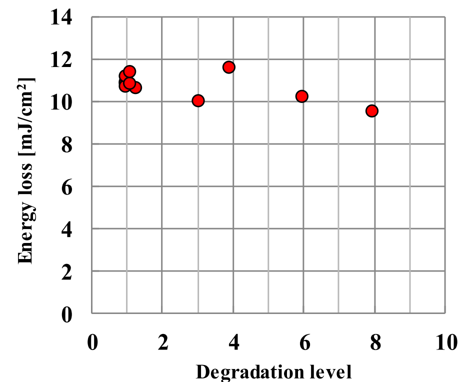


Fig. 16. Energy losses during the second pulse at failure step.

similar phenomenon occurred and the SiC-MOSFETs broke down at lower I_{sw}. Fig. 13 shows a PL image of RRSOA failed DUTs. In Fig. 13(a), failure occurred near the termination area shown in Fig. 5 (degradation level 1.0). This is appropriate because failure is caused by avalanche, and the carriers are more concentrated near the termination area. On the other hand, in Fig. 13(b), failure occurred away from the termination area. But the point was near the gate-leading area that carriers could not flow through as with the termination area. Therefore, near the gate-leading area, the current density is higher than closer to the center.

Fig. 14 shows the RBSOA failure waveforms at degradation levels 4.1 and 8.0. Fig. 14(a) shows the waveforms of degradation level 4.1. I_{sw} was about 950 A/cm^2 and hardly decreased compared to degradation level 1.0. Fig. 14(b) shows the waveforms of degradation level 8.0. I_{sw} was about 860 A/cm^2 and was about 10% less than the result of degradation level 4.1. Although self-heating during the second pulse was considered a factor of RBSOA failure, I_{sw} at failure did not decrease much. The cause of these results is considered to be the temperature dependence of the SF's electric resistance. Fig. 15 shows the temperature dependence of the ON-voltage. The ON-voltage decreased depending on the temperature. Although it was measured again at 25 °C after at 200 °C, the ON-voltage was almost the same as the first measurement. This means that the temperature coefficient of the SF's electric resistance indicates as negative. Thus, a model was proposed [22]. The model is that electron trapping decreases due to the reduction of the energy bandgap between the quasi-electron Fermi energy and the highest occupied state in the SF quantum well due to the Fermi energy reduction caused by the temperature rising. As shown in Fig. 14, the failure occurred after turn-OFF, which is the same as at degradation level 1.0. Therefore, it is inferred that the failure model is the same as that of degradation level 1.0 although more SFs exist. Since the RBSOA failure was caused by overheating, energy loss due to failure should not decrease dependently on degradation level. Fig. 16 shows the energy losses during the second pulse at the failure step. Except for degradation level 8.0, energy losses did not depend on degradation level. At degradation level 8.0, the ON-voltage might not decrease to the same level as that of low degradation level.

Fig. 17 shows I_{sw} at failure at each degradation level. RRSOA reliability decreased dependently on degradation

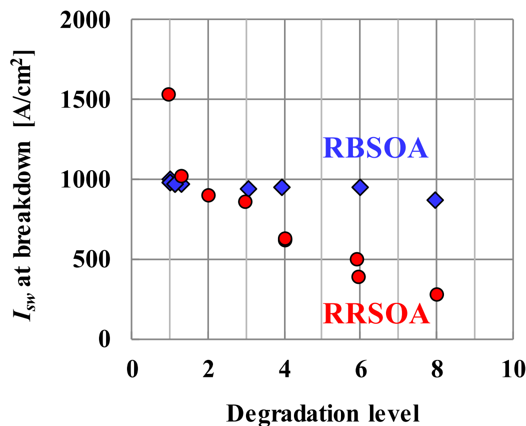


Fig. 17. Switching current at failure.

level. On the other hand, RBSOA reliability hardly decreased even if SFs containing SiC-MOSFETs were used.

IV. Conclusion

We carried out double-pulse switching tests using SiC-MOSFETs and analyzed the failure mode. RRSOA failure occurred near the termination or gate-wiring area, and we concluded that the failure was caused by avalanche due to hole concentration during reverse recovery. RRSOA reliability decreased when SFs expanded because the SFs reduced the effective active area and the current density increased. RBSOA failure occurred after turn-OFF, and the ON-voltage during the second pulse was very high. Therefore, we concluded that RBSOA failure was caused by degradation of the gate isolation layer due to overheating. Since the temperature coefficient of SF's electric resistance indicates as negative, RBSOA reliability hardly decreased even if SFs containing SiC-MOSFETs were used.

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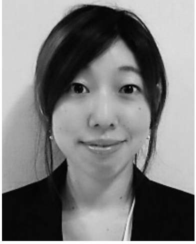

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