"Kink" in AlGaN/GaN-HEMTs: Floating Buffer Model

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***Abstract*— We report on a floating buffer model to explain "kink," a hysteresis in the output characteristics of Fe-doped AlGaN/GaN HEMTs observed at low drain bias. Unintentionally doped background carbon can make the GaN buffer p-type allowing it to electrically float. We further note that reverse bias trap-assisted leakage across the junction between the 2DEG and the p-type buffer can provide a mechanism for hole injection and buffer discharging at just a few volts above the knee, explaining the "kink" bias dependence and hysteresis. We show that HEMTs with a different background carbon have dramatically different kink behaviors consistent with the model. Positive and negative magnitude drain current transient signals with 0.9-eV activation energy are seen, corresponding to changes in the occupation of carbon acceptors located in different regions of the GaN buffer. The observation of such signals from a single trap calls into question conventional interpretations of these transients based on the bulk 1-D deep-level transient spectroscopy (DLTS) models for GaN devices with floating regions.**

***Index Terms*— Carbon doping, drain current transient spectroscopy, floating buffer, GaN, HEMT, iron doping, kink effect, traps.**

I. Introduction

THE kink effect is a hysteretic instability of FET drain current, which is observed during a slow drain bias sweep. The current shows a small step to increase a few volts above the knee region on the forward-sweep, with a little or no reduction on the return sweep. It has been observed in all generations of FETs, irrespective of the material system, whenever the substrate or surface is able to store charge and achieve a potential which diverges from ground. In partially depleted silicon on insulator MOSFETs or silicon on sapphire MOSFETs. [1], the floating conducting Si buffer is charged by a hole current from impact ionization. In GaAs FETs, the buffer is semi-insulating and can store impact ionization derived charge in deep trap states back-biasing the 2DEG and causing a kink [2]. Kink has also been observed in GaN HEMTs at both cryogenic [3] and room temperatures (RTs), with surface related traps originally assigned as the cause [4], although this explanation became untenable as it was unchanged as the passivation schemes improved. Previously, kink in GaN HEMTs has been attributed to impact ionization [5]. However, the fact that the kink is often seen just a few volts (as little as 2 and 3 V) above the knee makes it implausible for the carriers to have sufficient energy to cause impact ionization and provide a supply of holes. As a result, models have been suggested based on the unusual defect properties. Meneghesso *et al.* [6] proposed a strongly field-dependent detrapping process from deep acceptor states in the vicinity of the gate could be responsible for this effect. These states were linked to the epitaxy rather than being processing-related and showed a complex light sensitivity, which was related to yellow cathodoluminescence [7]. On the other hand, Wang and Chen [8] found that in their devices there was no kink in the very first bias sweep, contrary to the observations in [6] and [7], and that the kink magnitude increased with the maximum drain voltage [8]. They proposed a model based on strongly field-dependent trapping into deep donor states, again in the vicinity of the gate. In both of these models, the required field-dependent capture cross sections and trapping/detrapping processes cannot be explained by the conventional defect models.

In this paper, we show that the kink is strongly dependent on the growth conditions, which impact carbon concentration. We propose an explanation for kink in iron-doped (Fe) GaN/AlGaN HEMTs based on a "leaky dielectric" model of a floating semi-insulating p-type GaN buffer, [9] together with the conventional deep-level defect behavior. The supply of holes to charge the buffer then arises primarily due to band-to-band trap-assisted leakage paths rather than via impact ionization. Simulations of the hysteresis associated with the kink show that it can be enabled and modified by small changes in the concentration of background carbon that are well below the Fe density. We also demonstrate that conventional interpretations of drain current transient spectroscopy can be flawed in devices with a floating p-type GaN buffer.

II. Device Under Test and Measurements

Two wafers were grown using metal-organic chemical vapor deposition (MOCVD) with nominally identical layer structure

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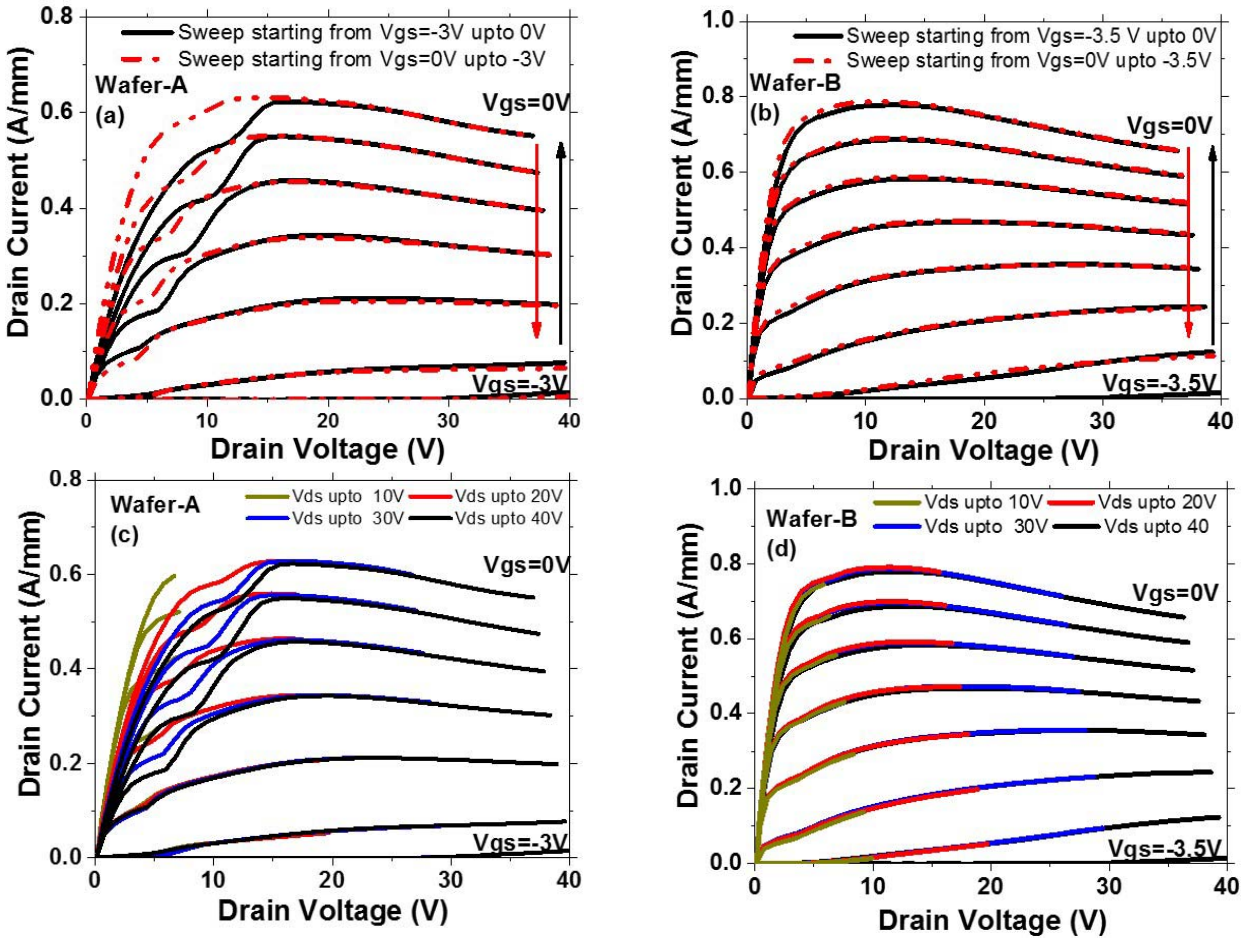

Fig. 1. dc I_D–V_{DS} sweeps for wafers A and B. (a) Wafer A and (b) Wafer B show the difference between V_{GS} stepping from −3 to 0 V and stepping from 0 to −3.5 V in the steps of 0.5 V. V_{DS} is swept from 0 up to 40 V. (c) Wafer A and (d) Wafer B show the impact of maximum V_{DS} sweep voltage on kink. V_{DS} swept up to 10, 20, 30, and 40 V with V_{GS} stepped from −3 to 0 V. Sweep rate is 1 V/s for all cases.

of AlGaN barrier, GaN buffer, and AlGaN nucleation layer on insulating SiC. Secondary ion mass spectrometry (SIMS) measurements were undertaken on similar wafers [shown in Fig. 3(b)] [10], [11]. Both wafers incorporated a conventional Fe doping profile in the GaN bulk to suppress short-channel effects, having a peak density of 3×10^{18} cm^{-3}, which decreased exponentially towards the surface. Both wafers had a 0.2-μm GaN channel region with unintentionally incorporated carbon density of 5×10^{16} cm^{-3}, but different growth conditions in the lower part of the GaN layer resulted in different carbon profiles. Wafer A had $3 \pm 1 \times 10^{17}$ cm^{-3} carbon and wafer B had 2×10^{16} cm^{-3} carbon. Oxygen and silicon were below the SIMS background of 5×10^{15} cm^{-3}.

AlGaN/GaN HEMTs with a width of 2×125 μm, a gate length of 0.25 μm, source–drain spacing of 4 μm, and source–gate spacing of 1 μm were fabricated using Ti/Al/Ni/Au and Ni/Au for ohmic and Schottky contacts, respectively, and with identical silicon nitride passivation. Repeatability was demonstrated by processing a further pair of wafers grown with the same conditions, with essentially identical results (not shown). Fig. 1(a) and (b) shows the result of a dc I_D–V_{DS} measurement at sweep rate of 1 V/s demonstrating the effect of stepped gate voltage sweep direction. Wafer A showed a strong kink effect, with hysteresis observable at V_{DS} below the kink, which is sweep history-dependent. It has been reported that the first forward-sweep can be kink free [8], however, in this case a small kink is observable at $V_{GS} = 0$ for Wafer A, with a much lower magnitude than subsequent sweeps Fig. 1(a). The kink was seen ∼3–5 V above the knee in all cases and was found to increase in magnitude with increasing the maximum drain bias Fig. 1(c). Above the kink, all signs of hysteresis are suppressed. These observations are broadly similar to the prior reports in [5]. By contrast, for wafer B the kink and its associated hysteresis was almost entirely suppressed, as shown in Fig. 1(b), and did not show a significant dependence on the maximum drain voltage in the sweep, Fig. 1(d).

Fig. 2 shows the result of the drain current transient measurements at $V_{DS} = 4$ V (above the knee but below the kink) following a step from $V_{DS} = 20$ V at $V_{GS} = -1.7$ V and at different temperatures. The transient drain current corresponds to measure the hysteretic recovery seen in Fig. 1 following a bias sweep to high V_{DS}. Wafer B shows a relatively simple behavior, displaying a recovery consistent with electron detrapping with a single time constant of $\sim 10^{-2}$s at RT and activation energy of ∼0.55 eV comparable with the measured values reported for Fe-doped devices [12], [13], superimposed

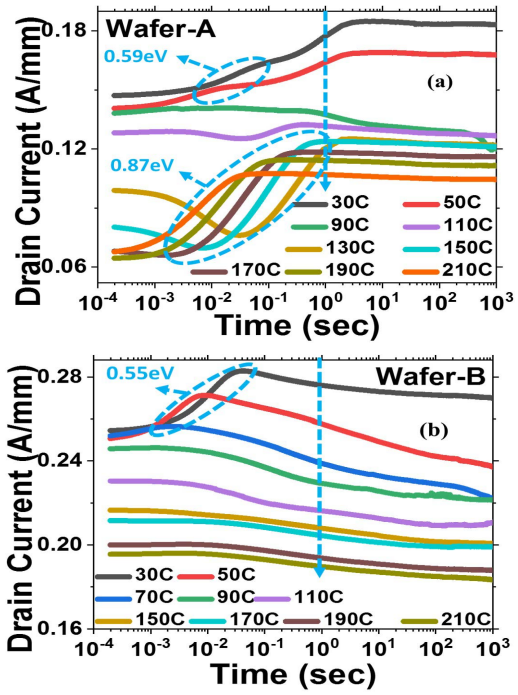

Fig. 2. Drain current transients measured in the kink region at the indicated temperatures from 30 °C to 210 °C at $V_{GS} = -1.7$ V and after V_{DS} is stepped from 20 to 4 V for (a) Wafer A and (b) Wafer B. Activation energies have been extracted for the circled features. The vertical line at 1 s indicates the approximate timescale for the dc sweep of Fig. 1.

on a background of slow drift at higher temperatures. A minimum of five temperatures have been used to calculate activation energies as summarized by Bisi *et al.* [14]; since the temperature range is at most 70 °C, the energies are subject to a significant error. By contrast, wafer A shows more complex behavior. Below 100 °C, wafer A shows two time constants, one at 10^{-2} s with activation energy ~0.59 eV (similar to wafer B), and the second one at ~1 s with very low activation energy. At temperatures >100 °C, a new regime is observed with overlapping positive and negative going transients; the positive going component having an activation energy of roughly 0.9 eV and the negative going one having a similar value but with larger error. At RT, it is clear that there is a reasonable consistency between the transient and sweep measurements. Wafer B shows a little kink because its recovery after high drain bias stress is faster than the effective time constant of the voltage sweep, whereas wafer A's longer recovery time makes the kink visible. In both cases for the sweeps, charge trapping occurs rapidly at higher drain bias, which is then neutralized more slowly below the kink (not shown here).

In order to determine where within the device the changes in current observed in the drain current transients were occurring, the transient measurements of the distribution of channel resistance were undertaken. The ON-resistance was taken as $R_{ON} = R_S + R_D$, where R_S and R_D are the access resistances on either side of the gate. Using the gate as a potential probe a small probe voltage of −100 to +100 mV was applied on the drain (nominal $V_{DS} = 0$ V), and R_S and R_D were measured within 2 s following a stress at 4 or 20 V, as shown in Table I.

TABLE I
SUMMARY OF SOURCE RESISTANCE (R_S) AND DRAIN RESISTANCE (R_D) MEASURED FOR BOTH WAFERS FOR NO STRESS AND AFTER $V_{DS} = 4$ AND 20 V STRESSES

		Rs (Ω.mm)	Rd (Ω.mm)
Wafer-A	No stress	0.40	2.5
	4V stress	0.36	2.7
	20V stress	0.28	3.2
Wafer-B	No Stress	0.33	2.0
	4V stress	0.33	2.3
	20V stress	0.34	3.4

For wafer A, we observed a decrease in R_S and an increase in R_D after stress, whereas for wafer B an increase in R_D and no change in R_S was seen.

III. MODEL

The GaN buffer in this case is Fe-doped which has an acceptor trap level 0.5–0.7 eV below the conduction band [15] and is normally assumed to be n-type due to Fe pinning of the Fermi level (E_F) in the upper half of the gap, preventing the buffer from floating. However, as pointed out in [16] and [17], unintentionally incorporated doping (UID) with carbon can convert it into p-type. Carbon on the nitrogen site (C_N) has an acceptor trap level 0.9 eV above the valence band (VB) [18]. Fe and C_N are both deep acceptors, and in the absence of any external field, the Fermi level will lie near the lowest energy level (C_N), with acceptors above the Fermi level being neutral (Fe). The degree of compensation by donors is critical in determining the n- or p-type nature of the GaN but is normally unknown. The Fermi level will switch between close to the Fe trap level and close to the C_N level, a shift of ~1.8 eV, when the donor density is greater than or less than the C_N density, respectively. There are several literature reports of related effects. Raman measurements of commercial Fe-doped devices fabricated by Cree (CGHV1J006D) suggested that the bulk GaN was indeed p-type [19]. In that case, the SIMS background carbon density was 10^{17} cm^{-3} with an unknown donor density, which presumably must have been less than that value. Scanning probe measurements in carbon-doped GaN have shown that the material can change from p-type at high C density to n-type at low density [20]. Koller *et al.* [21] measured the built-in voltage in a p-n diode and showed that high C density material is p-type.

The consequence of high carbon doping making the material p-type is that the highly resistive GaN buffer will be isolated from the 2DEG by a p-n junction. Hence the buffer can float and act as a reservoir for time-dependent charge storage. We argue here that this can be the origin of the kink effect, with the buffer reaching a bias history-dependent potential at low bias below the kink and coming into equilibrium with the 2DEG at higher drain bias above the kink as a result of field-dependent leakage across the p-n junction.

To understand the effect of UID carbon on the HEMT, an Fe-doped GaN device with $L_{SD} = 3.75$ μm and $L_G = 0.25$ μm has been simulated with Silvaco Atlas for a

TABLE II
GaN Buffer Profiles Used for Simulation

	Case-1 (wafer A)	Case-2 (wafer B)	Case-3 (wafer B)
Fe acceptor (E_C-0.7eV) (cm^{-3})	$7x10^{15}$ at 2DEG increasing exponentially with depth to $3x10^{18}$ at 1.1μm		
C_N acceptor (E_V+0.9eV) (cm^{-3})	$2x10^{17}$	$1.5x10^{16}$	$1.5x10^{16}$
C_{Ga} and intrinsic donors (E_C-0.03eV) (cm^{-3})	$1x10^{17}$	$0.5x10^{16}$	$2.5x10^{16}$

wide range of compensation ratio and donor densities [22]. Three illustrative GaN buffer doping combinations are shown in Table II, and the resulting band diagrams and doping profiles are shown in Fig. 3. Case 1 corresponds to wafer A with 3×10^{17} cm^{-3} carbon, where the compensation ratio of carbon on the Ga (donor) and N (acceptor) sites, C_{Ga}/C_N, has been set at 0.5 consistent with what is inferred for power devices and making the layer p-type [9], [23]. Cases 2 and 3 correspond to the carbon profile of wafer B with 1.5×10^{16} cm^{-3} C_N and two assumptions for the unknown intrinsic donor density. Case 2 corresponds to a low donor density of 5×10^{15} cm^{-3} and hence the layer is dominated by the C_N and is also p-type, whereas Case 3 has a higher donor density of 2.5×10^{16} cm^{-3} which exceeds the C_N density and hence is n-type. In all cases, the 0.2-μm-thick channel region was fully depleted and doped with $3 \times 10^{16} C_N$ and 2×10^{16} cm^{-3} C_{Ga} making it semi-insulating (lightly p-type). No doping was incorporated in the 5 nm below the 2DEG to improve the simulator convergence. The capture cross section for Fe was set to 10^{-13} cm^2, a high value since Fe can capture via its excited states [17], [24], and C_N to 10^{-15} cm^2.

A key issue in the simulation of these devices is the requirement to include leakage paths through the reverse-biased depletion regions below the 2DEG. It is known from GaN LEDs and vertical p-i-n diodes that the reverse bias leakage occurs by a trap-assisted band-to-band hopping process associated with threading dislocations [25]–[27], which occurs at a low field far below that which is required for impact ionization. In GaN-on-Si devices [21], it has been shown by substrate ramps that there is a leakage through the UID GaN layer from the 2DEG to the p-type GaN:C buffer for the field polarity corresponding to positive drain bias [28]. Sufficient leakage to positively charge the buffer occurred in a few seconds for a field as low as 2×10^5 V/cm at RT. Hence it is reasonable to expect a hole current to flow into the buffer as soon as the field in the channel exceeds a few times 10^5 V/cm. Fig. 4 shows the simulated vertical electrical field at $V_{DS} = 10$ V. Case 3, which is n-type, shows low field since there is no significant voltage drop between the 2DEG and the buffer. However, cases 1 and 2, where the buffer is p-type, show a field of as much as 4×10^5 V/cm over the entire gate to drain gap suggesting that this does indeed provide a plausible explanation for hole leakage into the buffer at a bias consistent with the bias where a kink is observed. There is no built-in model for leakage in a reverse-biased GaN p-n junction in the simulator, and hence a simple

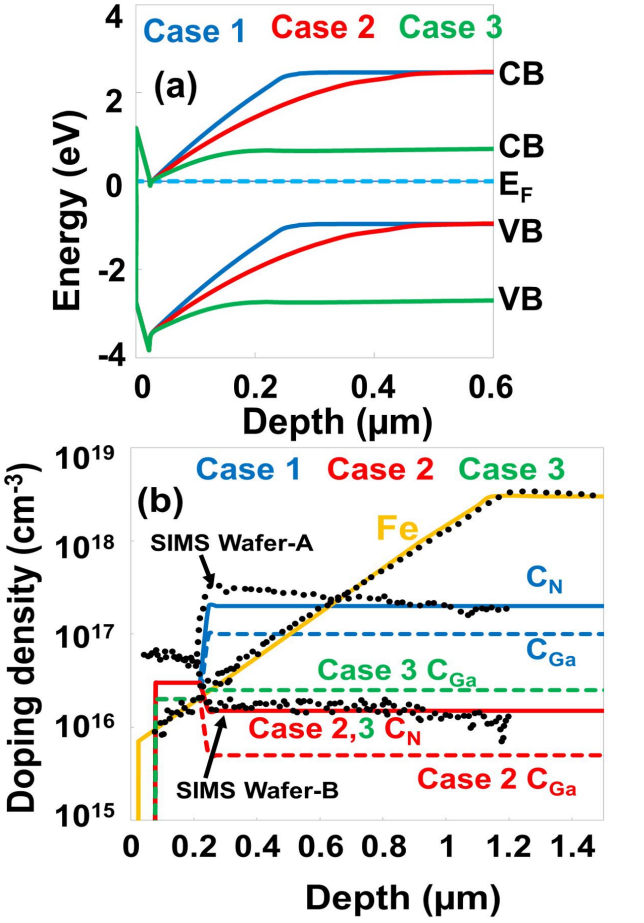

Fig. 3. (a) Simulated unbiased band profiles in this paper for a vertical cutline through the gate. (b) Doping density profiles as in Table II. Overlaid are measured SIMS profiles of Fe and C for similar wafers to A and B (shown in black dotted line).

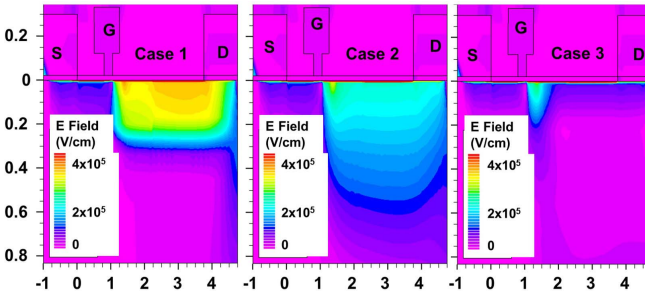

Fig. 4. Vertical electrical field component for the buffers of Table II at $V_{DS} = 10$ V and $V_{GS} = 0$ V. Cases 1 and 2, where the buffer is p-type, show a field of as much as 4×10^5 V/cm over the entire gate to drain gap, while for the n-type buffer of case 3, low field is predicted except at the gate edge.

approximation which has been used successfully to simulate current-collapse in GaN power devices was employed [9]. This uses a p++ shorting region located under the source and drain contacts, which provides a path for holes to flow into the semi-insulating buffer. It is well established that such leakage paths are often present under ohmic contacts [29]. This simulation approach requires holes to flow from the p++ region at the drain to gate region in order to impact the threshold voltage and thus results in unrealistically long time constants at RT. Nevertheless, it does allow the buffer potential to be sensitive

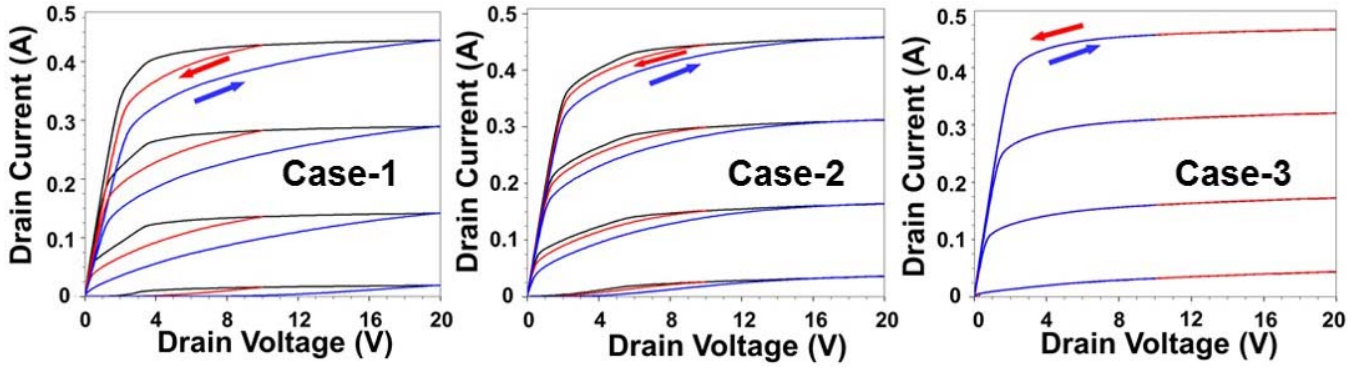

Fig. 5. Overlaid simulated output characteristics for the buffers of Table II with $V_{GS} = 0$ to -2 V in 0.5-V steps. Black line: static (equilibrium) sweep. Blue line: static bias of $V_{DS} = 20$ V, immediately followed by 10 V/s up-sweep from 0 to 20 V. Red line: static bias of 10 V followed by a 10 V/s down-sweep to 0 V.

to the drain bias, gives an indication of how buffer potential can affect the channel current by a back-gating mechanism, and seems to capture the behavior for T > 100 °C, as discussed later.

A simulation of the slow sweep leading to hysteresis is shown in Fig. 5, where a static IV characteristic is compared with two types of 10-V/s sweep. The assumption here is that leakage into the buffer will occur at $V_{DS} \geq 10$ V allowing the buffer to come into quasi-equilibrium with the drain bias during a slow sweep at all biases above 10 V. Hence a sweep at 10 V/s from the static case at $V_{DS} = 10$ V down to 0 V corresponds to the backward-sweep shown in Fig. 1. The forward-sweep of Fig. 1 is simulated by starting with a static simulation at $V_{DS} = 20$ V followed by a step to 0 V in 10 ns, followed by a slow sweep at 10 V/s up to 20 V. The simulation captures the hysteresis in I_D below the kink associated with charge stored at high drain bias. However, it will not capture the kink itself which would be caused by the onset of leakage between the 2DEG and the buffer, effectively pinning its potential to that in the 2DEG. For the n-type buffer (Case 3), no deviation from the static sweep is observed for the 10-V/s sweeps, whereas for the p-type buffers of Cases 1 and 2 there is a significant hysteresis (reduction) in current apparent in the knee region for the forward-sweep compared with the backward sweep case. For Case 1, the static sweep exceeds both forward- and backward-sweeps. These simulations clearly show how a kink could arise if a nonohmic leakage path was present. Charge distributions stored in the buffer cannot change easily at low bias if the buffer is floating but will be able to come into equilibrium at a few volts above the knee once hole charge can flow into the buffer.

To understand more clearly the origin of the complex transient behavior seen in Fig. 2, drain current transients in the kink region have been simulated for a bias step from 0 to 4 V (corresponding to initial sweep) and from 20 to 4 V (subsequent sweep), as shown in Fig. 6. For the three cases considered here, on step-down [Fig. 6(a)] there is a recovery apparent at ~10 ms corresponding to the neutralization of charge stored in ionized Fe acceptors under the gate, a time scale too short to be observed in the slow sweep simulations of Fig. 5. This Fe-related response arises even for the p-type Cases 1 and 2 since the Fermi energy must always cross the Fe

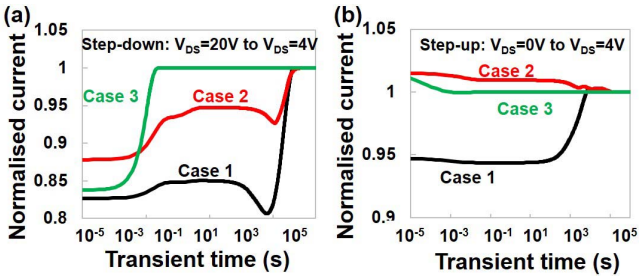

Fig. 6. Normalized drain current transients for the buffers of Table II (a) following step-down from $V_{DS} = 20$ to 4 V and (b) step-up from $V_{DS} = 0$ to 4 V, with $V_{GS} = -1.5$ V in all cases.

trap level within the channel depletion layer. This is followed by the negative and positive magnitude long time constant processes for Cases 1 and 2, as can also be observed for >100 °C in the current transient measurement for wafer A [see Fig. 2(a)]. A conventional interpretation of such negative and positive drain current transients would ascribe them to donor and acceptor traps, respectively, [14]. However, this cannot be the case in the simulation since the donors are always ionized and only changes in occupation of the C_N acceptor occurs. For Case 3, there is no barrier preventing electrons from flowing into the n-type buffer and hence no additional transients are observed on step-down.

Net ionized charge density for Case 1 with and without drain bias is shown in Fig. 7 to help to explain the mechanism of positive and negative magnitude contributions seen in Figs. 2(a) and 6(a). Fig. 7(a) for $V_{DS} = 0$ V shows that the depletion charge of ionized C_N is constant from source to drain except in the vicinity of the p++ shorting regions at the outer edges of the contacts. However, for positive drain bias, a small hole current starts to flowthrough the highly resistive buffer, forward biasing the depletion region in the source–gate gap and reverse biasing the depletion region in the gate–drain gap as can be seen for Fig. 7(b). This reduces the negative charge below the channel near the source and increases it near the drain, so R_S is reduced, and R_D increased. This is exactly what was measured for Wafer A, as shown in Table I. The reduction in R_S is excellent supporting evidence for the attribution of wafer A as p-type with a high C_N density. The absence of any change in R_S in Wafer B is consistent with

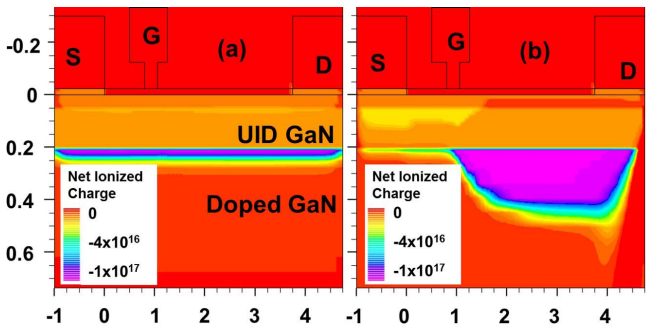

Fig. 7. Net ionized charge densities for Case 1 with a different bias. (a) $V_{GS} = 0$ V and $V_{DS} = 0$ V. (b) $V_{GS} = 0$ V and $V_{DS} = 20$ V.

its low C_N density. There is insufficient depletion charge to cause a significant change in R_S.

This all suggests that the positive and negative magnitude buffer time constants seen in Fig. 2(a) and simulated in Fig. 6(a) are all due to the same C_N acceptors but located in different parts of the device. The positive going transient is associated with the relaxation of negatively charged C_N acceptors located under the gate, whereas the negative component is due to ionization of neutral C_N acceptors in the source–gate depletion region. (There will also be relaxation of charged acceptors in the gate–drain gap, however, this will have a little impact on I_D above the knee since the device is saturated at $V_{DS} = 4$ V). Clearly the real situation for Wafer A in Fig. 2(a) is more complex, however, above 100 °C it is consistent with the simulation, with GaN transport dominated by bulk resistive conduction via holes thermally activated to the VB, thus explaining the observed 0.9-eV activation energy. We note that two time constants (and hence apparent capture cross sections) from the same trap has previously been observed in related measurements and simulations for a p-type floating buffer [30], although in that case both contributions had the same sign. Below 100 °C, the GaN buffer is more resistive and the behavior would be consistent with the hopping transport between the 2DEG and acceptors dominating, perhaps explaining the widely observed 0.5–0.6-eV activation energy [12], [14], [31].

There have been conflicting reports on the occurrence of the kink on the initial forward-sweep [6], [8]. Fig. 6(b) shows how this can arise depending on the background carbon concentration. It shows the change in current as V_{DS} is stepped from 0 V to $V_{DS} = 4$ V and corresponds to the first sweep from unbiased equilibrium to a bias below the kink but above the knee and hence in saturation. The high C_N density Case 1 shows a normalized increase in current of 6% mostly associated with a reduction in R_S. This compares with a 17% increase in current when stepping from 20 to 4 V [Fig. 6(a)] where the reduction in resistance under the gate exceeds the effect of the increase in R_S. By contrast, the low carbon density Case 2 shows minimal change for initial step-up [Fig. 6(b)]. This is because there is a correspondingly lower source region depletion charge and so there is an insignificant effect on R_S and hence would show no kink. Wafer A, which has the high carbon density, shows a small kink on the initial sweep in Fig. 1(a), consistent with this prediction. Wafer B shows minimal kink and is consistent with an n-type buffer meaning that there is a background concentration of donors greater than 2×10^{16} cm^{-3} whose origin is not known.

IV. Conclusion

Kink effect in Fe-doped devices, a hysteresis in drain current in the knee region of GaN HEMTs, is explained using a floating buffer model. To observe kink and hysteresis, two effects must be present: the presence of a background substitutional carbon impurity which makes the bulk of the GaN buffer p-type, and band-to-band trap-assisted leakage of holes from the 2DEG into the buffer at moderate electric fields. Both these requirements are likely to be met in Fe-doped MOCVD epitaxy explaining its relatively frequent observation. We note that kink is also often observed in carbon-doped power devices as a result of essentially the same mechanism. The magnitude of the kink and its precise time dependence is strongly dependent on the carbon concentration and its degree of self-compensation, the density of background donors, and the exact band-to-band leakage path, helping to explain why even apparently identically grown epitaxy can result in a different kink behavior. Depending on the carbon density, a kink can be either present or suppressed during the initial sweep providing an explanation for the reported difference in behavior in the literature [6], [8]. Suppression of the kink effect would require a detailed control of native defects and unintentional dopants as well as parasitic leakage paths and will constitute a challenge for the community.

We show that floating p-type buffers can result in transient behavior which is dependent on the transport path to the trap state rather than just the trap properties themselves. This results in positive and negative sign transients from the same trap, having the same activation energy but located in different parts of the device. Conventionally this would be interpreted as a "donor" and an "acceptor" trap having a different capture cross section. This calls into question some simplistic interpretations of drain current transient spectroscopy based on classical DLTS, which assume the availability of a bath of majority carriers.

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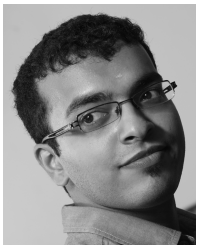

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