Impact of Substrate Resistivity on the Vertical Leakage, Breakdown, and Trapping in GaN-on-Si E-Mode HEMTs

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***Abstract*— This paper presents an extensive investigation of the impact of the resistivity of the silicon substrate on the vertical leakage and charge trapping in 200 V GaN-on-Si enhancement-mode high-electron mobility transistors. Three wafers having different substrate resistivities were submitted to combined DC characterization, step-stress experiments, and electroluminescence (EL) analysis. The results described within this paper demonstrate that: 1) the use of a highly resistive silicon substrate can increase the vertical breakdown voltage of the transistors, due to the fact that the voltage drop on the GaN buffer is mitigated by the partial depletion of the substrate (this latter causes a plateau region in the drain to substrate I–V characteristic) and 2) highly resistive substrate results in stronger trapping effects, due to the capacitance of the depleted substrate and the resulting backgating effects. The results described within this paper indicate that the choice of the resistivity of the substrate is the result of a tradeoff between high breakdown voltage (that could be in principle achieved through a highly resistive substrate) and the minimization of trapping processes (which can be hardly obtained with a resistive substrate).**

***Index Terms*— Buffer traps, GaN, high-electron mobility transistor (HEMT), vertical leakage.**

I. Introduction

GAN-ON-SILICON power high-electron mobility transistors (HEMTs) are promising devices for switching application in the range of voltages up to 1200 V. Thanks to the intrinsic properties of GaN [1], including the high-critical electric field (>3 MV/cm), high-electron mobility (up to 2000 $cm^2\ V^{-1}s^{-1}$) and high thermal conductivity (~1.3 $W\ K^{-1}cm^{-1}$), it is possible to fabricate devices with high breakdown voltage, high power-density, and low ON-resistance. This means that the next-generation power converters will be smaller and more efficient than today.

GaN power HEMTs are preferentially grown heteroepitaxially on a silicon substrate; this is so far the best solution, since a silicon compatible process allows the fabrication of large area (up to 200 mm) wafers, guaranteeing high yield and scalability, and a considerable cost reduction.

A critical aspect for power HEMTs is the robustness against high electric fields, in OFF-state conditions. In this operation mode, different breakdown phenomena can occur [2]: 1) lateral breakdown between drain and gate [3] or between and the drain and source [4], which are, respectively, related to passivation/barrier failure and punch through effects and 2) a vertical breakdown through the whole vertical stack [5], [6]. The lateral breakdown voltage can be increased by optimizing the geometry and the layout of the devices, as well as through an accurate design of the field plates. On the other hand, the vertical leakage and robustness are strictly related to the composition and thickness of the epitaxial layers [7], [8].

Several approaches have been exploited for increasing the vertical robustness of the GaN HEMTs [9]. Most of them act on the substrate that can significantly impact on the breakdown voltage: two recently adopted solutions are the use of a local p^+ doping of the silicon substrate just below the drain–gate region [10], and the local removal of the substrate between gate and drain [11], [12]. Both approaches are effective in increasing the breakdown voltage of the transistors.

The aim of this paper is to contribute to the understanding of the impact of the properties of the substrate on the stability and reliability of GaN-based power HEMTs. More specifically, we investigate the role of the substrate resistivity in defining the device's breakdown voltage, leakage current, and dynamic behavior. For the first time, we demonstrate that there is a tradeoff between the vertical robustness and the trapping effects; by increasing the resistivity of the substrate, the breakdown voltage increases due to the partial depletion of the silicon, while the dynamic behavior of the transistors

Manuscript received March 23, 2018; accepted April 23, 2018. Date of publication May 21, 2018; date of current version June 19, 2018. This work was supported by the Electronic Component Systems for European Leadership Joint Undertaking POWERBASE through the European Union's Horizon 2020 Research and Innovation Program and Austria, Belgium, Germany, Italy, The Netherlands, Norway, Slovakia, Spain, and U. K. under Grant 662133. This article reflects only the authors' view and the JU is not responsible for any use that may be made of the information it contains. The review of this paper was arranged by Editor A. Haque. *(Corresponding author: Matteo Borga.)*

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Digital Object Identifier 10.1109/TED.2018.2830107

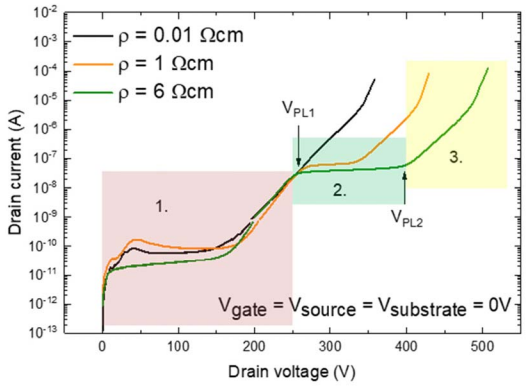

Fig. 1. Two-terminal vertical leakage measured on three wafers with different resistivities of the p-type silicon substrate. A "plateau" is observed only in the wafers having high substrate resistivity.

worsens, due to the parasitic capacitance of the depleted substrate, which leads to a positive backgating effect. Combined DC characterization, step-stress analysis, and substrate ramp experiments are used to define a model for the experimental data.

II. Experimental Details

The tested devices are normally off HEMTs based on an AlGaN/GaN heterostructure, with a p-type GaN gate [13]. The active region is grown over a carbon-doped GaN (C:GaN) layer that prevents punch through effects. A 25 × 1.525 μm-thick superlattice is placed over the substrate in order to minimize the density of dislocations that propagate from the silicon substrate and AlN nucleation layer through the nitride-based semiconductor. Three silicon substrates were used for device fabrication, having increasing resistivity: $\rho = 0.01$, 1, and 6 Ω·cm.

The geometry of the devices is as follows: gate–drain length $L_{GD} = 10$ μm, in order to avoid early lateral breakdown; gate width $W_G = 100$ μm; gate–source distance $L_{SG} = 0.75$ μm.

All the measurements and stresses were carried out with a power device analyzer Keysight B1505A having a high-voltage source-measurement unit (SMU) (±3000 V) and two high-power SMUs (±200 V). The measurements were carried out at different ambient temperatures, in the range between 30 °C and 120 °C. The electroluminescence (EL) analysis was carried out using a cooled charge-coupled device (CCD) camera with high sensitivity, which was mounted on an optical microscope equipped with a 50× lens.

III. Results and Discussion

A. Vertical Leakage Current: Dependence on Voltage and Physical Origin

To evaluate the impact of substrate resistivity on the vertical robustness and leakage current, we characterized the three wafers with different substrate resistivities by means of two terminal (drain-to-substrate) measurements (Fig. 1).

Three different regions can be identified in Fig. 1: in region 1, the vertical leakage through the structure is controlled by the voltage drop on the GaN buffer, while the voltage drop on the silicon substrate is minimum. For this

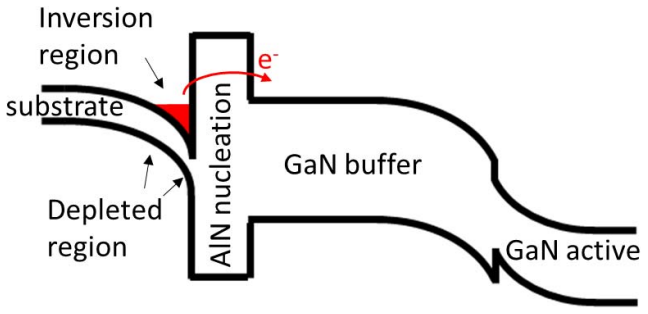

Fig. 2. Schematic band diagram of the vertical stack showing the depleted silicon substrate and the generation of an inversion layer at the Si/AlN interface.

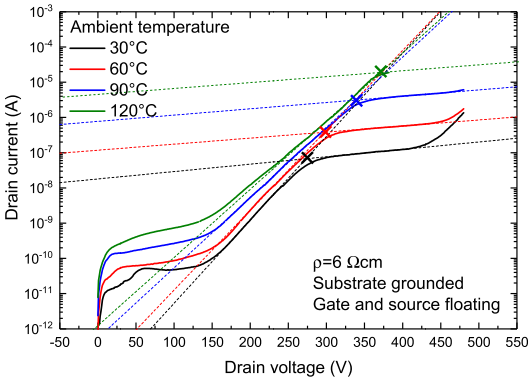

Fig. 3. Two-terminal vertical leakage current measured on the wafer with the highest substrate resistivity at different temperature levels. The voltage at which the plateau starts increases with temperature, consistently with a higher density of ionized doping in the buffer.

reason, all three wafers show identical behavior, regardless of substrate resistivity. In region 2, the I–V curves of the devices with resistive substrate ($\rho = 1$ and 6 Ω·cm) show a significant change in slope. A plateau (where the current is nearly constant with increasing voltage) can be identified. We ascribe this plateau to the partial depletion of the silicon substrate. As the drain–substrate voltage increases beyond a certain value (V_{PL1} in Fig. 1), a space charge region starts building up in the silicon substrate. As a consequence, the voltage on the GaN buffer stops increasing, and so does the vertical leakage current. In this voltage range, the silicon substrate acts as a parallel plate capacitor and charge builds up across it. The plateau ends at voltage V_{PL2} (indicated in Fig. 1 for the wafer with the highest substrate resistivity, black line), and the vertical leakage recovers the initial slope. We ascribe the end to the plateau to the injection of electrons from the silicon substrate to the GaN buffer. Recent studies [10], [14] pointed out that at high drain bias, an electron inversion region is generated at the AlN/Si interface (see Fig. 2). When the vertical voltage exceeds V_{PL2}, electron injection from substrate to the GaN buffer (through the AlN layer) may occur via trap-assisted tunneling. A few tens of volts before the catastrophic failure the current further increases (showing a change in the slope) probably due an avalanche in the Si substrate.

B. Temperature Dependence of Vertical Leakage and EL Investigation

In order to better characterize the origin of the "plateau" region, we carried out the current–voltage–temperature characterization of the samples having the substrate with the highest

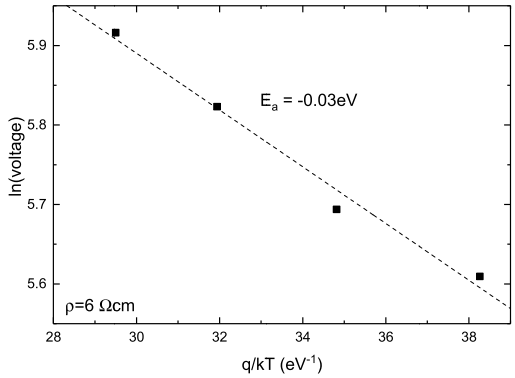

Fig. 4. Arrhenius plot of the voltage at which the plateau starts with the corresponding activation energy.

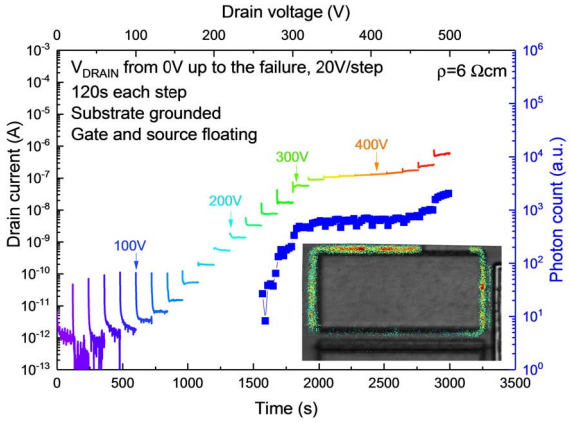

Fig. 5. Comparison between drain current and EL signal during a step-stress experiment. EL signal has the same trend as a drain current, indicating that when the plateau is reached, current and field stop increasing across the GaN buffer, and a significant depletion starts on the silicon substrate. Inset: false color EL pattern measured during a two-terminal (drain-to-substrate) stress on one of the analyzed devices, at 480 V. EL signal is emitted under and around the drain contact, while the rest of the device area is unaffected.

resistivity. The results of this analysis (Fig. 3) indicate the following: in region 1 ($V < 200$ V), the leakage current increases with temperature due to the increase in conductivity of the buffer layer. In fact, at higher temperatures, conduction may be favored by the increase in the free carrier density and by the increase in the thermal energy of the carriers. The most interesting changes with temperature are noticed in the plateau region, i.e., between 250 and 400 V. As can be noticed, with increasing temperature the voltage for the onset of the plateau (V_{PL1}) moves toward higher temperatures. An estimate of the dependence of V_{PL1} on temperature was obtained by defining V_{PL1} as the x-coordinate of the intercept of the linear regression of the plateau region and the linear regression of the region where the current strongly increases, as shown in Fig. 3. We found that V_{PL1} has an Arrhenius dependence on temperature, as shown in Fig. 4, with an activation energy of 30 meV. This value is consistent with the ionization energy of p-type acceptors in the p-silicon substrate, thus supporting the hypothesis on the plateau being related to the depletion of the substrate.

In order to further investigate the origin of the plateau, an EL analysis was performed. We measured the dependence of the EL signal on drain–substrate voltage as follows: with substrate grounded, the drain voltage was increased from 0 V to failure (step of 20 V every 120 s). During each step, an EL image was acquired with an exposure time of 10 s in order to avoid the saturation of the CCD sensor. Under high-vertical bias, the EL signal originates from the flow of hot electrons within the GaN stack. The electrons injected from the substrate are accelerated by the high field across the GaN buffer [15]. The deceleration of such electrons (bremsstrahlung) due to interaction with the lattice leads to the generation of a weak luminescence signal.

Fig. 5 shows the current measured during the staircase voltage sweep used for the EL characterization (thin solid line), along with the intensity of the EL signal collected from the sample (square dots). The inset of Fig. 5 reports a micrograph of the drain pad, showing a false-color map of the luminescence signal. As can be noticed, during the EL measurements, current shows the characteristic plateau at voltages between 250 and 300 V, consistently with the results in Figs. 1 and 3. A measurable EL signal starts being emitted at 200 V. Remarkably, also the EL signal shows a plateau for voltages higher than 250–300 V, exactly in the same way as the vertical leakage current. This is a further confirmation of the fact that within the plateau region, the voltage drop on the GaN buffer (and the corresponding vertical leakage current) is constant. In fact, the intensity of luminescence depends on current (directly proportional to the number of hot electrons) and on the average energy of electrons (which is determined by the electric field). In the plateau, current is fixed, and an increase in voltage between drain and substrate does not lead to an increase in luminescence. This is explained by considering that during the plateau, the voltage across the GaN buffer stops increasing, while a considerable voltage drop starts building up across the silicon substrate. The EL signal starts increasing again once the end of the plateau is reached, since vertical leakage starts flowing again through the structure.

C. Step-Stress Experiments: A V_{th} Shift is Observed in the Plateau Region

In Sections III-A and III-B, we have discussed the impact of substrate resistivity on breakdown voltage and vertical leakage of GaN-based transistors. In this section, we show that the use of a highly resistive substrate may result in additional trapping processes that are not present in wafers with a low resistivity substrate. To evaluate these aspects, we executed a set of four-terminal step-stress experiments. With source and gate grounded, the drain-to-substrate bias was increased by 20 V every 120 s, and the corresponding leakage current was measured. After each stage of the step-stress experiments, we carried out a full characterization of the electrical properties of the transistors, to identify the changes in the electrical properties induced by stress. Representative results obtained on wafers with different substrate resistivities are reported in Fig. 6. Fig. 6(a) reports the drain-to-substrate current measured during stress, while Fig. 6(b) reports the variation in threshold voltage induced by stress. The curve related to the wafer with a low-resistivity substrate [Fig. 6 (black line)] shows the lower

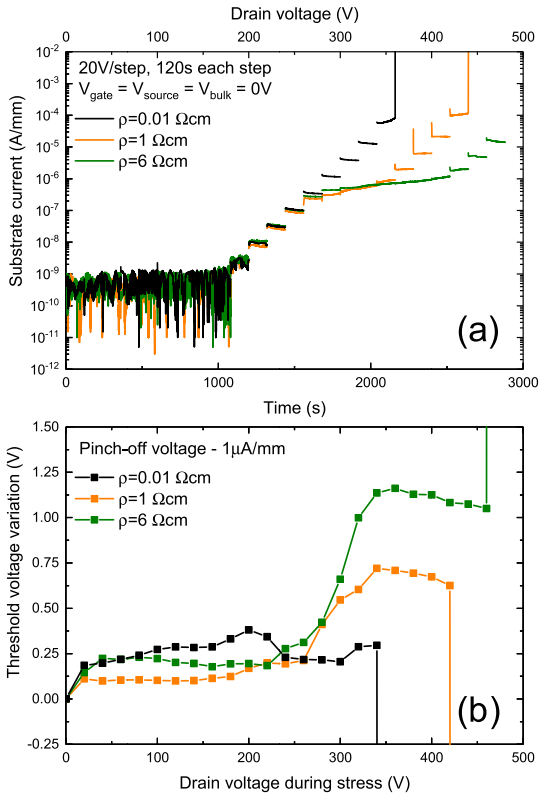

Fig. 6. Results of step-stress experiments carried out on wafers with different resistivities of the p-type silicon substrate. (a) Substrate current measured during the step-stress experiment. (b) Variation in threshold voltage induced by stress. A significant threshold voltage shift is observed only on the wafers with highly resistive substrate.

breakdown voltage (consistently with the results in Fig. 1), no plateau above 250 V, and no shift in threshold voltage after stress. On the other hand, the devices with resistive substrate show higher breakdown voltage, a significant plateau (i.e. a voltage range where the current is constant during stress), and a considerable shift in threshold voltage induced by stress.

Remarkably, the threshold variation occurs in correspondence of the plateau region [compare Fig. 6(a) and (b)]. Since we ascribed the plateau region to the depletion of the silicon/III-N-junction, we suggest that the depletion of Si substrate leads also to the threshold voltage variation. We can explain this as follows: for stress voltage V_{stress} smaller than the onset of the plateau V_{PL1}, the voltage drops mostly on the GaN buffer, due to the depletion of the uid-GaN/C-GaN junction. When V_{stress} is higher than the plateau onset V_{PL1}, the substrate starts depleting. As a consequence, the bottom of the buffer region moves to a positive potential, equal to $V_{stress}-V_{PL1}$. At the end of each stage of the step-stress experiment, the stress bias is removed, and the drain goes back to zero. Both junctions (silicon/III-N and uid-GaN/C-GaN) are depleted: the uid-GaN/C-GaN depletion region quickly recovers thanks to the high-carrier availability in the active region. On the contrary, in the nucleation/superlattice layers, the carrier's mobility is much lower due to the presence of several high-barrier heterojunctions. This causes a slow recovery (from the depletion) of the silicon/III-N-junction. It is worth noticing that during recovery, carrier supply may be provided

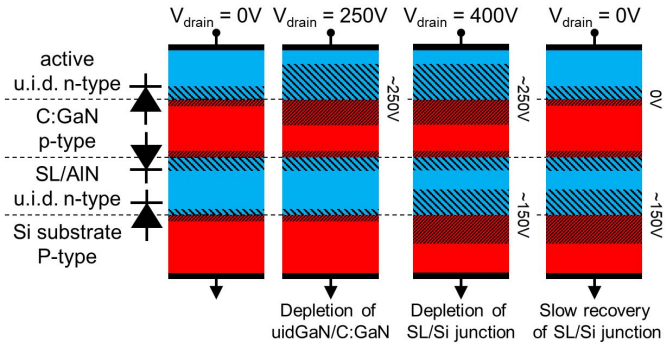

Fig. 7. Schematic of the vertical stack interfaces in OFF-state condition with different drain voltages. At V_{stress} = 250 V, the substrate starts depleting, and a space charge region is formed in the p-type substrate. For high-stress voltages (e.g., 400 V), a considerable voltage drop appears across the depleted region of the p-type substrate. When the drain bias is brought back to zero (rightmost frame), the depleted region in the substrate acts as a parallel plate capacitor and—temporarily—keeps the voltage at the bottom of the buffer at a positive value (around 100–200 V). Such positive backgating effect leads to a significant threshold voltage shift.

also by the silicon substrate, through the AlN layer. Due to the low vertical leakage through the AlN layer, the space charge region in the substrate acts as a parallel-plate capacitor, charged at the voltage $V_{stress}-V_{PL1}$ (in the range 100–200 V, depending on stress voltage). This means that when the drain bias goes to zero, the bottom of the buffer goes temporarily to a positive potential (around 100–200 V, depending on stress voltage). This brings to a positive voltage backgating effect, as shown schematically in Fig. 7. A positive backgating may induce a significant buffer trapping [16], since the C-GaN/uid-GaN diode (which behaves as a p-n junction) reaches a positive bias, and this leads to a significant electron injection to the C-doped buffer.

D. Positive Substrate Ramps Confirm the Hypothesis on Stress Mechanism

To confirm that a positive backgating can induce a significant charge trapping, we carried out a positive backgating ramp experiment. In this test, an HEMT is continuously biased in linear region, with a drain voltage of 1 V. At the same time, the substrate voltage is swept from 0 to 200 V and backward to 0 V, with a ramp rate of about 25 V/s. Ideally, in the absence of traps, a positive substrate bias would result in a slight and recoverable increase in 2-Dimensional electron gas (2DEG) density, and this is consistent with the blue line (upward sweep) in Fig. 8 (inset).

Remarkably, the results shown in Fig. 8 indicate that once a positive substrate potential higher than 150 V is reached, a significant charge trapping takes place. In fact, as the substrate bias returns to zero, drain current (and 2DEG resistivity) shows a strong decrease, which is ascribed to the trapping of electrons in the buffer. Such trapping is induced by the exposure to positive substrate (and buffer) potential. It is worth noticing that the three wafers with different substrates behave in the very same way.

Temperature-dependent analysis was carried out to extrapolate the activation energy of the defect filled by positive buffer potential. Specifically, we investigated the time constant

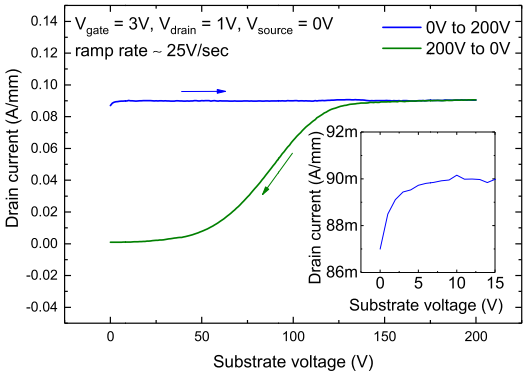

Fig. 8. Drain current dependence on a positive substrate voltage sweep. A significant drop in current (hysteresis) is observed during the downward sweep, due to the trapping of electrons in the buffer induced by the positive backgating potential. Inset: enlarged view of the drain current during the upward sweep.

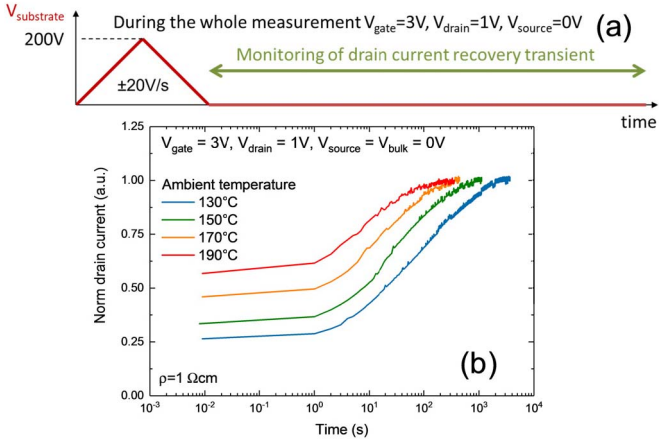

Fig. 9. (a) Schematic of the measurement: positive backgating ramps induce trapping effects within the vertical stack that reduces the drain current. After the positive backgating, the recovery of the current is monitored during the time. (b) Recovery of the drain current over the time after a positive backgating ramp has been measured at different ambient temperatures.

of the recovery from the trapped condition (induced by a positive substrate ramp up to 200 V, 25 V/s), as a function of temperature. The results are shown in Fig. 9, for one of the analyzed wafers. As can be noticed, once the positive substrate potential is removed, it takes a relatively long time (>10 s) for the 2DEG conductivity to recover to the pristine value. The recovery (detrapping) process is thermally activated, with an activation energy in the range 0.5–0.66 eV (Fig. 10). It is worth noticing that the three wafers with different substrate resistivities show a very similar behavior and Arrhenius plot (within process variability); this is consistent with the hypothesis that the charge trapping observed during positive backgating is related to buffer traps (which have—in a first order approximation—no dependence on substrate properties).

In Section III-C, we have demonstrated that a significant V_{th} shift is observed when the wafers with resistive substrate is stressed in the plateau region; we have ascribed this effect to the fact that when the drain bias is removed, the potential at the bottom of the buffer becomes temporarily positive (150–200 V), due to the depletion capacitance of the substrate. In Section III-D, we have demonstrated—by means of positive substrate ramps—that a positive back-bias can effectively lead to a significant buffer trapping. Now, we need to demonstrate

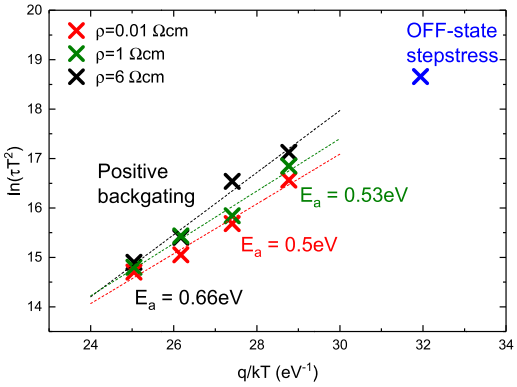

Fig. 10. Arrhenius plot of positive backgating and OFF-state recovery transients. The time constant of the trapping process induced by positive backgating and of the process induced by OFF-state stress are on the same Arrhenius plot, indicating the common physical origin.

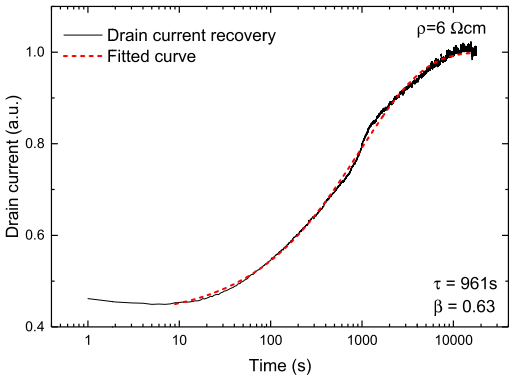

Fig. 11. Drain current recovery after a step stress up to 440 V. Once the sample was step stressed up to 440 V, the recovery of drain current (in the linear region) was monitored for several hours.

that the trap states filled during a step-stress experiment are the same, which are filled during a positive back-bias stress. To demonstrate this, we submitted a sample to a step-stress test; the final voltage was 440 V (well above V_{PL1}), in order to ensure a sufficient degradation and shift in V_{th}.

After reaching this trapping condition, both the substrate and source potentials were fixed at 0 V, and the transistor was biased in the linear region ($V_{GS} = 3$ V and $V_{DS} = 1$ V). The recovery of drain current (from the trapped condition to the fully recovered value) was measured (Fig. 11), and the related time constant was extrapolated by fitting the recovery transient with a stretched exponential function defined as $I = I_0 + A_0 \cdot \exp[-(t/\tau)^{\beta}]$ [17]. As shown in Fig. 10, the time constant of the recovery from step stress is perfectly aligned (in the Arrhenius) plot with the time constant of the recovery from positive backgating stress. This result supports the hypothesis on the role of positive buffer potential in the degradation of the devices: both OFF-state and positive backgating recoveries are driven by the same detrapping process. The band diagram in different bias conditions is shown in Fig. 12: zero-bias condition (a); plateau condition ($V_{DRAIN} > V_{PL1}$) (b); zero-bias after a drain bias higher than V_{PL1} is applied and substrate depletion occurs (c); and positive backgating bias (d). It is worth noticing that in Fig. 12(c) and (d), the band condition of the active/buffer junction is very similar, and the injection of electrons from the active region (n-type) to the buffer can occur easily.

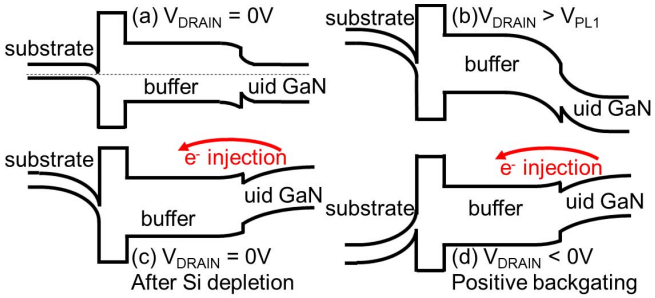

Fig. 12. Band diagrams of the vertical stack in different bias conditions. Charge injection from the active region to the buffer has been highlighted. (a) Zero-bias condition. (b) Plateau condition ($V_{DRAIN} > V_{PL1}$). (c) Zero bias after a drain bias higher than V_{PL1} is applied and substrate depletion occurs. (d) Positive backgating bias.

IV. Conclusion

With this paper, we have investigated and described for the first time the impact of the substrate resistivity on the breakdown voltage and trapping characteristics of GaN-based power transistors. We demonstrate that—thanks to the presence of a plateau region in the vertical I–V curves—the wafers with higher silicon resistivity show the highest breakdown voltage. The existence of the plateau is ascribed to the build-up of a depleted region in the silicon substrate, which takes part of the drain–source voltage difference thus limiting the voltage drop on the GaN buffer stack. In the second part of this paper, we demonstrate that the wafers with high substrate resistivity suffer from additional trapping effects with respect to those with low resistivity. A significant threshold voltage shift is observed when the devices are stressed in the plateau region. Such shift is ascribed to the fact that—at high drain voltages—a considerable voltage drop (in the range 150–200 V) falls on the depleted Si substrate. Once the stress bias is removed, such voltage drop leads to positive backgating effects which, in turn, results in the injection of electrons toward the buffer. By monitoring the drain current recovery after a positive backgating bias is applied on the substrate, we demonstrate that the origin of the V_{th} shift observed during step stress is the same as in positive backgating, and we provide information on the properties of the related traps. As a general conclusion, we can state that the use of highly resistive substrate can improve the breakdown robustness; however, this happens at the expense of the V_{th} stability. A tradeoff must be considered, if resistive substrates are used for fabricating GaN power transistors.

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