Charge-based Model for Junction FETs

Farzan Jazaeri, Nikolaos Makris, Ali Saeidi, Matthias Bucher, and Jean-Michel Sallese

***Abstract*— We present a unified charge-based model for double-gate and cylindrical architectures of junction field-effect transistors (JFETs). The central concept is to consider the JFET as a junctionless FET (JLFET) with an infinitely thin insulating layer, leading to analytical expressions between charge densities, current, and voltages without any fitting parameters. Assessment of the model with numerical technology computer-aided design simulations confirms that holding the JFET as a special case of the JLFET is justified in all the regions of operation, i.e., from deep depletion to flat-band and from linear to saturation.**

***Index Terms*— Cylindrical gate all around junction field-effect transistor (JFET), double-gate FETs, nanowire FETs, power semiconductor FETs, radiation-hard electronics, vertical JFET (V-JFET).**

I. Introduction

THE junction field-effect transistor (JFET, also called the junction unipolar gate FET) is the first field-effect device which has been produced before the MOSFET hegemony. Even though the JFETs are mainly used in specific low-noise solutions, actually there is a growing interest for using these devices in power electronics with new architectures and new materials (SiC, for instance). Recently, a silicon-based vertical JFET (V-JFET) switch, consisting in arrays of cylindrical JFETs (CJFETs) connected in parallel, was designed and fabricated at Instituto de Microelectrónica de Barcelona-Centro Nacional de Microelectrónica [1] for the inner tracker of the future high luminosity upgrade of the ATLAS [1]. Due to their excellent electrical properties, i.e., high voltage capability and high immunity in terms of ionization induced damages, these devices can be used as switches for high-voltage powering [1]. Since defects in the gate oxide and at the semiconductor/oxide interfaces were identified as major issues for MOSFET's radiation damages, oxide-free V-JFET devices are expected to tolerate higher total ionizing doses. Recently, V-JFETs confirmed these higher performances in terms of forward current, transfer characteristics, and leakage currents [1], [2].

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However, even though JFETs have been used in discrete electronics, physics-based compact models are still quite conservative and deal with the so-called full depletion approximation where the crude deep depletion regime is enhanced with smoothing functions [3]–[6]. For instance, Sansen and Das [4] adopted a MOSFET like approach to interpolate the subthreshold, quadratic and linear modes of operation. Semiempirical log-exponential functions were introduced to ensure a smooth transition across the pinchoff domain [4], a technique also used in [7] and [8].

In this derivation, we propose a unified charge-based model for double-gate and CJFETs. The central idea is to *consider the JFET as a junctionless FET (JLFET) [9] with a negligible insulating layer*, i.e., a JLFET with an *infinite gate capacitance*, a very valid assumption since the doping density of the gates is much higher than the channel counter doping. Next, the intimate correspondence which has been demonstrated between double-gate and gate-all-around (GAA) JLFET topologies [10] will be used to simulate CJFETs with equivalent parameters (to the best of the author's knowledge, no analytical model exists for CJFETs). Therefore, as for the JLFET [10], [11], the physics-based model for JFET will cover all the regions of operation, excluding accumulation which is not compatible with the forward biasing of the gate-to-channel p-n junctions.

The core model will be validated for an ideal long channel CJFET, thus ignoring short channel effects that can be introduced in the future developments.

II. Device Structure and Principle Operation of the Junction FETs

The 3-D geometry of the V-JFET and double-gate JFETs are depicted in Figs. 1 and 2, respectively. The V-JFET, conceived as a cellular device transistor, is composed of several thousands of parallel cells in a high-resistivity substrate, allowing the transistor to drive high currents. Based on a 3-D architecture, a circular silicon channel is surrounded by a doped silicon gate. The current, between the source at the top and the drain at the backside of the cells, flows through a lightly doped channel whose effective width is controlled by the depleted regions induced by the gate. Each cell can be considered as a conventional individual CJFET in series with an access resistance from the low doped substrate.

Alike the JLFET biased below the flat-band, the JFET operates in depletion and the current flows in the volume, not at the interface. Similar to the JLFET [9], the JFET has no source and drain p-n junction. However, a major difference exists between these two devices, whereas the JLFET has an

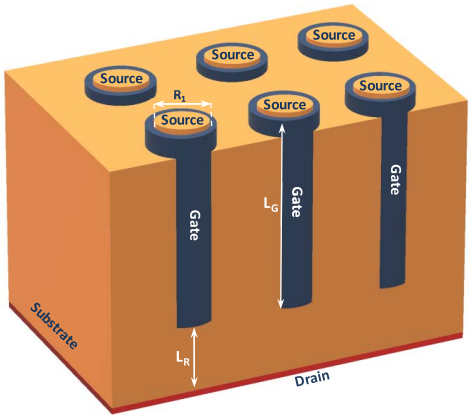

Fig. 1. Schematic view of an n-type V-JFET made of individual CJFETs built in a common substrate.

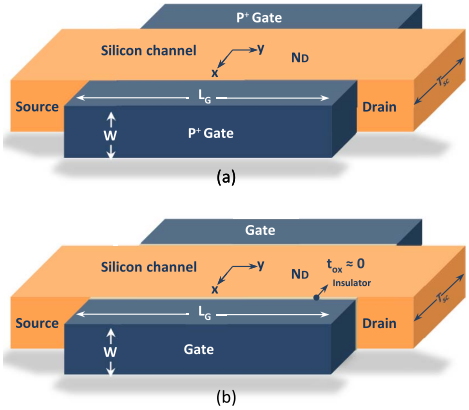

Fig. 2. Schematic view of (a) n-type double-gate JFET and its equivalent (b) n-type double-gate JLFET with an infinite oxide capacitance.

insulating layer between the channel and the gate electrode; in JFETs, this role is accounted by a reverse biased gate-to-channel p-n junction (the gate is highly doped with respect to the channel to minimize the charge depletion into the gate). The JFET is usually in ON-state at $V_{GS} = 0$ and, in case of an n-channel, a negative V_{GS} bias depletes the channel and modulates the conductance. The way the charge-based model developed in [10] and [11] for the double-gate and cylindrical JLFETs can be mapped on the JFET model is now detailed.

III. Junction FET: A Junctionless FET With an Infinite Gate Capacitance

A. Mobile Charges in Symmetric Double-Gate JFETs

Fig. 2 is a schematic of an n-type doped long channel double-gate (a) JFET and (b) JLFET. To develop a physics-based model for the mobile charge density in double-gate JFETs, first, we rely on the analytical expression for the charge density in JLFET stated in [11], but now imposing $t_{ox} \approx 0$. The reason why this "trick" holds is justified as follows. Assuming the full-depletion approximation across the gate-to-channel junction in the JFET, the charge neutrality imposes $qX_G N_G = qX_{ch} N_D$, where X_G and X_{ch} are, respectively, the "fully depleted" widths in the gate and channel regions. These are given by $X_G = (2\varepsilon_{si}\psi_G/qN_G)^{1/2}$ and $X_{ch} = (2\varepsilon_{si}\psi_{ch}/qN_D)^{1/2}$, where ψ_G and ψ_{ch} are the potentials drop in the p-type gate and the n-type channel, respectively. Combining these relations, we obtain $\psi_G/\psi_{ch} = N_D/N_G$. Therefore, when the doping of the gate is much higher than the channel doping, the potential drop "inside" the gate can be neglected with respect to the potential drop "inside" the channel. In other words, any variation in the gate potential is almost entirely transferred to the channel, with negligible potential drop in the gate electrode, i.e., $\delta\psi_s \approx \delta V_{GS}$. From a modeling point of view, this is satisfied when assigning C_{ox} to "infinity" for the gate insulator of a virtual JLFET. When the whole channel operates in depletion, the gate channel p-n junction should be reversely biased in order to avoid the gate leakage current which in forward bias increases exponentially with the gate-channel bias, and therefore, the gate-to-source voltage must satisfy $V_{GS} < 0$.

Here, we recall the link between the channel charge density and potentials for JLFETs operating in depletion mode [11]

$$V_{GS} - V_{ch} - \Delta\phi_{ms} - U_T \ln\left(\frac{N_D}{n_i}\right) \overset{dep}{\approx} -\frac{Q_{sc}^2}{8qN_D\varepsilon_{si}} - \frac{Q_{sc}}{2C_{ox}} + U_T \ln\left[1 - \left(\frac{Q_{sc}}{Q_{fix}}\right)^2\right], \quad (1)$$

where Q_{sc} is the total charge density composed of mobile, Q_m, and fixed, $Q_{fix} = qN_D T_{sc}$, charges densities and is given by $Q_{sc} = Q_{fix} + Q_m$ and $\Delta\phi_{ms}$ is the difference between work function of the metal and the intrinsic Fermi level of the semiconductor. In case of JFET, the metal gate of the JLFET is replaced with a highly doped semiconductor and $\Delta\phi_{ms} = U_T \ln(N_G/n_i)$. Here, n_i and U_T are, respectively, the intrinsic carrier density and the thermal voltage. The term V_{ch} is the shift in the electron quasi Fermi potential (the Fermi energy at the source is the reference), T_{sc} is the silicon channel thickness, and ε_{si} is the silicon permittivity. Since the JFET can be viewed as a JLFET with an infinite gate capacitance, the charge-potential relationship based on relation (1) is readily obtained

$$V_{GS} - V_{ch} - V_{bi} \overset{dep}{\approx} \frac{-Q_{sc}^2}{8qN_D\varepsilon_{si}} + U_T \ln\left[1 - \left(\frac{Q_{sc}}{Q_{fix}}\right)^2\right], \quad (2)$$

where V_{bi} is given as

$$V_{bi} = \Delta\phi_{ms} + U_T \ln\left(\frac{N_D}{n_i}\right) = U_T \ln\left(\frac{N_G N_D}{n_i^2}\right). \quad (3)$$

Neglecting the logarithmic term in relation (2) when the mobile charge density tends to zero gives the pinchoff voltage in JFETs

$$V_P = -\frac{qT_{sc}^2 N_D}{8\varepsilon_{si}} = -\frac{Q_{fix}}{8C_{si}}, \quad (4)$$

where $C_{si} = \varepsilon_{si}/T_{si}$.

Defining the threshold voltage as the gate voltage where Q_m tends to zero (at $V_{DS} = 0$) while using the same reasoning as for the pinchoff voltage definition in (2), i.e., neglecting the logarithmic dependence, gives

$$V_{TH} = V_{bi} + V_P. \quad (5)$$

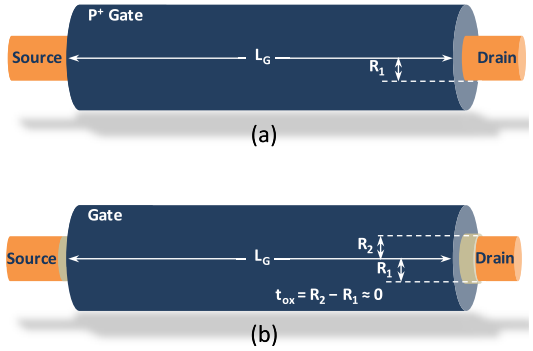

Fig. 3. Schematic view of (a) n-type CJFET and its equivalent (b) n-type GAA JLFET with an infinite oxide capacitance.

It is worth noting that ideally in a JLFET, the doping of the channel is similar to that of drain and source (note that for a lightly doped channel, the source and drain regions are still reasonably heavily doped to provide a low access resistance. This leads to a built-in potential at source/channel and drain/channel junctions which could be accounted in $V_{\rm bi}$ but will not be addressed in this paper).

B. Channel Current in Symmetric Double-Gate JFETs

The total electron current density is obtained by adding the diffusion and drift contributions. The current, thus, is given as

$$I_{\rm DS} = -W\mu Q_m \frac{dV_{\rm ch}}{dx} = \frac{W}{L_G}\mu \int_0^{V_{\rm DS}} (qN_D T_{\rm sc} - Q_{\rm sc}) dV_{\rm ch}$$
$$= \frac{W}{L_G}\mu q N_D T_{\rm sc} V_{\rm DS} - \frac{W}{L_G}\mu \int_0^{V_{\rm DS}} Q_{\rm sc} dV_{\rm ch}, \quad (6)$$

where μ is the free electron mobility (assumed constant) [12], W and L_G are, respectively, the width and gate length of the channel, and $Q_{\rm sc}dV_{\rm ch}$ is obtained from the junctionless double-gate FET in depletion mode by letting $C_{\rm ox}$ become infinite

$$Q_{\rm sc}dV_{\rm ch} \overset{\rm dep}{\approx} \left[\frac{Q_{\rm sc}^2}{4qN_D\varepsilon_{\rm si}} + \frac{2U_T\left(\frac{Q_{\rm sc}}{qN_D T_{\rm sc}}\right)^2}{1-\left(\frac{Q_{\rm sc}}{qN_D T_{\rm sc}}\right)^2}\right] dQ_{\rm sc}. \quad (7)$$

Similar to the JLFETs in depletion mode, the drain current is obtained from

$$I_{\rm DS} = \frac{W\mu}{L_G} f(Q_m)\Big|_S^D = \frac{W\mu}{L_G}[f(Q_{m,d}) - f(Q_{m,s})], \quad (8)$$

where

$$f(Q_m) = -\frac{Q_m^3}{12qN_D\varepsilon_{\rm si}} - \frac{Q_m^2}{8C_{\rm si}} + 2U_T Q_m$$
$$- 2U_T Q_{\rm fix} \ln(Q_m + 2Q_{\rm fix}). \quad (9)$$

C. Approximate Expressions for Charges in GAA JFETs: Equivalence Between Planar and Cylindrical Shapes

Following the idea that double-gate and GAA JLFET architectures can share a common model (see [10]), a unified charge-based model for the CJFET can also be derived from the GAA JLFET model (quantum mechanical corrections are ignored for channel thicknesses greater than 10 nm [13]–[15]). A typical GAA JLFET is shown in Fig. 3.

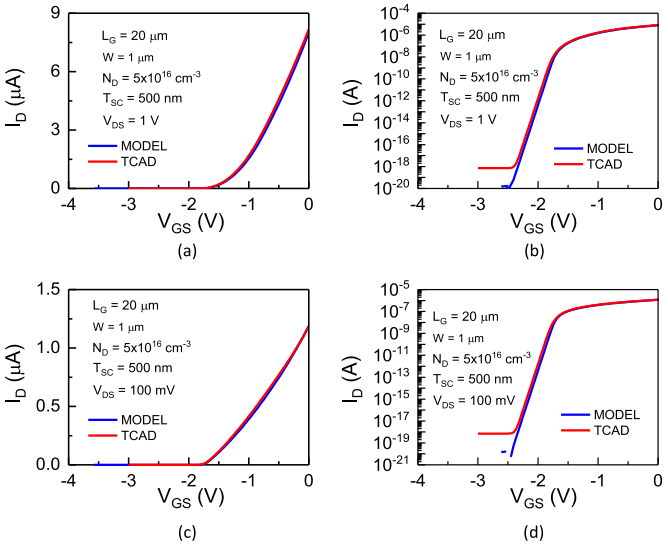

Fig. 4. Drain to source current versus the gate voltage in linear and saturation modes of operation in both linear and logarithmic scales for double-gate JFETs ($L_G = 20\ \mu$m, $W = 1\ \mu$m, $N_D = 5 \times 10^{16}$ cm^{-3}, and $T_{\rm sc}$ = 500 nm).

Here, L_G and $t_{\rm ox} = R_2 - R_1$ represent the gate length and the gate oxide thickness; R_1 and N_D are the semiconductor radius and the channel dopant density. As proposed in [10], similarities between charge–voltage relationships in double-gate and GAA JLFETs enables to use the same approach to model the electrical characteristics of CJFETs. As stated in [10], the main relationships derived for the planar double-gate JFET can be used to obtain the mobile charge density in CJFET, for which to the best of our knowledge, no analytical model has been developed so far.

For sake of clarity, the equivalent double-gate model parameters for cylindrical gate all around JFETs are recalled in Table I.

D. Derivation of the Channel Current in CJFETs

Since the mobile charge density given by (2) represents the mobile carrier concentration per unit "projected" surface in the double-gate picture, half of the CJFET perimeter ($W^{\rm Eq-DG} = \pi R$) will represent the equivalent width of the double gate. Then, the current reads

$$I_{\rm DS} = -W^{\rm Eq-DG}\mu Q_m \frac{dV_{\rm ch}}{dx}. \quad (10)$$

Integrating from source to drain making use of the definitions of the equivalent parameters listed in Table I, the current can be calculated, which is formally the same as in (9) for the double-gate counterpart.

IV. Results and Discussion

To illustrate and appraise the validity of the proposed approach, the drain current characteristics in an n-type double-gate JFET ($L_G = 20\ \mu$m and $W = 1\ \mu$m) obtained with technology computer-aided design (TCAD) simulations and the model are plotted in Fig. 4 (short channel effects are ignored and a constant carrier mobility is used).

TABLE I
CORRESPONDENCE BETWEEN GAA JUNCTIONLESS PHYSICAL PARAMETERS AND EQUIVALENT JUNCTIONLESS DOUBLE-GATE FET MODEL PARAMETERS

Physical parameters	Nanowire	Equivalent DG MOSFET
Radius and thickness	R (radius)	$T_{sc} = 2 \times R$
Width	–	$W = \pi \times R$
Doping concentration	N_D	$N_D/2$
Intrinsic carrier conc.	n_i	$n_i/2$

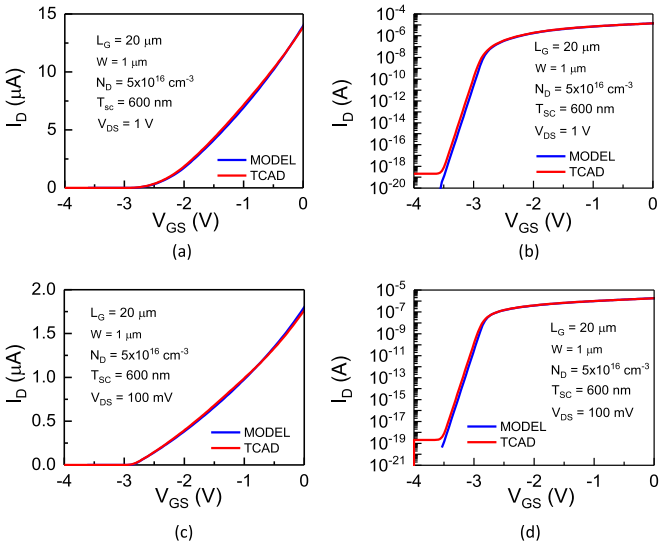

Fig. 5. Drain to source current versus the gate voltage in linear and saturation modes of operation in both linear and logarithmic scales for double-gate JFETs ($L_G = 20$ μm, $W = 1$ μm, $N_D = 5 \times 10^{16}$ cm^{-3}, and $T_{SC} = 600$ nm).

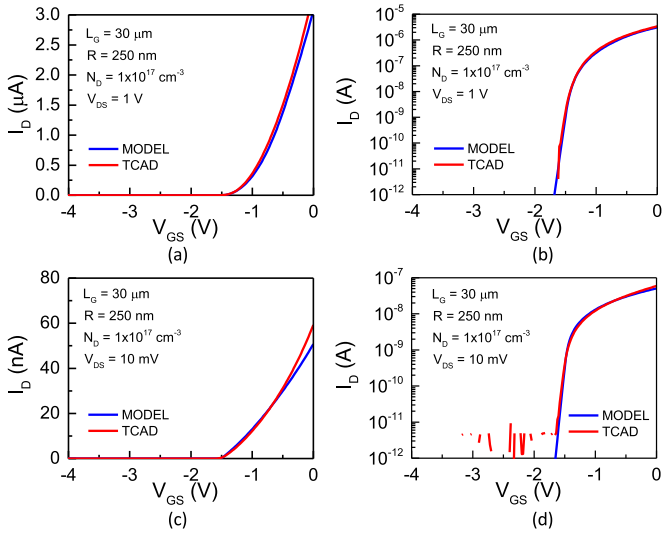

Fig. 6. Drain to source current versus gate voltage in linear and saturation modes of operation in both linear and logarithmic scales for a CJFET with $L_G = 30$ m, $R = 250$ nm, and $N_D = 10^{17}$ cm^{-3}.

Fig. 4 depicts the channel current versus the gate voltage for a 500-nm silicon thickness doped at $N_D = 5 \times 10^{16}$ cm^{-3} biased in saturation [$V_{DS} = 1$ V, Fig. 4(a) and (b)] and linear [$V_{DS} = 100$ mV, Fig. 4(c) and (d)] modes. The agreement between the numerical calculations and the model is quite good in linear and logarithmic scales. The same holds for a 600-nm silicon thickness device with $N_D = 5 \times 10^{16}$ cm^{-3} (see Fig. 5). It is worth noticing that the thicker channel exhibits quite pronounced quadratic current–voltage characteristics at low V_{DS}, which is a signature of the extended depletion taking place in wide channels. Considering now a n-type CJFETs with $N_D = 10^{17}$ cm^{-3}, $R = 250$ nm, and $L_G = 30$ μm, the current densities versus the effective gate voltage obtained from numerical (TCAD) simulations are plotted on Fig. 6 (red line) for $V_{DS} = 1$ V and $V_{DS} = 10$ mV.

The drain current characteristics obtained with the analytical model developed for the double-gate JFET structure using the equivalent parameters are also plotted (blue line) using the same set of parameters as for TCAD. Again, a good agreement is obtained for all operation modes, even though some slight mismatch is observed at low V_{DS} when the gate voltage is close to 0 V.

V. CONCLUSION

In this paper, an analytical charge-based model was developed for the double-gate and GAA JFETs by twinning them with JLFET architectures by means of an infinite gate insulator capacitance. The model is derived without the need to develop a new set of analytical relationships and is found to be valid in all the regions of operation, from deep depletion to flat-band and from linear to saturation, as confirmed by extensive comparison with TCAD numerical simulations. In addition, this equivalence should also hold for ac analysis [16], asymmetric operation [17], noise [18], and short channel effects, as developed for JLFETs.

REFERENCES

[1] P. Fernández-Martínez, D. Flores, S. Hidalgo, D. Quirion, R. Duraà, and M. Ullán, "First fabrication of a silicon vertical jfet for power distribution in high energy physics applications," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 877, pp. 269–277, Jan. 2018.

[2] E. G. Villani *et al.*, "Hvmux, a high voltage multiplexing for the atlas tracker upgrade," *J. Instrum.*, vol. 12, p. C01076, Jan. 2017.

[3] P. Lauritzen and O. Leistiko, "Field-effect transistors as low-noise amplifiers," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers.*, Feb. 1962, pp. 62–63.

[4] W. M. C. Sansen and C. J. M. Das, "A simple model of ion-implanted JFETs valid in both the quadratic and the subthreshold regions," *IEEE J. Solid-State Circuits*, vol. SSC-17, no. 4, pp. 658–666, Aug. 1982.

[5] W. W. Wong, J. J. Liou, and J. Prentice, "An improved junction field-effect transistor static model for integrated circuit simulation," *IEEE Trans. Electron Devices*, vol. 37, no. 7, pp. 1773–1775, Jul. 1990.

[6] W. W. Wong and J. J. Liou, "JFET circuit simulation using SPICE implemented with an improved model," *IEEE Trans. Comput.-Aided Design Integr.*, vol. 13, no. 1, pp. 105–109, Jan. 1994.

[7] H. Ding, J. J. Liou, K. Green, and C. R. Cirba, "A new model for four-terminal junction field-effect transistors," *Solid-State Electron.*, vol. 50, no. 3, p. 422–428, 2006.

[8] W. Wu, S. Banerjee, and K. Joardar, "A four-terminal JFET compact model for high-voltage power applications," in *Proc. Int. Conf. Microelectron. Test Struct.*, Mar. 2015, pp. 37–41.

[9] J.-P. Colinge *et al.*, "Nanowire transistors without junctions," *Nature Nanotechnol.*, vol. 5, pp. 225–229, Mar. 2010.

[10] J.-M. Sallese, F. Jazaeri, L. Barbut, N. Chevillon, and A. Lallement, "A common core model for junctionless nanowires and symmetric double-gate FETs," *IEEE Trans. Electron Devices*, vol. 60, no. 12, pp. 4277–4280, Dec. 2013.

[11] J.-M. Sallese, N. Chevillon, C. Lallement, B. Iniguez, and F. Pregaldiny, "Charge-based modeling of junctionless double-gate field effect transistors," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2628–2637, Aug. 2011.
[12] F. Jazaeri and J.-M. Sallese, "Carrier mobility extraction methodology in junctionless and inversion-mode fets," *IEEE Trans. Electron Devices*, vol. 62, no. 10, pp. 3373–3378, Oct. 2015.
[13] Y. Omura, S. Horiguchi, M. Tabe, and K. Kishi, "Quantum-mechanical effects on the threshold voltage of ultrathin-SOI nMOSFETs," *IEEE Electron Device Lett.*, vol. 14, no. 12, pp. 569–571, Dec. 1993.
[14] D. Munteanu, J.-L. Autran, X. Loussier, S. Harrison, R. Cerutti, and T. Skotnickit, "Quantum short-channel compact modeling of drain-current in double-gate MOSFET," in *Proc. 35th Eur. Solid-State Device Research Conf.*, vol. 50, Sep. 2006, pp. 137–140.
[15] J.-P. Colinge, "Multiple-gate SOI MOSFETs," *Solid-State Electron.*, vol. 48, no. 6, pp. 897–905, Jun. 2004.
[16] F. Jazaeri, L. Barbut, and J.-M. Sallese, "Trans-capacitance modeling in junctionless symmetric double-gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 60, no. 12, pp. 4034–4040, Dec. 2013.
[17] F. Jazaeri, L. Barbut, and J. M. Sallese, "Modeling asymmetric operation in double-gate junctionless FETs by means of symmetric devices," *IEEE Trans. Electron Devices*, vol. 61, no. 12, pp. 3962–3970, Dec. 2014.
[18] F. Jazaeri and J. M. Sallese, "Modeling channel thermal noise and induced gate noise in junctionless fets," *IEEE Trans. Electron Devices*, vol. 62, no. 8, pp. 2593–2597, Aug. 2015.

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