A Novel Variation of Lateral Doping Technique in SOI LDMOS With Circular Layout

Kemeng Yang, *Student Member, IEEE,* Yufeng Guo, *Member, IEEE,* David Z. Pan, *Fellow, IEEE,* Jun Zhang, *Student Member, IEEE,* Man Li, Yi Tong, Lin He, and Jiafei Yao, *Member, IEEE*

***Abstract*— The breakdown characteristics of a practical silicon-on-insulator (SOI) lateral power device are generally limited by the 3-D curvature effect induced by its circular layout. The Conventional 2-D design methods such as 2-D variation of lateral doping (VLD) technique cannot derive optimal device parameters. In this paper, for the first time, a 3-D VLD technique is proposed to suppress the 3-D curvature effect in the lateral power device with circular layout. The 3-D Poisson equation is solved to formulate the optimized doping profile. TCAD tools are employed to verify the model and explore the physic insight. By adding an inversely proportional doping profile onto the conventional linear doping profile, the analytical and numerical results show that the uniform electric field in the drift region and maximized breakdown voltage (BV) are obtained for the SOI lateral double-diffused metal–oxide–semiconductor with circular layout. Furthermore, compared to the 2-D VLD device, the proposed 3-D VLD technique also contributes to excellent on-state characteristics, including the high on-state BV, reduced specific on-resistance, large saturation current, suppressed quasi-saturation effect, improved transconductance, and thus a large Baliga's figure of merits (BFOM).**

***Index Terms*— 3-D variation of lateral doping (VLD), breakdown voltage (BV), circular layout, electric field, Baliga's figure of merits (BFOM), specific on-resistance ($R_{on,sp}$).**

I. Introduction

VARIATION of lateral doping (VLD) technique is the most mature and commercialized technique for evening the surface electric field and maximizing the lateral breakdown voltage (BV) in the lateral power device [1]–[4]. In 1991, linear doping profile first proves to be able to obtain a uniform electric field in theory and is implemented in a silicon-on insulator (SOI) device [2]. Until now, the linear doping profile has been used in various SOI power devices as one of most effective way to achieve a high BV [5]–[7]. The linear doping profile technology is derived based on the 2-D theory [1]. However, the power device, especial in high-power application, is always designed and fabricated by the circular, runway, or multifinger layout [8]–[11]. Electric field crowding always occurs at the small radius region in the real lateral power devices due to the 3-D curvature effect [12]. Many experimental results show the peak of electric field in the 3-D power device leads to a much lower BV, which will surely become severe with the continuous decrease of the device dimensions [12]–[15]. That is one of the most important reason why the linear doping profile based on 2-D theory usually overestimated the breakdown performance of real 3-D structure of SOI lateral power device.

In this paper, based on solving 3-D Poison equation, an inversely proportional doping profile is added to the conventional linear doping profile to uniform the lateral electric field in the drift region of SOI lateral double-diffused metal–oxide–semiconductor (LDMOS). As a result, the 3-D curvature effect due to the layout is entirely diminished and the BV is maximized. Furthermore, LDMOS with the novel drift doping profile also exhibits the improved ON-state performances, including the high ON-state BV, reduced specific on-resistance ($R_{on,sp}$), large saturation current, diminished quasi-saturation effect, improved transconductance (g_m), and thus a large Baliga's figure of merits (BFOM).

II. 3-D Variation of Lateral Doping

As the 3-D effect of circular layout causes the crowding of the lateral electric field, the optimization of electric field is critical in the circular layout. The cross section of the SOI LDMOS cell for modeling and simulation is shown in Fig. 1. As shown in Fig. 1(a), the r-axis of the cylindrical coordinate system is the radius of the drift region, and the y-axis is the axis of the cylinder. The origin of the cylindrical coordinate system is the center of the circle which is at the surface of the top Si layer. r_d and r_c are the radius of the drain region and the drift region, respectively. L_d is the length of the drift region. $N_{3-D}(r)$ is the doping concentration of the drift region. t_s and t_{ox} are the thicknesses of the drift region and buried oxide, respectively.

Manuscript received December 4, 2017; revised January 30, 2018; accepted February 16, 2018. Date of publication March 6, 2018; date of current version March 22, 2018. This work was supported in part by the National Natural Science Foundation of China under Grant 61574081 and Grant 61704084 and in part by the Graduate Students Research Innovation Program of Jiangsu Province under Grant KYLX16_0649. The review of this paper was arranged by Editor F. Udrea. *(Corresponding author: Yufeng Guo.)*

K. Yang, Y. Guo, J. Zhang, M. Li, Y. Tong, L. He, and J. Yao are with the College of Electronic and Optical Engineering and College of Microelectronics, Nanjing University of Posts and Telecommunications, Nanjing 210023, China, and also with the National & Local Joint Engineering Laboratory for RF Integration and Micro-Packaging Technologies, Nanjing University of Posts and Telecommunications, Nanjing 210023, China (e-mail: yfguo@njupt.edu.cn).

D. Z. Pan is with the College of Electronic and Optical Engineering and College of Microelectronics, Nanjing University of Posts and Telecommunications, Nanjing 210023, China, with the National & Local Joint Engineering Laboratory for RF Integration and Micro-Packaging Technologies, Nanjing University of Posts and Telecommunications, Nanjing 210023, China, and also with the Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, TX 78712 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2018.2808193

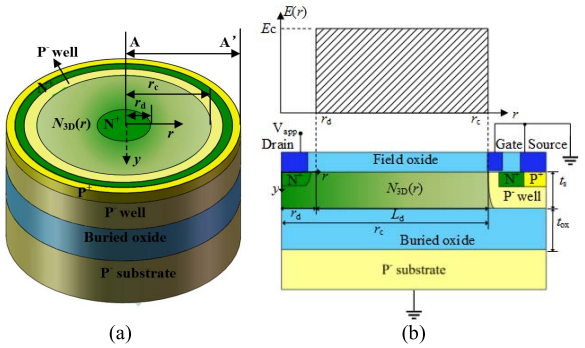

Fig. 1. SOI LDMOS cell with a circular layout. (a) 3-D cell of the device. (b) Cross section along the A–A' direction.

At a given reversed biased voltage V_{app}, the drift region is fully depleted and a differential equation that describes the surface electric potential $\varphi(r,0)$ in silicon film can be given by [15]

$$\frac{\partial^2\varphi(r,0)}{\partial r^2}+\frac{1}{r}\frac{\partial\varphi(r,0)}{\partial r}-\frac{\varphi(r,0)}{t^2}=-\frac{qN_{3D}(r)}{\varepsilon_s} \tag{1}$$

where q is the electronic charge, $t=(0.5t_s^2+t_st_{ox}\varepsilon_s/\varepsilon_{ox})^{0.5}$ is the characteristic thickness, ε_s and ε_{ox} are the dielectric constant of silicon and silicon dioxide material, respectively. In the ideal case, the surface electric field is a constant, the critical electric field of silicon E_C, when the lateral breakdown occurs. According to the assumption that $E(r)=E_C$, we can obtain

$$\frac{\partial^2\varphi(r,0)}{\partial r^2}=0,\quad \frac{\partial\varphi(r,0)}{\partial r}=-E_C,\ \ \varphi(r,0)=E_c(r_c-r). \tag{2}$$

Thus, by submitting (2) and the boundary conditions ($\varphi(r_d,0)=V_{app}$, $\varphi(r_c,0)=0$) into (1), a novel lateral doping profile considering the 3-D curvature effect is derived

$$N_{3D}(r)=N_{2D}(r)+N_{ADD}(r) \tag{3}$$

$$N_{2D}(r)=\frac{E_C\varepsilon_s}{qt}\times\frac{(r_C-r)}{t} \tag{4}$$

$$N_{ADD}(r)=\frac{E_C\varepsilon_s}{q}\times\frac{1}{r}. \tag{5}$$

Equations (4) and (5) are 2-D and 3-D components of the novel lateral doping profile. The 2-D component is the conventional linear doping profile, and the 3-D component is an additional an inversely proportional doping profile in which the factor of $1/r$ indicates the impact of the device cell shapes. Fig. 2 gives a specific case of 2-D/3-D VLD profiles based on (3). It illustrates that the doping concentration close to the drain side increases obviously with the reduction of the radius of the drain region. That indicates the small drain region brings an enhanced curvature effect, which has to be compensated by an additional impurity implant in the drift region. The higher doping concentration at the drain side generates more impurity centers with positive charge after ionizing. The direction of electric field caused by these positive impurity centers is opposite of the total electric field direction in the drift region. Thus, the N_{ADD} contributes to decrease the electric field at drain side and suppress the electric field crowding. When r_d tends to infinity, (3) reduces to (4) which is in accordance with the conventional VLD [2]. That means that the 3-D effect of circular layout can be neglected for a large drain region. In other words, the conventional 2-D VLD profile can be treated as the 3-D VLD profile when the drain region is large enough.

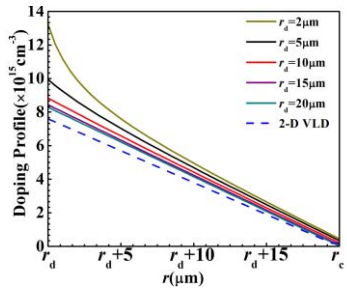

Fig. 2. Doping profile in the drift region of 3-D VLD LDMOS with various radii of the drain region ($t_S=3$ μm, $t_{ox}=3$ μm, and $L_d=20$ μm).

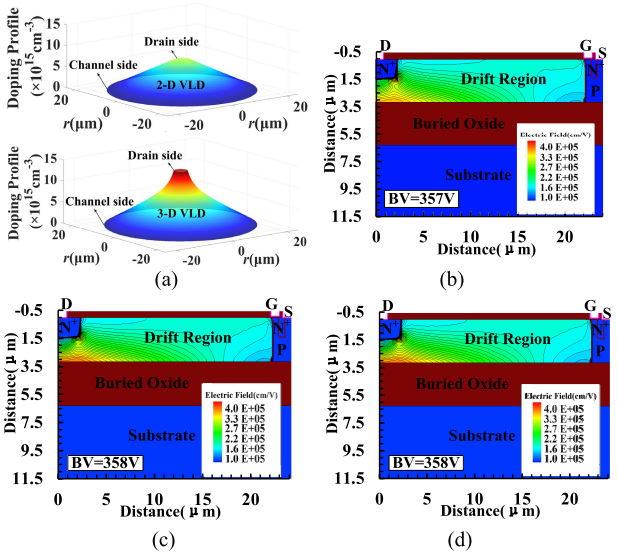

Fig. 3. Comparison of the lateral doping profile and electric field distribution in the drift region for 3-D/2-D VLD LDMOS ($r_d=2$ μm, $t_S=3$ μm, $t_{ox}=3$ μm, and $L_d=20$ μm). (a) Optimized lateral doping profile. (b) Electric field contours of 2-D VLD LDMOS using 2-D simulation (neglecting the curvature effect). (c) Electric field contours of 2-D VLD LDMOS using 3-D simulation (considering the curvature effect). (d) Electric field contours of 3-D VLD LDMOS using 3-D simulation (considering the curvature effect).

III. Breakdown Characteristics

MEDICI, a synopsys TCAD tool, is employed to study the characteristics of the proposed 3-D/2-D VLD LDMOS. The simulation models used in MEDICI are CONSRH, AUGER, BGN, FLDMOB, IMPACT I, and CCSMOB. The optimal lateral doping profiles based on (3)–(5) are shown in Fig. 3(a), and the vertical doping profile is uniform. Fig. 3(b) illustrates the contour of electric field in the drift region of an optimized 2-D VLD LDMOS according to (4) and Fig. 3(a) (top). The simulation is implemented in the rectangle coordinate for avoiding the curvature effect. Few electric field contours in

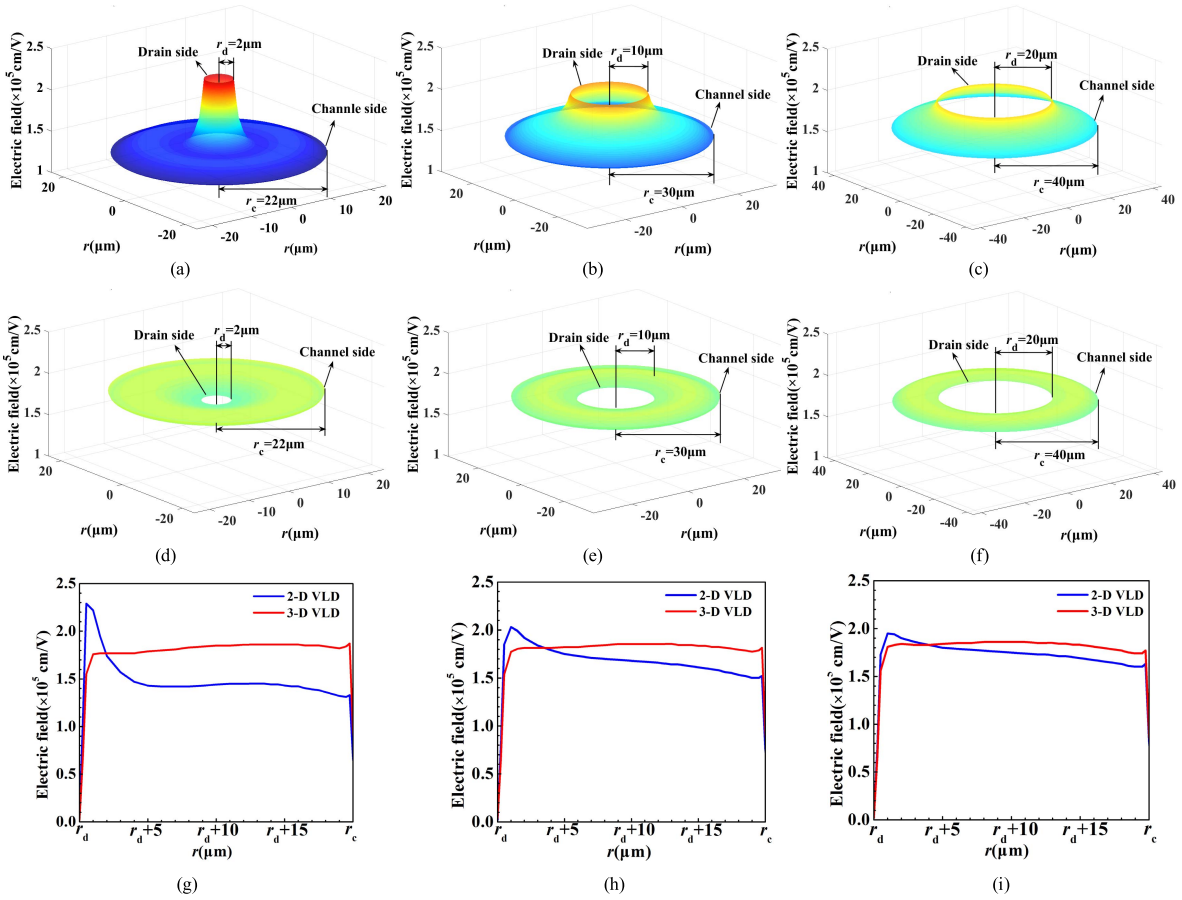

Fig. 4. Surface electric field at breakdown for the 2-D VLD LDMOS with circular layout (a) $r_d = 2$ μm, (b) $r_d = 10$ μm, and (c) $r_d = 20$ μm and 3-D VLD LDMOS with circular layout (d) $r_d = 2$ μm, (e) $r_d = 10$ μm, and (f) $r_d = 20$ μm. Surface electric field at breakdown along the r-axis for 2-D/3-D VLD LDMOS with circular layout (g) $r_d = 2$ μm, (h) $r_d = 10$ μm, and (i) $r_d = 20$ μm ($t_s = 3$ μm, $t_{ox} = 3$ μm, and $L_d = 20$ μm).

the drift in Fig. 3(b) indicate a uniform surface electric field is obtained. However, when the numerical simulation is done in the cylinder coordinate for the same device and the effect of circular layout is considered, Fig. 3(c) shows that the electric field strongly crowds at n^+n-junction. BV decreases by 18% (from 357 down to 294 V). In order to reduce the influence of the 3-D effect in circular layout, a novel lateral doping profile, namely, the 3-D VLD, is proposed according to (3), which is shown in Fig. 3(a) (bottom). The numerical simulation under a cylinder coordinate is performed for the LDMOS with the new lateral doping profile in the drift region. The contour of the electric field shown in Fig. 3(d) presents that the surface electric field remains uniform and the curvature effect fails to decrease the BV. Therefore, the proposed 3-D VLD technique deeply suppresses the curvature effect of circular layout in SOI LDMOS.

IV. Results and Discussion

A. Breakdown Voltage

To explore the breakdown mechanism of the proposed 3-D VLD lateral power device, the impact of circular layout radius on the breakdown performance of 3-D and 2-D VLD LDMOS are compared. The optimal doping profiles based on (3)–(5) for the simulated 2-D/3-D VLD LDMOS are shown in Fig. 2, and the vertical doping profile is uniform.

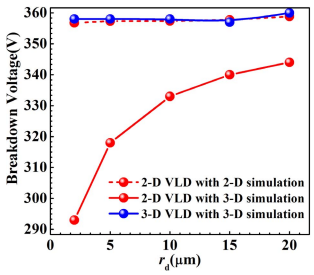

Fig. 5. BV of the 2-D and 3-D VLD SOI LDMOS ($t_s = 3$ μm, $t_{ox} = 3$ μm, and $L_d = 20$ μm).

Fig. 4 shows the surface electric field distribution when the circular LDMOS with 2-D VLD/3-D VLD profile break down. Fig. 4(a)–(c) shows that the shrinked drain region results in a serious electric field crowding at the drain side. However, as shown in Fig. 4(d)–(f), the additional drift doping profile leads to the unchanged uniform electric field regardless of the size of drain region in 3-D VLD devices. An intuitive comparison of surface electric field along the r-axis is also given in Fig. 4(g)–(i).

Fig. 5 compares the BV of 2-D VLD and 3-D VLD power device. When considering curvature effect in circular layout,

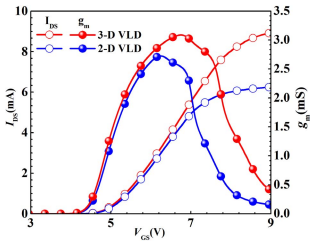

Fig. 6. Transfer and transconductance characteristics of 2-D VLD LDMOS and 3-D VLD LDMOS with circular layout (V_{DS} = 40 V and r_d = 2 μm).

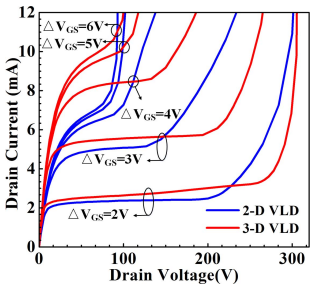

Fig. 7. Output characteristics of 2-D and 3-D VLD LDMOS with circular layout (r_d = 2 μm, t_s = 3 μm, t_{ox} = 3 μm, L_d = 20 μm, and $\Delta V_{GS} = V_{GS} - V_{th}$).

the BV of 2-D VLD LDMOS decreases with the reduced drain region due to deterioration of the electric field. However, the BV of 3-D VLD LDMOS equals to the optimal BV regardless of the size of drain region. This reveals the proposed doping profile of 3-D VLD LDMOS could improve the BV and thus weaken the influence of curvature effect.

B. On-State Characteristics

Fig. 6 gives the transfer and transconductance characteristics of the 2-D and 3-D VLD LDMOS with circular layout. Compared to 2-D device, the proposed 3-D VLD device exhibits a higher I_d and larger g_m due to the higher doping concentration. Fig. 7 shows the output characteristics of 2-D VLD and 3-D VLD LDMOS with circular layout at various V_{GS}. The additional $N_{ADD}(r)$ in the 3-D VLD device benefits the improved ON-state BV, large saturation current, and suppressed quasi-saturation effect. The 2-D contours and 1-D profiles of the current density shown in Fig. 8 can give a physical explanation. The heavier impurity in the drift region near the drain enhances the current density and enlarges the conduction region due to the reduced drift region resistance, thus leading to the increased saturation and quasi-saturation currents. Furthermore, the smaller drift region resistance brings a delayed trigger of the parasitic bipolar transistor, thus resulting in a larger ON-state BV. Therefore, the 3-D VLD technique could be expected a higher performance in analog applications.

C. Specific On-Resistance and Baliga's Figure of Merits

Another benefit of the additional $N_{ADD}(r)$ in 3-D VLD LDMOS is the lower specific on-resistance ($R_{on,sp}$), especially

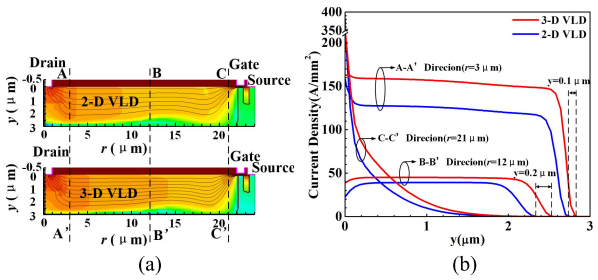

Fig. 8. (a) 2-D contours. (b) 1-D profiles of current density of 2-D and 3-D VLD LDMOS with circular layout (r_d = 2 μm, t_s = 3 μm, t_{ox} = 3 μm, L_d = 20 μm, ΔV_{GS} = 4 V, and V_{DS} = 50 V).

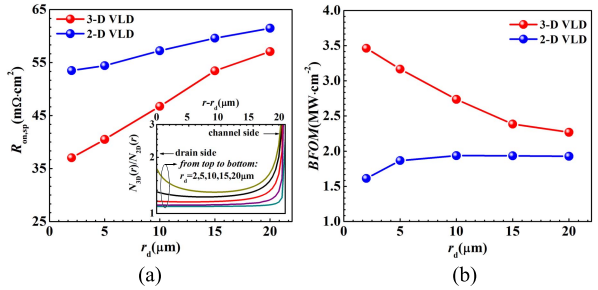

Fig. 9. Comparison of the 2-D and 3-D VLD SOI LDMOS with circular layout. (a) Specific on-resistance. (b) BFOM (t_s = 3 μm, t_{ox} = 3 μm, L_d = 20 μm, V_{GS} = 5 V, and V_{DS} = 0.01 V).

for a small r_d. The simulation results in Fig. 9(a) show that the $R_{on,sp}$ reduces from 53 mΩ·cm^2 of the 2-D device to 37 mΩ·cm^2 of the 3-D device at r_d = 2 μm. The ratio of doping profile in 3-D VLD and 2-D VLD devices are shown in the inset of Fig. 9(a). The horizontal axis in the inset of Fig. 9(a) represents doping concentration of the 2-D VLD device. The additional $N_{ADD}(r)$ contributes to the higher doping concentration in the drift region of the 3-D VLD device, especially at the terminals of the drift region, leading to a lower $R_{on,sp}$. For the large r_d, the drift doping concentration of the 3-D VLD device is nearly the same with that of the 2-D VLD device, except a small region near the source. As a result, the almost same specific on-resistance can be expected for the 2-D and 3-D VLD devices with a large radius of the drain region.

Fig. 9(b) compares the BFOM (BFOM = BV^2/$R_{on,sp}$ [17]) of the 2-D VLD and the proposed 3-D VLD LDMOS with circular layout. Due to the higher BV and lower $R_{on,sp}$, the BFOM of the 3-D VLD LDMOS is larger than that of 2-D VLD LDMOS, especially at small radius. For example, BFOM of the 3-D VLD device is about 2.3 times of BFOM of the 2-D VLD device at r_d = 2 μm.

V. Conclusion

In this paper, a 3-D VLD technique is proposed to suppress the electric field crowding of the SOI LDMOS with a circular layout. The solution of 3-D Poisson equation shows that the uniform surface electric field can be obtained by adding an inverse function to the conventional linear doping profile. Synopsys TCAD tools are employed to verify the theoretical model and explore the physic insight. Compared to

2-D VLD LDMOS, the 3-D VLD device presents an excellent operation performance including high ON/OFF-states BVs, low specific on-resistance, improved BFOM, increased large saturation current, large transconductance, and suppressed quasi-saturation effect. This novel 3-D VLD technique can also be applied in practical lateral power device with other layouts including multifinger and runway layout.

REFERENCES

[1] R. Stengl and U. Gösele, "Variation of lateral doping—A new concept to avoid high voltage breakdown of planar junctions," in *IEDM Tech. Dig.*, Washington, DC, USA, Dec. 1985, pp. 154–157, doi: 10.1109/IEDM.1985.190917.

[2] S. Merchant, E. Arnold, H. Baumgart, S. Mukherjee, H. Pein, and R. Pinker, "Realization of high breakdown voltage (>700 V) in thin SOI devices," in *Proc. ISPSD*, Baltimore, MD, USA, 1991, pp. 31–35, doi: 10.1109/ISPSD.1991.146060.

[3] C. W. Chan, P. A. Mawby, and P. M. Gammon, "Analysis of linear-doped Si/SiC power LDMOSFETs based on device simulation," *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2442–2448, Jun. 2016, doi: 10.1109/TED.2016.2550865.

[4] Z. J. Wang *et al.*, "Realization of 850 V breakdown voltage LDMOS on Simbond SOI," *Microelectron. Eng.*, vol. 91, no. 3, pp. 102–105, 2012, doi: 10.1016/j.mee.2011.10.014.

[5] M. Qiao, C. Li, Y. Liu, Y. Wang, Z. Li, and B. Zhang, "Design of a novel triple reduced surface field LDMOS with partial linear variable doping n-type top layer," *Superlattices Microstruct.*, vol. 93, pp. 242–247, May 2016, doi: 10.1016/j.spmi.2016.03.038.

[6] X. Luo *et al.*, "Novel reduced ON-resistance LDMOS with an enhanced breakdown voltage," *IEEE Trans. Electron Devices*, vol. 61, no. 12, pp. 4304–4308, Dec. 2014, doi: 10.1109/TED.2014.2364842.

[7] Y. Guo, J. Yao, B. Zhang, H. Lin, and C. Zhang, "Variation of lateral width technique in SoI high-voltage lateral double-diffused metal–oxide–semiconductor transistors using high-*k* dielectric," *IEEE Electron Device Lett.*, vol. 36, no. 3, pp. 262–264, Mar. 2015, doi: 10.1109/LED.2015.2393913.

[8] S. Hardikar, R. Tadikonda, D. W. Green, K. V. Vershinin, and E. M. S. Narayanan, "Realizing high-voltage junction isolated LDMOS transistors with variation in lateral doping," *IEEE Trans. Electron Devices*, vol. 51, no. 12, pp. 2223–2228, Dec. 2004, doi: 10.1109/TED.2004.839104.

[9] M. Qiao, Y. Li, X. Zhou, Z. Li, and B. Zhang, "A 700-V junction-isolated triple RESURF LDMOS with n-type top layer," *IEEE Electron Device Lett.*, vol. 35, no. 7, pp. 774–776, Jul. 2014, doi: 10.1109/LED.2014.2326185.

[10] K. Mao, H. Nie, Z. Chen, Y. Yao, and J. Du, "Optimized dynamic R_{ON} with p-type buried layer bridge in 700-V triple RESURF nLDMOS," *IEEE Trans. Electron Devices*, vol. 64, no. 8, pp. 3287–3292, Aug. 2017, doi: 10.1109/TED.2017.2714703.

[11] X. Luo, B. Zhang, Z. Li, Y. Guo, X. Tang, and Y. Liu, "A novel 700-V SOI LDMOS with double-sided trench," *IEEE Electron Device Lett.*, vol. 28, no. 5, pp. 422–424, May 2007, doi: 10.1109/LED.2007.894648.

[12] M. Qiao *et al.*, "3-D edge termination design and $R_{ON,sp}$ -BV model of a 700-V triple RESURF LDMOS with n-type top layer," *IEEE Trans. Electron Devices*, vol. 64, no. 6, pp. 2579–2586, Jun. 2017, doi: 10.1109/TED.2017.2694451.

[13] Y. Suzuki, T. Kishida, H. Takano, Y. Shirai, and M. Suzumura, "3-D effect of cell designs on the breakdown voltage of power SOI-LDMOS," in *Proc. IEEE Int. SOI Conf.*, Sanibel Island, FL, USA, 1996, pp. 134–135, doi: 10.1109/SOI.1996.552530.

[14] G. Yufeng, W. Zhigong, and S. Gene, "A three-dimensional breakdown model of SOI lateral power transistors with a circular layout," *J. Semiconduct.*, vol. 30, no. 11, pp. 51–54, 2009, doi: 10.1088/1674-4926/30/11/114006.

[15] J. Zhang, Y.-F. Guo, D. Z. Pan, and K.-M. Yang, "A novel 3-D analytical method for curvature effect-induced electric field crowding in SOI lateral power device," *IEEE Trans. Electron Devices*, vol. 63, no. 11, pp. 4359–4365, Nov. 2016, doi: 10.1109/TED.2016.2609908.

[16] X. R. Luo *et al.*, "Ultralow ON-resistance SOI LDMOS with three separated gates and high-*k* dielectric," *IEEE Trans. Electron Devices*, vol. 63, no. 9, pp. 3804–3807, Sep. 2016, doi: 10.1109/TED.2016.2589322.

Kemeng Yang (S'18) received the B.S. degree from the Nanjing University of Posts and Telecommunications, Nanjing, China, in 2014, where she is currently pursuing the Ph.D. degree with the College of Electronic and Optical Engineering and College of Microelectronics.

Her current research interests include simulation, modeling and process of power semiconductor devices, and RF devices.

Yufeng Guo (M'05) received the Ph.D. degree in microelectronics and solid-state electronics from the University of Electronic Science and Technology of China, Chengdu, in 2005. He is currently the Dean of the College of Electronic and Optical Engineering and the Vice-Director of the National and Local Joint Engineering Laboratory of RF Integration and Micro-Assembly Technology, Nanjing University of Posts and Telecommunications, Nanjing,China.

David Z. Pan (S'97–M'00–SM'06–F'14) is currently the Engineering Foundation Professor with The University of Texas at Austin, Austin, TX, USA. He has authored over 280 refereed technical papers and has the holder of eight U.S. patents. His current research interests include cross-layer IC designs for reliability, security, manufacturability, physical design, and analog design automation, and CAD for emerging technologies.

Jun Zhang (S'17) received the B.S. degree in microelectronics from the Nanjing University of Posts and Telecommunications, Nanjing, China, in 2013, where he is currently pursuing the Ph.D. degree in microelectronics and solid-state electronics, under the supervision of Prof. Y. Guo.

Since 2016, he has been a Visiting Scholar at The University of Texas at Austin, Austin, TX, USA.

Man Li received the B.S. and M.S. degrees from the Nanjing University of Posts and Telecommunications, Nanjing, China, in 2014 and 2017, respectively.

In 2017, she joined the Nanjing University of Posts and Telecommunications, where she is currently an Assistant Experimentalist with the College of Electronic and Optical Engineering and College of Microelectronics. Her current research interests include power device designs and power device models.

Yi Tong received the B.S. degree from the Beijing University of Aeronautics and Astronautics, Beijing, China, the M.Phil. degree in solid-state electronics from the University of Liverpool, Liverpool, U.K., and the M.Eng. and Ph.D. degrees from the Electrical Engineering Department, National University of Singapore, Singapore.

He is currently with the Nanjing University of Posts and Telecommunications, Nanjing, China, focusing on advanced semiconductor devices.

Lin He received the M.Eng. degree in instrumentation engineering from Southeast University, Nanjing, China, in 2002, and the Ph.D. degree in electronic engineering from the National University of Singapore, Singapore, in 2009.

He was a Research Associate Professor with the Department of Electronic Science and Technology, University of Science and Technology of China, Hefei, China. He is currently a Professor with the Nanjing University of Post and Telecommunication, Nanjing.

Jiafei Yao (M'18) received the B.S. and Ph.D. degrees in microelectronics from the Nanjing University of Posts and Telecommunications, Nanjing, China, in 2010 and 2016, respectively.

He is currently a Lecturer with the College of Electronic and Optical Engineering and College of Microelectronics, Nanjing University of Posts and Telecommunications.