Simplified Model Analysis of Self-Excited Oscillation and Its Suppression in a High-Voltage Common Package for Si-IGBT and SiC-MOS

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***Abstract*— This paper presents the analysis of a simplified model for the design of a module structure that avoids the risk of self-excited oscillation (SE-Osc). A necessary and sufficient simplified model that can extract the critical oscillation mode is proposed based on a comparison of several simplifying steps. The differential equation of the simplified model is solved, and the solution is plotted in the frequency domain to analyze the oscillatory conditions. The simplified model is verified via a time-domain full-model simulation modeled by 3-D electromagnetic simulation and solved by finite-element simulation. Measurements of test modules show consistent oscillatory conditions and frequency. SE-Osc modes are eliminated by reducing the inductance connected to the emitter and increasing the inductance connected to the collector. Increasing the ratio of C_{CE} to C_{GC} increases the risk of self-exciting oscillation. Suppressions of SE-Osc from a common package design with state-of-the-art Si-insulated gate bipolar transistors (IGBTs) presenting small feedback capacitance, SiC-MOS, and hybrids of state-of-art Si-IGBTs and SiC-Schottky barrier diodes are verified.**

***Index Terms*— Common package, feedback capacitance, hybrid, insulated gate bipolar transistor (IGBT), low inductance, Schottky barrier diode, self-excited oscillation (SE-Osc), SiC-MOS, suppression.**

I. Introduction

WIDE bandgap semiconductors have the potential to allow smaller and lighter inverters due to their low switching energy [1]–[4]. In parallel, the improvement of Si-insulated gate bipolar transistor (IGBT) continues to progress. Recent research has shown that reducing feedback capacitance improves the tradeoff relation between switching energy versus dv/dt and di/dt considerably [5]–[9].

Each of these base device technologies presents vastly different capacitance and transconductance characteristics. A noticeable market trend is the emergence of common package platforms intended to avoid significant inverter mechanical design changes between devices.

When new chip technologies are assembled in a common package, module designers may face unexpected oscillation problems, even if the original mounted chip technology did not exhibit any oscillations. These problems are assumed to be caused by the differences in the capacitance, transconductance, and physical behavior of the modulated carriers. There are several oscillation modes [10].

Turn-OFF oscillation (TO-Osc) is the oscillation between the junction capacitance and main loop inductance after the transistor or diode is turned OFF. The frequency ranges from several mehahertz to several tens of mehahertz. Because SiC devices are unipolar, in contrast to bipolar devices such as Si-IGBTs and Si-p-i-n diodes, there is no tail current after the switch is turned OFF, or reverse recovery of the diode occurs [11].

Oscillation is caused by the plasma extraction transition time (PETT), the resonant frequency of the junction capacitance, and the stray inductances of the system. The frequency ranges from approximately 100 MHz to several gigahertz. PETT oscillations may be circumvented by avoiding the crosspoint of V_{ce}-dependent PETT, the resonant frequency of the internal loop inductance, and C_{CE} [12]. Because SiC devices operate in unipolar mode, PETT oscillations do not cause critical problems to SiC devices.

Self-excited oscillation (SE-Osc) occurs when the damping resistance is not sufficiently high to mitigate the oscillations of the L–C loop activated by the current amplification factor and triggered switching incident. The frequency ranges from tens of mehahertz to 100 MHz. These oscillations may be generated by both unipolar and bipolar structures and can occur in both high- and low-inductance circuits. The oscillations can be mitigated by increasing the gate resistance (R_G) [13]–[17], which in turn significantly dampens the SE-Osc; however, an excessively high R_G may lead to an increase in the switching energy and thus reduce the benefits of state-of-the-art devices.

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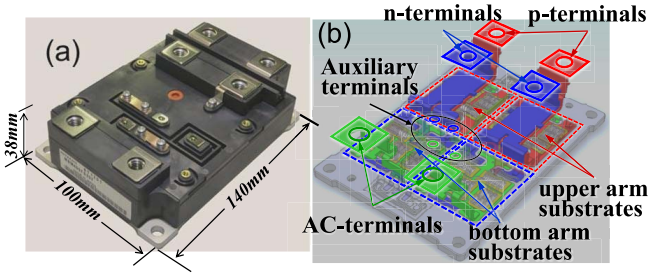


Fig. 1. Low-inductance common package. (a) Photograph. (b) 3-D model.

This research aimed to extract the parameters influencing SE-Osc using a simplified analysis methodology to proactively identify the risks of SE-Osc. The actual measurement results for fabricated devices were then compared to the simulated detailed device models and lumped circuit parameter model. Several iterations of the simplified models were generated to verify their ability to validate the potential for SE-Osc. The simplifying method was applied to three types of semiconductor devices: Si-IGBTs with Si-p-i-n diodes, Si-IGBTs with SiC-Schottky barrier diode (SBD), and Si-IGBTs with SiC-MOS.

This paper further elaborates on the content presented at ISPSD2017 [17] by validating the simplified model process and verifying the model using actual devices.

II. Low-Inductance High-Power Common Package

One common package outline was used to investigate the Si-IGBT, Si–SiC hybrid, and SiC-MOS-FET devices [Fig. 1(a)]. The low-inductance package was used to avoid TO-Osc and thus segregate the SE-Osc. Details of this package and the avoidance of TO-Osc are provided in [11] and [18]. Similar concepts of low-inductance packages have been proposed recently [19]–[22].

The outline dimensions of the common package are stipulated from the application side [23]. Low inductance is realized by narrowing the gap between the p and n terminals [red and blue terminals in Fig. 1(b)]. Arrangement of the module terminals side by side allows the external bus bar to be designed with low inductance. The use of a phase-leg topology in a single package helps to reduce the total inductances and thus avoid TO-Osc. Inside the module, two substrates are connected in parallel to form one arm. SE-Osc is assumed to occur between them. The SE-Oscs can be independently analyzed by eliminating the TO-Osc.

III. Parameters Influencing SE-Osc

Different structures of Si and SiC chips, each with a wide variation of capacitance and transconductance characteristics, were mounted using the common package platform. The transconductance and capacitance characteristics of the various devices are shown in Fig. 2(a)–(d), respectively. In addition, the variations in the output capacitance and feedback capacitance are inversely proportional to the square root of V_{CE} or V_{DS}.

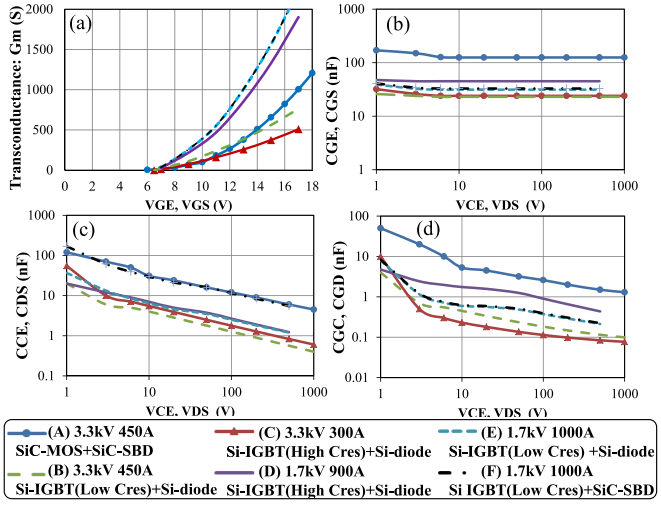


Fig. 2. Transconductance and capacitance characteristics of various voltages (1.7–3.3 kV), structures (low and high C_{res}), and semiconductor materials (Si, SiC, and hybrid). (a) Transconductance, (b) C_{GE} and C_{GS}, (c) C_{CE} and C_{DS}, and (d) C_{GC} and C_{GD}.

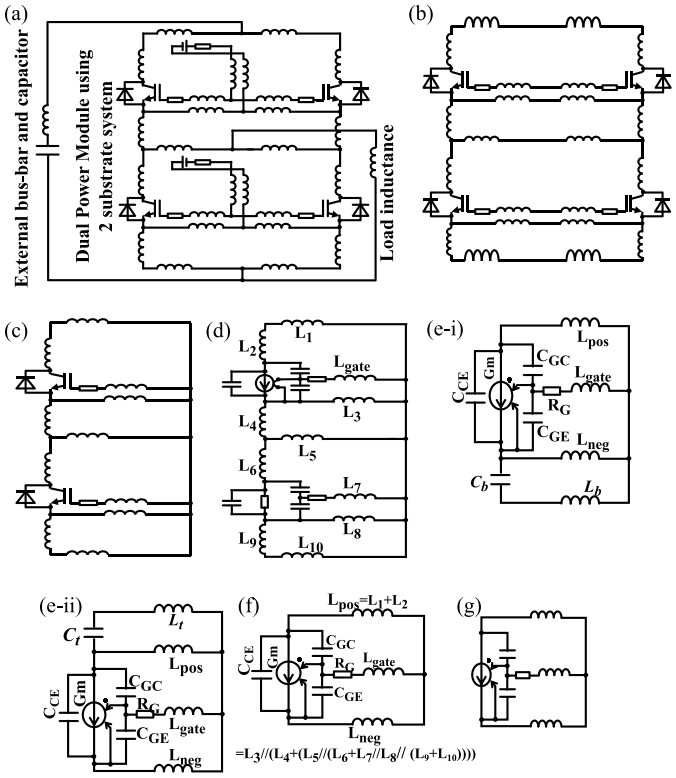


Fig. 3. Simplification steps of circuit model. (a) Fully modeled lumped circuit. (b) Power module model, external circuit removed. (c) Simplified ac model for symmetrical circuit. (d) Simplified MOS model. (e-i) Simplified model with junction capacitance of counter arm. Top arm switching. Bottom arm off-state. (e-ii) Bottom arm switching, top arm off-state. (f) Simplified without junction capacitance counter arm. (g) Simplified without junction capacitance.

IV. Simplifying Model to Analyze SE-Osc

A. Simplifying Circuit Model

Circuit models for analyzing the SE-Osc are shown in Fig. 3. Fig. 3(a) illustrates an entire circuit model, including the gate driver, dc voltage source, and load inductance. Lumped circuit parameters are extracted from the 3-D

$$\begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ C_{CE}\cdot L_{\rm neg}\cdot C_b\cdot L_b & L_{\rm neg}\cdot C_{GE}\cdot C_b\cdot L_b & -(C_{GE}+C_{CE})\cdot L_{\rm neg}\cdot C_b\cdot L_b \end{pmatrix}\cdot\begin{pmatrix} e_C^{(4)} \\ e_G^{(4)} \\ e_E^{(4)} \end{pmatrix}$$
$$+\begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & Gm\cdot L_{\rm neg}\cdot C_b\cdot L_b & -Gm\cdot L_{\rm neg}\cdot C_b\cdot L_b \end{pmatrix}\cdot\begin{pmatrix} e_C^{(3)} \\ e_G^{(3)} \\ e_E^{(3)} \end{pmatrix}$$
$$+\begin{pmatrix} -L_{\rm pos}\cdot(C_{GC}+C_{CE}) & L_{\rm pos}\cdot C_{GC} & C_{CE}\cdot L_{\rm pos} \\ L_{\rm gate}\cdot C_{GC} & -L_{\rm gate}\cdot(C_{GC}+C_{GE}) & L_{\rm gate}\cdot C_{GE} \\ C_{CE}\cdot L_{\rm neg} & L_{\rm neg}\cdot C_{GE} & -\{(C_{GE}+C_b+C_{CE})\cdot L_{\rm neg}+C_b\cdot L_b\} \end{pmatrix}\cdot\begin{pmatrix} \ddot{e_C} \\ \ddot{e_G} \\ \ddot{e_E} \end{pmatrix}$$
$$+\begin{pmatrix} 0 & -L_{\rm pos}\cdot Gm & L_{\rm pos}\cdot Gm \\ R_g\cdot C_{GC} & -R_g\cdot(C_{GC}+C_{GE}) & R_g\cdot C_{GE} \\ 0 & Gm\cdot L_{\rm neg} & -Gm\cdot L_{\rm neg} \end{pmatrix}\cdot\begin{pmatrix} \dot{e_C} \\ \dot{e_G} \\ \dot{e_E} \end{pmatrix}+\begin{pmatrix} -1 & 0 & 0 \\ 0 & -1 & 0 \\ 0 & 0 & -1 \end{pmatrix}\cdot\begin{pmatrix} e_C \\ e_G \\ e_E \end{pmatrix}=0 \quad (1)$$

$$\sum_{n=0}^{12} D_n\cdot s^n=0 \quad (2)$$

$$D_6\cdot s^6+D_5\cdot s^5+D_4\cdot s^4+D_3\cdot s^3+D_2\cdot s^2+D_1\cdot s^1-E=0 \quad (3)$$

electromagnetic simulation. The semiconductor devices linked with a lumped circuit model were simulated through finite-element model (FEM) simulation. A full-model analysis yields the most accurate results; however, the high complexity and CPU requirements can be barriers in the preliminary design phase.

In this model, if the left- and right-hand sides have a symmetrical structure and the external circuit is connected at the midpoint, SE-Osc is generated from inside the module, and the external circuit can be eliminated [Fig. 3(b)]. To analyze the ac components of the oscillation, a complete mirror symmetrical system can be modeled with half of the entire circuit [Fig. 3(c)] [24]. The semiconductor device is replaced with capacitors and a voltage control current source [Fig. 3(d)]. The modeling of the capacitance and current source follows Fig. 2. This modeling is sufficiently accurate for considering turn-ON SE-Osc because the device operates mainly in unipolar mode. When this modeling is applied to bipolar operation, such as turn-OFF or short circuit, modification of the lumped circuit model can increase the accuracy [25].

When a switching event occurs, counter arms is in the OFF-state. If the top switch turns ON and the bottom switch is in the OFF-state, the circuit model can follow Fig. 3(e-i); Fig. 3(e-ii) is applicable in the opposite case. If the influence of the capacitance of the opposite arm is more dominant than the inductance of the opposite arm, the capacitance of the opposite arm (C_b, C_t) may be eliminated, and the circuit model can be described, as shown in Fig. 3(f). Herein, $L_{\rm pos}$ is sum of L_1 and L_2 in Fig. 3(d) and $L_{\rm neg}$ is combined inductance of L_3–L_{10} of Fig. 3(d). If the junction capacitance ($C_{\rm CE}$) of the switching arm is negligible, the circuit model is as shown in Fig. 3(g). The models shown in Fig. 3(e-i), (e-ii), (f), and (g) are validated using actual test results for comparison.

B. Differential Equations

By applying Kirchhoff's current rule, differential equations for Fig. 3(e-i) can be expressed as (1), as shown at the top of this page. To obtain solutions other than zero ($e_C = e_G = e_E = 0$), the determinant of the equation must be zero (2), as shown at the top of this page. By eliminating the dc components shown in the circuit simplifications [Fig. 3(a) and (b)] and by assuming complete mirror symmetry [Fig. 3(b) and (c)], the coefficients of high-order indices are derived as zero, and the equations can be simplified (4). The differential equations for Fig. 3(e-ii) can be expressed via similar steps but using C_t as the OFF-state junction capacitance connected at top side arm. Both equations are deduced in the sixth-order equation and can be solved numerically but not analytically.

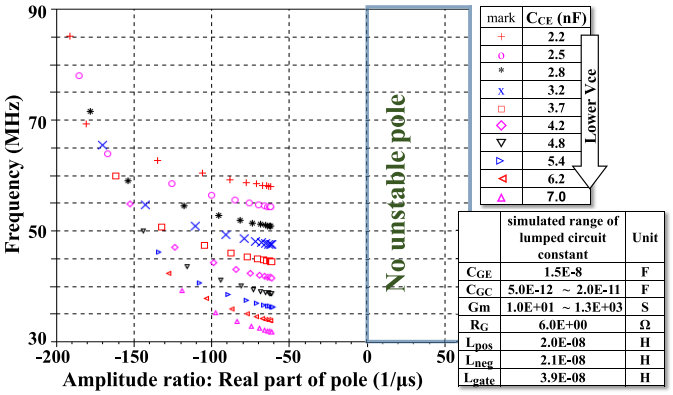
By assuming C_b in (1) as infinite, the differential equation for Fig. 3(f) is derived. By assuming $C_{\rm CE}$ as zero, the differential equation for Fig. 3(g) is derived. The determinants for Fig. 3(f) and (g) are the fourth-order equation, which can be solved analytically as (3), as shown at the top of this page, where

$$D_{12}, D_{11}, D_{10}, D_9, D_8, D_7 = 0. \quad (4)$$

C. Distribution of Solutions in the Frequency Domain

In this section, the solutions of the simplified circuit model are compared to determine which model is the most simplistic to extract the SE-Osc mode without omitting crucial conditions. From an SE-Osc perspective, as the most sensitive device, the 1.7-kV Si-IGBT and SiC-SBD are considered. In this case, the Si-IGBT has a low feedback capacitance, with the SiC-SBD presenting a higher junction capacitance ($C_{\rm CE}$) than the Si-p-i-n diode. The oscillation potential trend is described in the latter half of this paper. Both low feedback capacitance and high junction capacitance make devices oscillate, which is why this device was selected to validate the model.

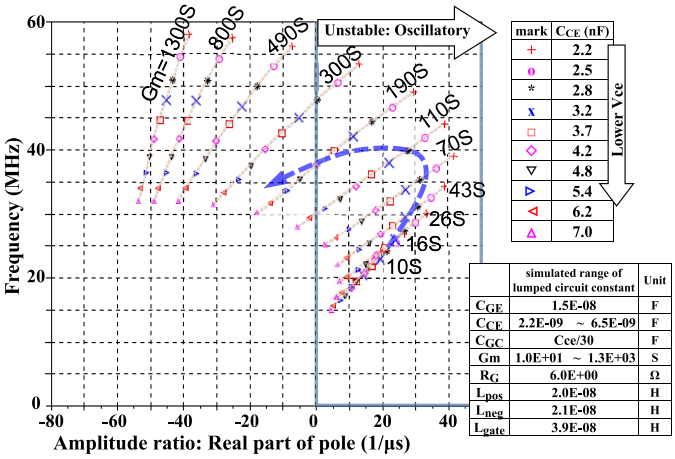
The solutions are plotted in the frequency domain in Figs. 4–7, with the range of parameters listed in the side table for the simplified circuits of Fig. 3(g), (f), (e-i), and (e-ii).



mark	C_{CE} (nF)
+	2.2
o	2.5
*	2.8
x	3.2
□	3.7
◇	4.2
▽	4.8
▷	5.4
◁	6.2
△	7.0

	simulated range of lumped circuit constant	Unit
C_{GE}	1.5E-8	F
C_{GC}	5.0E-12 ~ 2.0E-11	F
Gm	1.0E+01 ~ 1.3E+03	S
R_G	6.0E+00	Ω
L_{pos}	2.0E-08	H
L_{neg}	2.1E-08	H
L_{gate}	3.9E-08	H

Fig. 4. Solutions plotted in the frequency domain calculated using the simplified model shown in Fig. 3(g). The side table provides the simulated range of parameters.



mark	C_{CE} (nF)
+	2.2
o	2.5
*	2.8
x	3.2
□	3.7
◇	4.2
▽	4.8
▷	5.4
◁	6.2
△	7.0

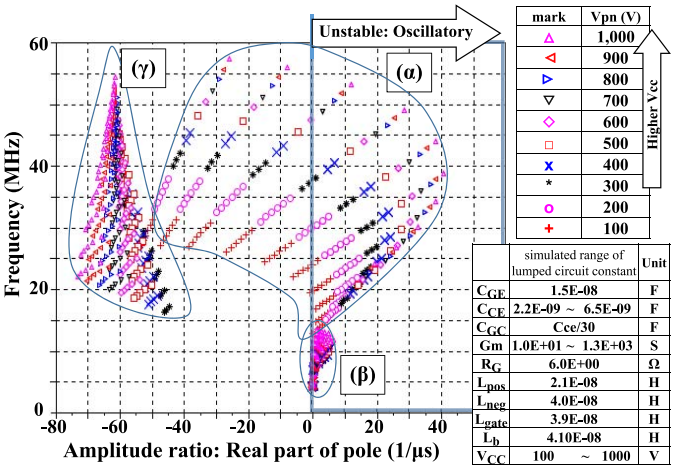
	simulated range of lumped circuit constant	Unit
C_{GE}	1.5E-08	F
C_{CE}	2.2E-09 ~ 6.5E-09	F
C_{GC}	Cce/30	F
Gm	1.0E+01 ~ 1.3E+03	S
R_G	6.0E+00	Ω
L_{pos}	2.0E-08	H
L_{neg}	2.1E-08	H
L_{gate}	3.9E-08	H

Fig. 5. Solutions plotted in the frequency domain calculated using the simplified model shown in Fig. 3(f). The side table provides the simulated range of parameters.

In these figures, the vertical value is the frequency, and the horizontal value is the increase in the ratio of amplitude per microsecond. The unstable point is to the right of the zero value. Any low-amplitude disturbance grows exponentially and reaches infinity over a long period. However, the switching instance does not remain constant under the same condition. Therefore, if the amplitude ratio is sufficiently high and the unstable period is sufficiently long, SE-Osc may appear in the waveform in the time domain. The plot to the left of the zero value represents stable operation and decaying amplitudes and thus does not contribute to the SE-Osc.

First, Fig. 4 does not show any positive amplitude ratio. Thus, the simplified circuit shown in Fig. 3(g) is not a sufficient model to extract the conditions of SE-Osc.

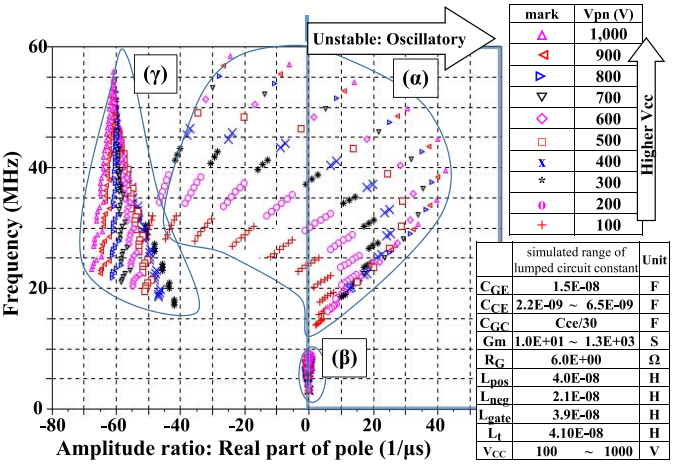
In Fig. 5, the solutions of the simplified model in Fig. 3(f) are plotted, revealing unstable conditions. The turn-ON phenomenon starts from low Gm and low C_{CE}, and both values increase as shown by the dashed arrow curve. In this process, the trace starts from 25 MHz, with the amplitude ratio increasing from 20 and reaching a maximum amplitude ratio before decreasing to a negative value. This trace indicates the generation of SE-Osc. Comparing the results in Figs. 4 and 5, the junction capacitance C_{CE} must be taken into consideration to extract the unstable conditions.



mark	Vpn (V)
△	1,000
◁	900
▷	800
▽	700
◇	600
□	500
x	400
*	300
o	200
+	100

	simulated range of lumped circuit constant	Unit
C_{GE}	1.5E-08	F
C_{CE}	2.2E-09 ~ 6.5E-09	F
C_{GC}	Cce/30	F
Gm	1.0E+01 ~ 1.3E+03	S
R_G	6.0E+00	Ω
L_{pos}	2.1E-08	H
L_{neg}	4.0E-08	H
L_{gate}	3.9E-08	H
L_b	4.10E-08	H
V_{CC}	100 ~ 1000	V

Fig. 6. Solutions plotted in the frequency domain calculated using the simplified model shown in Fig. 3(e-i). The side table provides the simulated range of parameters.



mark	Vpn (V)
△	1,000
◁	900
▷	800
▽	700
◇	600
□	500
x	400
*	300
o	200
+	100

	simulated range of lumped circuit constant	Unit
C_{GE}	1.5E-08	F
C_{CE}	2.2E-09 ~ 6.5E-09	F
C_{GC}	Cce/30	F
Gm	1.0E+01 ~ 1.3E+03	S
R_G	6.0E+00	Ω
L_{pos}	4.0E-08	H
L_{neg}	2.1E-08	H
L_{gate}	3.9E-08	H
L_t	4.10E-08	H
V_{CC}	100 ~ 1000	V

Fig. 7. Solutions plotted in the frequency domain calculated using the simplified model shown in Fig. 3(e-ii). The side table provides the simulated range of parameters.

Figs. 6 and 7 show the results in which the junction capacitances of the counter arm (C_b and C_t) are taken into consideration. Here, the sum of the voltage, top and bottom, is assumed to be the source voltage (V_{pn}). In the actual system, the transient voltage of the stray inductances, represented by the product of the stray inductance and the current derivative, is superimposed on the V_{CC}.

The capacitance in the opposite arm is a function of V_{CE} and V_{pn}. Considering that the device structure is the same for both arms, the dependence can be derived from Fig. 2(c). Decreasing the capacitance of one arm causes an increase in the counter arm capacitance.

In the case of the simplified model Fig. 3(e-i), as shown in Fig. 6, there are three distributions (α, β, and γ). Distribution α is same as Fig. 5, which means that without considering the counter arm capacitance, unstable conditions distributed at α can be extracted. Solution γ does not cause SE-Osc because of the negative amplitude ratio. However, distribution β is located on the positive amplitude ratio but has a considerably lower amplitude ratio than the solution in α. Moreover, the

TABLE I
COMBINATIONS OF PARAMETERS. TOTAL OF 281 600 COMBINATIONS

	Parameter	Unit	min value	max value	times by step	number of step
1)	L_{pos}	H	2.0E-08	1.6E-07	2	4
2)	L_{neg}	H	1.0E-08	8.0E-08	2	4
3)	L_{gate}	H	4.0E-08	3.2E-07	2	4
4)	C_{GE}	F	6.0E-09	4.8E-08	2	4
5)	Gm	S	100	800	2	4
6)	R_G	Ω	6	96	2	5
7)	C_{CE}	F	1.5E-10	1.5E-08	10^0.2	11
8)	C_{CE}/C_{GC}	times	1.9	30.0	2	5
9)	(C_{GC})	(F)	(5.0E12)	(8.0E-09)		
10)	number of total combination					281,600

frequency of α is higher than that of β. Thus, the SE-Osc caused by and distributed in α is considerably more dominant than that of β. These results indicate that the critical SE-Osc from the simplified circuit Fig. 3(e-i) can be extracted without considering the junction capacitance C_b.

Fig. 7 shows the solution distribution of the simplified circuit Fig. 3(e-ii). Similar to Fig. 6, three distributions appear, where the α and γ plots are identical to Fig. 3(e-i), and distribution β shows a further lower value than the distribution β of Fig. 6.

Considering a higher amplitude ratio and frequency of α than β or γ, suppressing the SE-Osc in the simplified circuit Fig. 3(f) is the necessary and sufficient model for analyzing the critical SE-Osc. In Section V, the parameters of the simplified model of Fig. 3(f) that influence SE-Osc are shown and verified with test modules mounted with several types of semiconductor devices.

V. PARAMETERS AFFECTING SE-OSC

Based on the results presented in Section IV, the simplified model shown in Fig. 3(f) is adopted. The influential parameters are extracted, and a counter measure for SE-Osc is presented. The results of the high-level simulation and experimental results of the test modules are compared.

A. Parameter for Extracting Unstable Poles Using the Simplified Circuit Model

The lumped circuit constants are provided in Table I. These constants are selected to have a wider dynamic range than the values shown in Fig. 2. The increments of C_{CE} are set at smaller values than for the other parameters because C_{CE} varies continuously by voltage. C_{GC} varies continuously. Its dependence on voltage is the same as that of C_{CE}. Therefore, C_{CE}/C_{GC} is handled as a variable parameter (Table I, row 9), and its influence is investigated. The total number of combinations is 281 600. Among these combinations, a total of 20 220 poles are extracted as unstable poles.

B. Analysis of Unstable Poles Based on the Simplified Circuit Model

The unstable poles are plotted in the frequency domain in Fig. 8. The existence of a pole indicates the risk of SE-Osc. Fig. 8(a) shows schematic oscillation waveforms in the time domain for respective points in the frequency domain. The amplitude of the schematic oscillation is normalized to zero at time zero.

In Fig. 8(b)–(h), changes in the C_{CE} trace are interpolated while the other parameters remain unchanged. The number of

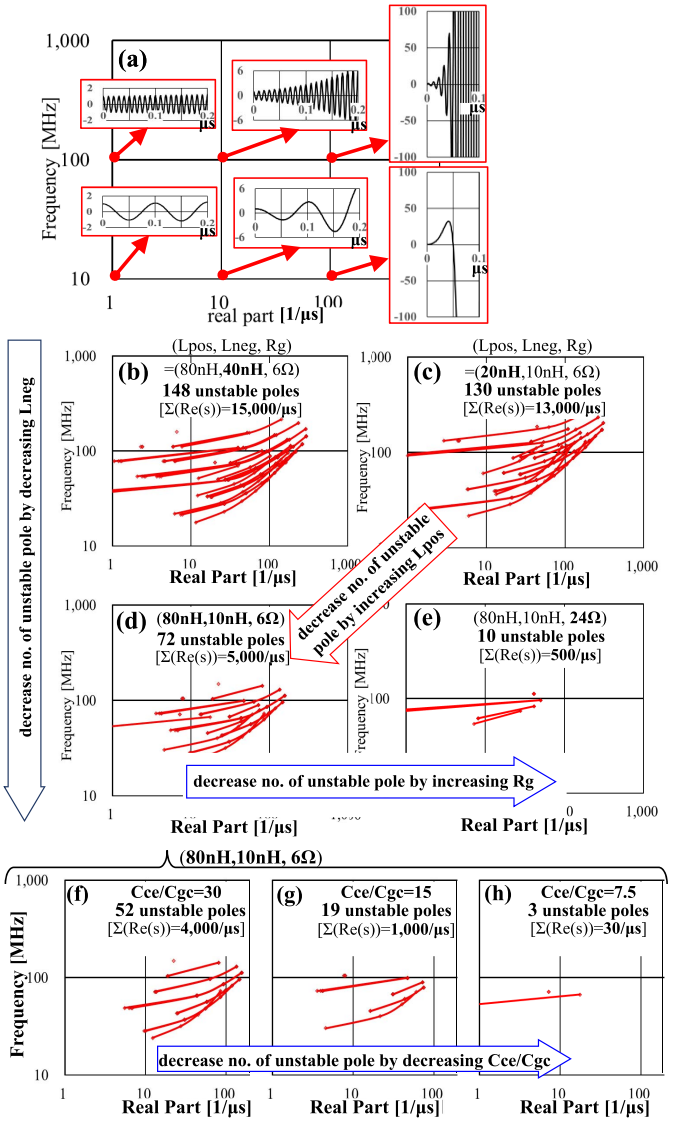


Fig. 8. Unstable poles plotted in the frequency domain calculated using a simplified model for the combination shown in Table I. (a) Schematic oscillation waveforms, unstable pole from (b) high L_{pos} and Lneg, (c) low L_{pos} and L_{neg}, (d) high L_{pos} and low L_{neg}, (e) high Rg, (f) high, (g) medium, and (h) low C_{ce}/C_{gc}.

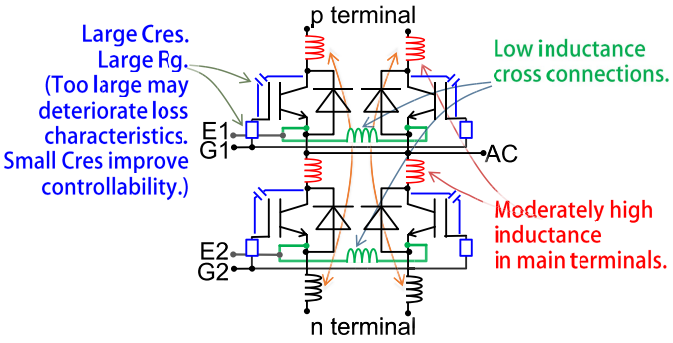


Fig. 9. Methods to mitigate the risk of SE-Osc.

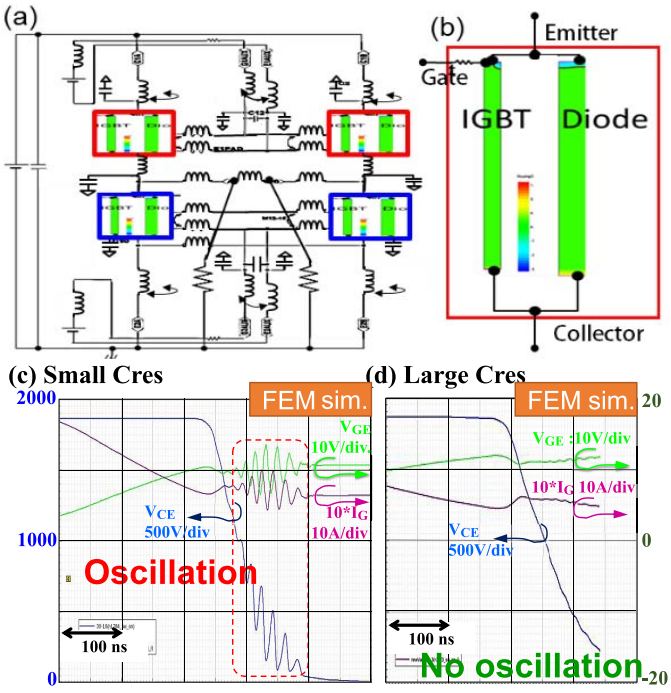


Fig. 10. Comparison of turn-on waveforms for small C_{res} [(c), $C_{CE}/C_{GC} = 30$] and large C_{res} [(d), $C_{CE}/Cge = 7.5$] via high-level FEM simulation of A 3.3 kV, 450 A module with the package structure of Fig. 3(a). (a) Simulated circuit model. (b) Si device model.

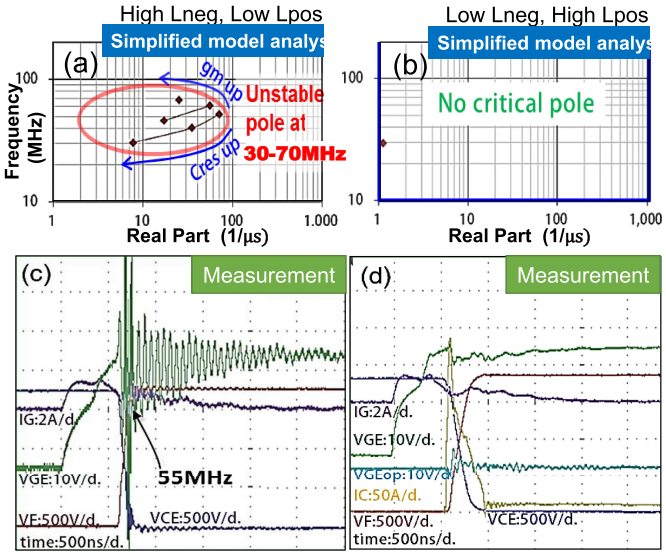


Fig. 11. Comparison of the turn-on waveforms of a low-C_{res} chip in the modules. (a) and (c) Low-L_{pos} and high-L_{neg} package designs. (b) and (d) High-L_{pos} and low-L_{neg} designs.

extracted unstable poles is shown in the graph. Qualitatively, increased numbers toward the right-hand side indicate larger oscillations.

The value of the sum of the real parts of the unstable poles is shown in black. The absolute value does not have any physical meaning but is useful for comparing oscillatory tendencies.

The number decreases with decreasing L_{neg} [(b)→(d)], increasing L_{pos} [(c)→(d)], increasing R_g [(d)→(e)], and increasing C_{CE}/C_{res} [(f)→(h)]. The oscillatory tendency of the system can be assessed based on these four measures.

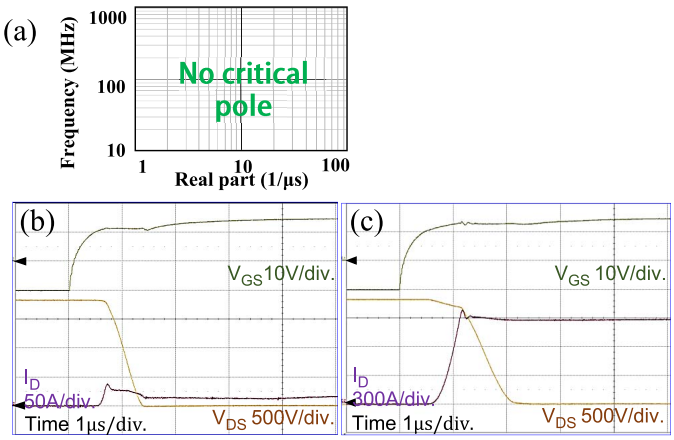
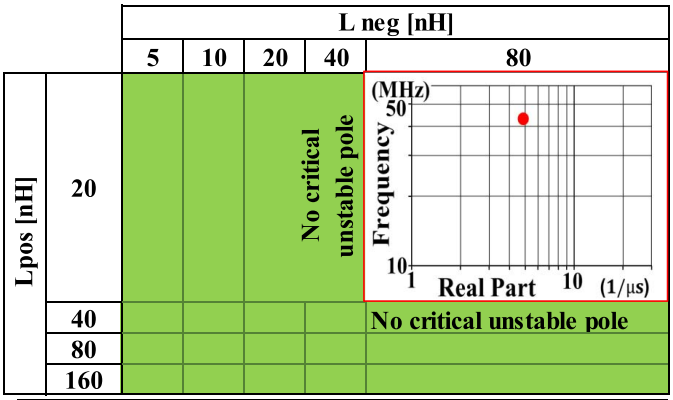


Fig. 12. (a) Results of the pole analysis using a simple model of a 3.3-kV SiC-MOS module. (b) and (c) Measured turn-on waveforms 10 and 900 A.



components	simulated range of lumped circuit constant			Unit
C_{GE}	1.5E-08			F
C_{CE}	**1.2E-09**	~	**5.2E-08**	**F**
C_{GC}=C_{CE}/7.5	1.6E-10	~	6.9E-10	F
Gm	6.0E+01	~	1.0E+03	S
R_G	6.0E+00			Ω
L_{pos}	**2.0E-08**	~	**1.6E-07**	**H**
L_{neg}	**5.0E-08**	~	**8.0E-07**	**H**
L_{gate}	4.0E-08			H

Fig. 13. Unstable pole plot of the 1.7 kV, Si-IGBT + Si-p-i-n diode in the frequency domain simulated with the simplified model.

Fig. 9 shows schematic countermeasures against SE-Osc. Increasing the internal gate resistance may reduce oscillations. However, increasing the internal gate resistance will decrease the switching speed and result in a higher switching loss. Increasing C_{GC} reduces the gate controllability, which might in turn result in a lower Eon + Err with low dv/dt. Modestly higher L_{pos} and lower L_{neg} values can be realized in a single switch module when parallel systems are connected. However, with a phase-leg package, L_{pos} of the upper arm and L_{neg} are mutually connected, with L_{neg} of the upper arm and L_{pos} of the bottom arm sharing a common path. Therefore, in the system design, the low-inductance cross connection between systems

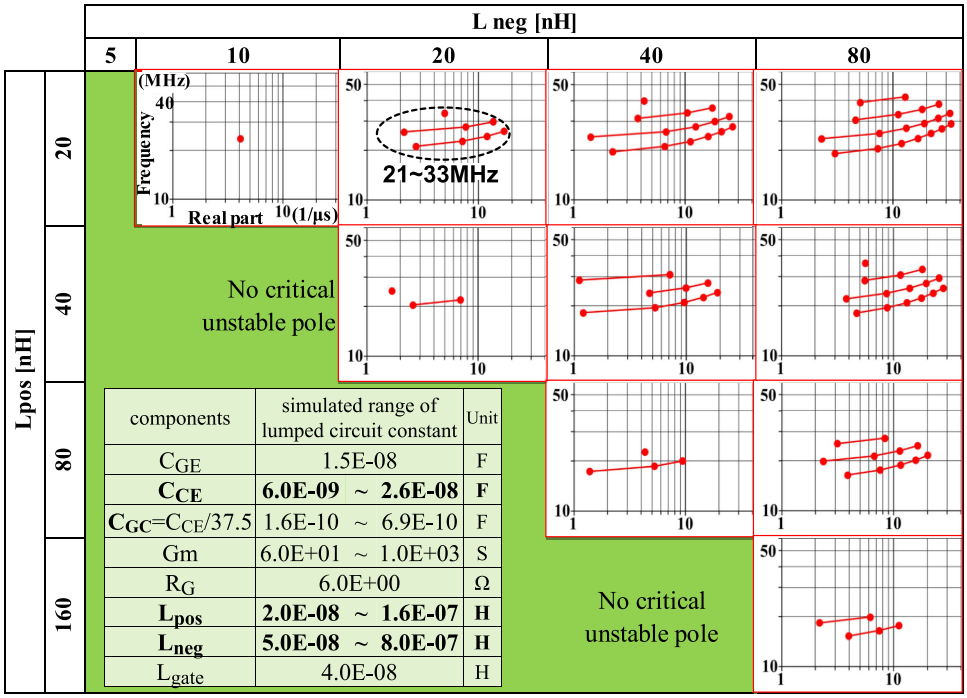


Fig. 14. Unstable pole plot of the 1.7 kV, Si-IGBT + SiC-SBD in the frequency domain simulated with the simplified model.

and the moderate inductance of the main terminal must be considered.

C. Verification of Unstable Poles Extracted From the Simplified Circuit Model

1) *SE-Osc From Si-IGBT With Si-p-i-n Diode:* The device model and lumped circuit model extracted using 3-D electromagnetic simulation were verified via high-level FEM simulation. Fig. 10 shows the comparison of the turn-ON waveforms between small and large C_{res} corresponding to Fig. 8(f) and (h). Device structures are handled in [5] and [26], respectively. The proposed simplified calculation shows good consistency with the detailed numerical simulation.

Fig. 11 shows one example of applying the method to avoid SE-Osc. As shown in Fig. 9, a small-C_{GC} chip design tends to generate SE-Osc. Using this chip, counter measure by module design was verified experimentally. The high-L_{neg} and low-L_{pos} design shows turn-ON oscillation with a frequency of 55 MHz, which is consistent with simplified calculation showing an unstable pole at 30–70 MHz [Fig. 10(a) and (c)]. Reducing L_{neg} and increasing L_{pos} erase unstable poles [Fig. 10(b)], and the trial module does not exhibit SE-Osc [Fig. 10(d)] without increasing the internal gate resistance.

2) SE-Osc From SiC-MOS-FET: Fig. 12 shows the switching waveforms of a 3.3-kV SiC-MOS assembled in the common package, which exhibits no SE-Osc. Despite 10 times larger capacitances compared to Si-IGBT (Fig. 2 symbols (A) and (B)), SiC-MOS unstable conditions can be predicted from the simplified model calculation, and SE-Osc can be avoided using a single package design.

3) SE-Osc From a Si-IGBT + SiC-SBD Hybrid: A hybrid module consisting of Si-IGBT and SiC-SBD(Si + SiC) is compared with Si-IGBTs with a Si-diode (Si + Si). Si-IGBT has a low feedback capacitance. The characteristics are shown in Fig. 2 (symbols (F) and (E)). Because the same IGBTs with the same number of parallel dies are used, the transconductances [Fig. 2(a)], C_{GE} [Fig. 2(b)], and C_{GC} [Fig. 2(d)] are the same. However, C_{CE} of the hybrid version is considerably higher than that of Si because of the thinner drift width of SiC-SBD. This higher C_{CE} results in a higher value of C_{CE}/C_{GC} than for Si. Fig. 8(f)–(h) illustrates that Si + SiC is most prone to self-excitation. L_{pos} and L_{neg} are used as survey parameters. Fig. 13 shows the unstable poles of Si + Si calculated from the simplified model. The only combination arising in unstable poles is the cell at $L_{pos} \leq 20$ nH and $L_{neg} \geq 80$ nH.

Fig. 14 shows the unstable poles of the Si + SiC calculated from simplified model. The oscillatory range is wider than that of Si + Si (Fig. 13), and a border between oscillatory and nonoscillatory behavior exists at $L_{pos} \times 0.5 \geq L_{neg}$.

Three types of dual modules were assembled to compare the turn-ON waveforms (Fig. 15). Dual modules typically have different L_{pos} and L_{neg} combinations between the top arm and bottom arm. The top row shows the Si + Si, with the comparative L_{pos} and L_{neg} for the top and bottom shown in Fig. 15. No oscillations were observed in the top- or bottom-arm waveforms. The second column shows the Si + SiC. For the top arm, the comparative inductance combination is outside of the $L_{pos} \times 0.5 \geq L_{neg}$ relation. As predicted, oscillations are observed with a frequency of 29 MHz. This observation is consistent with the results of Fig. 14 for (20 nH, 20 nH), showing the unstable pole at 21–33 MHz. By contrast, the bottom arm does not show oscillation because the

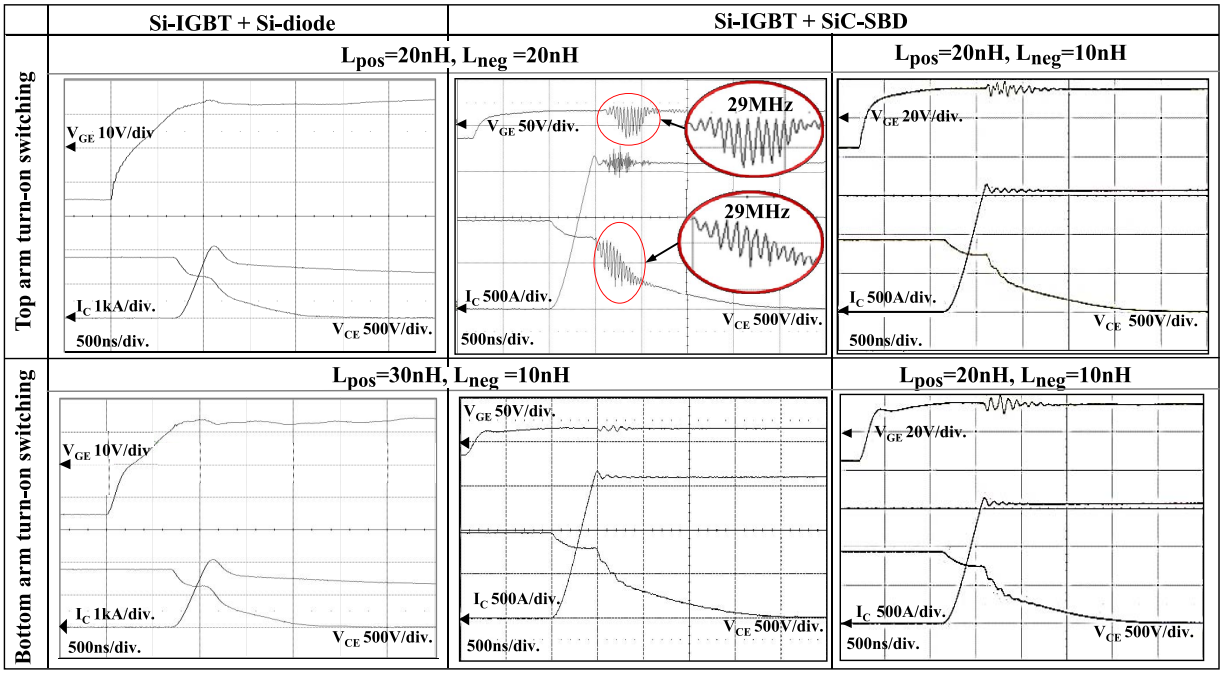


Fig. 15. Comparison of the turn-on waveforms between the top arm (top row) and bottom arm (bottom row) and among Si + Si (left), Si + SiC (middle), and countermeasured Si + SiC (right). The switching conditions are $T_j = 150$ °C, $V_{CC} = 900$ V, $V_{ge} = \pm 15$ V, $L_s = 40$ nH, $R_g = 2.7\ \Omega$, and Ic = 1400 A.

comparative inductance combination fulfills the Lpos $\times 0.5 \geq L_{neg}$ relation.

The bottom row displays the results of a module with a modified internal inductance. By reducing L_{neg} of the top arm from 20 to 10 nH, L_{pos} of the bottom arm decreases from 30 to 20 nH because the inductive path of L_{neg} of the top arm is a common path of L_{pos} of the bottom arm. A jumping cable or cross wire bonding is efficient to establish the desired inductance structure.

By adopting this measure, severe turn-ON oscillations from the top arm can be suppressed. Although minor oscillations on the gate waveforms can be observed, these oscillations can be suppressed by increasing the gate resistance without impacting the switching loss considerably.

The oscillatory trend was surveyed, and the directions of counter measures were proposed using a simplified model analysis. The validity of this model and effectiveness of the counter measures were verified with test modules.

VI. Conclusion

This paper proposed a simplified model analysis to design a module structure, avoiding the risk of SE-Osc. Oscillatory conditions were extracted analytically by simplifying both the semiconductor device and lumped circuit model. The model was validated via FEM simulation and measurement results of the test modules. SE-Osc can be prevented for state-of-the-art Si-IGBTs having a small feedback capacitance, SiC-MOS, and mounted Si + SiC hybrid in the common package design.

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